CURRENT MIRROR CIRCUIT WITH ACCURATE MIRROR GAIN FOR LOW β TRANSISTORS[*]

Huiting Chen**, Frank Whiteside***, Randall Geiger**

**Iowa State University
Ames, IA 50011, USA

*** Dallas Semiconductor Corp.
Dallas, TX 75244, USA

ABSTRACT

A new current mirror with accurate mirror gain for low β transistors is presented. The new current mirror employs a cascoded output stage to provide high output impedance. High mirror gain accuracy is achieved by using a split-collector transistor to compensate for base currents of the source-coupled transistor pair. The split factor is dependent on the desired mirror gain and the nominal β value.

1. INTRODUCTION

The current mirror is one of the most basic building blocks used in linear IC design. Although CMOS process have become dominant in applications requiring a large amount of digital circuitry on a chip, BJT circuits in either Bi-MOS or bipolar processes remain popular for high-speed applications due to the very high unity-gain frequencies attainable with modern bipolar transistors. Unfortunately, in bipolar transistors, the base control terminal draws a nonzero input current. Specially, for lateral transistor, the base current in some processes may be as large as 20% (for β = 5) of the collector current. In a simple bipolar current mirror with β = 5, the base current will cause a 30% error in current mirror gain. There are several known approaches for minimizing the base current effects [1]-[3]. Most are suitable for high β transistors where the detrimental effects of base current loss on mirror gain are already modest. For low β transistors, most existing methods show either poor accuracy or poor frequency response.

In this paper, a new approach for designing bipolar current mirrors is presented. The new current mirror has smaller gain errors due to base current loss than previously reported structures and is most beneficial when an accurate mirror gain is required from low β transistors. The new current mirrors can be implemented in bipolar or Bi-MOS processes or in CMOS process with the parasitic bipolar transistors.

In Section 2, existing approaches to designing bipolar current mirror with base current compensation are reviewed. The new low β current mirror is introduced in Section 3 and its performance is compared with that of existing structures.

2. BACKGROUND

A simple bipolar current mirror structure is shown in Figure 1. In this structure, a constant current source I_{in} is fed into the collector of the diode-connected transistor Q1 establishing a voltage across the base-emitter junction of Q1. This voltage is impressed across the base-emitter terminals of Q2. If Q1 and Q2 are matched, the emitter currents of Q1 and Q2 will be the same. If the base currents of Q1 and Q2 are negligibly small, it follows that the output current I_{out} will be the same as the input current. If the base currents are not negligibly small, this current mirror has an output current I_{out} that is smaller than the input current because a current whose value is equal to the sum of base currents of Q1 and Q2 is subtracted from the input current before it reaches the collector of Q1. Taking these two base currents into account and assuming Q1 and Q2 are perfectly matched, the current mirror gain is given by

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\frac{2}{\beta}} \tag{1}$$

where β is the transistor current gain of Q1 and Q2.

The current mirror gain error is defined by the expression

$$GainError = \left| \frac{A - A_{nom}}{A_{nom}} \right| \times 100(\%) \tag{2}$$
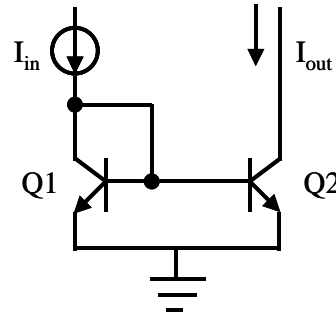

Figure 1. The simply bipolar current mirror

For lateral transistors, β is often in the range of only 4 to 20. For such transistors, the current mirror gain error is too large for most applications. For example, the current mirror gain error from (2) will be 30% if β = 5

A well-known modification of the simple current mirror that partially compensates for base current loss is shown in Figure 2. An emitter-follower buffer, Q3, is included between emitter and base of Q1. The sum of the base currents of Q1 and Q2 is divided by (β+1) of Q3 resulting in a smaller current that has to be subtracted from the input current I_{in}. Assuming $\beta_1 = \beta_2 = \beta_3 = \beta$, then the current mirror gain of the circuit of Fig. 2 is given by

---

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\dfrac{2}{\beta^2+\beta}} \cong \frac{1}{1+\dfrac{2}{\beta^2}} \qquad (3)$$

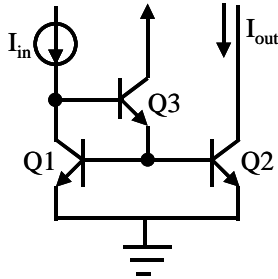For $\beta=5$, the current mirror gain error will be around 7%.

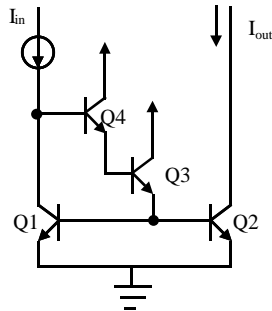**Figure 2**. A current mirror with an emitter-follower buffer to provide base current compensation.

Figure 3. A current mirror with Darlington configuration to compensate for the base currents

To further minimize the base current effect, the Darlington configuration can be used to achieve a larger current gain in the feedback amplifier. The current mirror structure based upon the Darlington compensation is shown in Figure 3. For this structure, the sum of the base currents of Q1 and Q2 is divided by $(\beta+1)^2$ resulting in a much smaller current that has to be subtracted from the input current I_{in}. Again assuming all the transistors are matched, the current mirror gain is given by

$$A = \frac{I_{out}}{I_{in}} = \frac{1}{1+\dfrac{2}{\beta^3+2\beta^2+\beta}} \cong \frac{1}{1+\dfrac{2}{\beta^3}} \qquad (4)$$

For $\beta=5$, the current mirror gain error will be about 1.6%. Although this structure does offer improvements in mirror gain accuracy, this current mirror has a poor high frequency response due to the fact that base current of Q3 is small and it takes long time to charge the parasitic capacitances at the base of Q3.

In the BiCMOS processes, an NMOS transistor can be added to compensate for the base currents. The structure is shown in Figure 4. If Q1 and Q2 are perfectly matched, this current mirror has an output current I_{out} exactly equal to the input current I_{in} due to the fact that no base current is subtracted from the input current. Unfortunately, the MOS transistor is not available in standard bipolar processes.
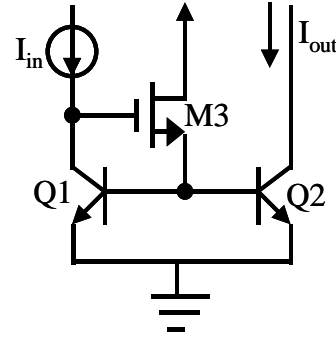
Figure 4. A current mirror with a MOS transistor to compensate for the base current

A bipolar transistor with a split-collector can be used to improve the current match between the input and output of the current mirror [3]. The split-collector current mirror structure is shown in Figure 5. A single split-collector transistor Q4 is used in this structure. The emitter of Q4 is connected to the common base of the transistors Q1 and Q2, the base terminal of Q4 is connected to collector of Q2, and one part of the split collector of Q4 is also connected to the collector of Q2. The other part of the split collector is directly connected to output. The cascoding transistor Q3 provides a high impedance at the output node and at the same time provides a compensation current to I_{in}. A routine analysis shows that the current mirror gain is given by the expression

$$A = \frac{I_{out}}{I_{in}} = \frac{M-(M-1)*\dfrac{1}{1+\beta}+[(1-\theta)M-\theta]*\dfrac{1}{(1+\beta)^2}-(1+M)(1-\theta)*\dfrac{1}{(1+\beta)^3}}{1+(M-1)*\dfrac{1}{1+\beta}-[(1-\theta)M-\theta]*\dfrac{1}{(1+\beta)^2}+(1+M)(1-\theta)*\dfrac{1}{(1+\beta)^3}} \qquad (5)$$

where M is the ratio of the emitter areas of Q2 to Q1 and θ is the collector current split factor. For M=1 and $\theta=1/2$, the mirror gain expression of (5) reduces to

$$A = \frac{I_{out}}{I_{in}} = \frac{1-\dfrac{1}{(1+\beta)^3}}{1+\dfrac{1}{(1+\beta)^3}} \qquad (6)$$

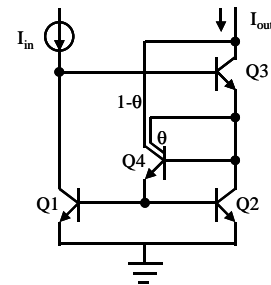For $\beta= 5$, then the mirror gain error is about 0.92%.

Figure 5. A current mirror with a split-collector BJT to compensate for the base currents [3]

Although the split-collector mirror gain is much more accurate than what is achievable with either the basic mirror or the base current compensated structure of Fig. 2, this mirror can get good current matching only when M is close to 1. For mirror gains

larger than 1, the first-order $(1+\beta)$ terms of the numerator and denominator in (5) no longer disappear and become dominant resulting in a large error in the mirror gain. For example, when M=2, the mirror gain error is around 30% for $\beta = 5$.

This paper provides a new design of a bipolar current mirror with base current compensation for low β transistors. The new structure is not only suitable for unity mirror gain but also for mirror gains greater than 1.

3. PROPOSED CURRENT MIRROR

A new current mirror structure is shown in Figure 6. In this structure, the base current loss is compensated by ideally subtracting a corresponding current from the output current. To achieve this, one split collector of Q3 is directly connected to the output and the other split collector is connected to the emitter of Q4. Part of collector current is divided by $(\beta+1)$ of Q4 and then subtracted from I_{out}. Assuming that all transistors have the same β, the current mirror gain is given by

$$A = \frac{I_o}{I_{in}} = M \cdot \frac{1 + \frac{(1+M)}{(1+\beta)} \cdot \frac{1}{M} \cdot \left[(1-\theta) + \frac{\theta}{(1+\beta)}\right]}{1 + \frac{(1+M)}{\beta \cdot (1+\beta)}} \qquad (7)$$

where M is ratio of the emitter areas of Q2 to Q1. It follows from (7) that the current mirror gain is exactly equal to M when $\theta = \frac{(1+\beta)\ (\beta-M)}{\beta^2}$. M has to be smaller than β to satisfy the condition of $0<\theta<1$.
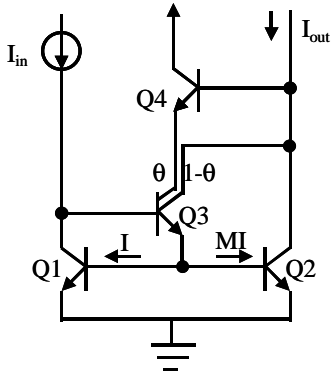

Figure 6. A current mirror with a split-collector transistor to compensate for the base currents

Due to process variations, the value of β may be different from its nominal value. Table 1 shows the current mirror gain error for the new circuit due to process variations of $\pm$ 20% and $\pm$ 30% for several different mirror gains and several different nominal values for β.

From Table 1, it is apparent that the mirror gain error is highest for low β and high M. For M=1 and β=5, the gain error is 1.28%, which is comparable to Mesa's work [3]. For mirror gains greater than 1, the proposed current mirror gives much smaller mirror gain errors than the circuit of Figure 5.

Table 1: Current mirror (Figure 6) gain error due to process variation of β.

β	M	Mirror (Fig. 6) gain Error (%)			
		-20%	+20%	-30%	+30%
15	13	1.63	0.78	3.09	1.00
	9	1.16	0.54	2.20	0.70
	5	0.65	0.30	1.25	0.39
	1	0.04	0.01	0.07	0.02
10	9	2.40	1.19	4.50	1.55
	5	1.40	0.67	2.65	0.87
	1	0.11	0.04	0.22	0.05
5	4	3.84	2.04	6.95	2.67
	3	2.98	1.54	5.45	2.01
	2	1.98	0.99	3.68	1.29
	1	0.65	0.29	1.28	0.36

Two issues of concern when designing any current mirror are the mirror gain accuracy and the output impedance of the current mirror. Multiple output current mirrors are also required in some applications. Two modifications of the basic circuit of Figure 6 follow. One version has a high impedance output and another has multiple outputs. Both have good current mirror gain accuracy even with low values of β.

3.1 Proposed current mirror with high output impedance

To increase the output impedance, a cascode version of above design is introduced. This current mirror has higher output impedance and better current matching. Figure 7 shows the modified current mirror structure. Various known methods can be used to generate the bias voltage, V_{bias} that is used to bias the cascode transistors.
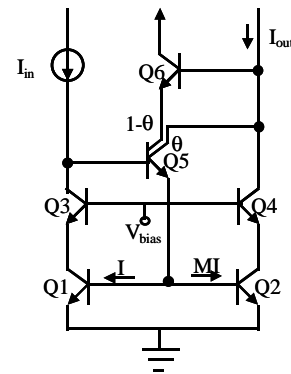

Figure 7. A cascode current mirror with split-collector to compensate for the base currents

The nominal current mirror gain is given by (8)

$$\frac{I_o}{I_{in}} = M \cdot \frac{1 + \frac{(1+M)}{\beta^2} \cdot \frac{\beta}{M} \cdot \left[\theta + \frac{1-\theta}{(1+\beta)}\right]}{1 + \frac{(1+M)}{\beta^2}} \qquad (8)$$

The current mirror gain is exactly equal to M when $\theta = \frac{(1+\beta) \cdot M - \beta}{\beta^2}$. M should be less than β and greater than $\beta/(1+\beta)$ to satisfy the condition of $0<\theta<1$.

Similar to the design in Figure 6, process variations of β will result in a modest mirror gain error. The mirror gain error due to β variation is shown in Table 2.

Table 2: Current mirror (Figure 7) gain error due to process variation of β.

β	M	Mirror (Fig. 7) gain Error (%)			
		-20%	+20%	-30%	+30%
15	13	1.76	0.82	3.35	1.05
	9	1.25	0.57	2.39	0.74
	5	0.70	0.32	1.36	0.41
	1	0.56	0.014	0.08	0.02
10	9	2.68	1.29	5.03	1.66
	5	1.56	0.73	2.99	0.93
	1	0.12	0.05	0.25	0.06
5	4	4.57	2.23	8.36	3.04
	3	3.57	1.77	6.62	2.29
	2	2.40	1.14	4.52	1.47
	1	0.80	0.33	1.59	0.42

From Table 2, we can see that, the worst case mirror gain error is 8.36% for $\beta=5$ and M=4. For M=1 and $\beta=5$, the error is 1.59%, which is slightly larger than what was achievable with the previous design.

3.2 Proposed current mirror with multiple outputs

To have multiple outputs, the current mirror shown in Figure 7 can be modified to a mirror with multiple outputs as shown in Figure 8.

If the mirror gain from the input to the outputs is nominally unity, the current mirror gain is given by the expression

$$A = \frac{I_{out1}}{I_{in}} = \frac{I_{out2}}{I_{in}} = \frac{\left[1 + \frac{N+1}{\beta} \cdot \theta + \frac{N+1}{\beta} \cdot \left(\frac{1}{N} - \theta\right) \cdot \frac{1}{(1+\beta)}\right]}{\left[1 + \frac{N+1}{\beta^2}\right]} \qquad (9)$$

where N is the number of outputs of the current mirror.

The mirror current gain exactly equals to 1 if

$$\theta = \frac{N + (N-1) \cdot \beta}{N \cdot \beta^2} \qquad (10)$$

To keep all branch current of emitter of Q5 positive, i.e.,

$$\frac{1}{N} - \theta > 0 \text{ and } \theta > 0 \qquad (11)$$

from (10) and (11), the maximum number of outputs N has to be less than β-1.
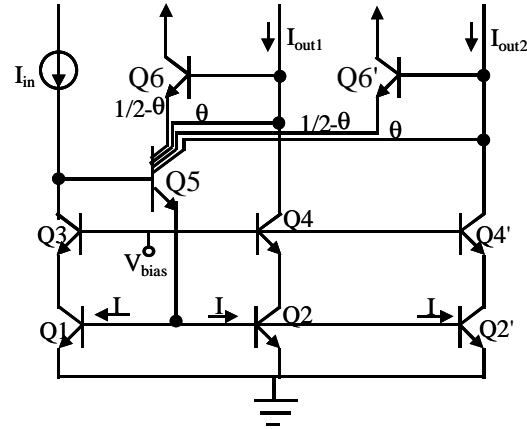

Figure 8. A current mirror with multiple outputs (for N=2, N is the number of outputs)

4. CONCLUSIONS

A new current mirror design based on a split-collector bipolar transistor was introduced that offers significant improvements in mirror gain accuracy over what is achievable with existing approaches in processes with low β transistors and discussed in detail. Extensions of this structure in applications requiring a high output impedance or multiple outputs were discussed. This current mirror is particularly attractive for building current mirrors from lateral transistors in standard bipolar processes but can also be used with parasitic bipolar transistors in standard CMOS process.

5. REFERENCES

[1] David A. Johns, Ken Martin, " Analog integrated circuit design" 1997. P147-148

[2] P.J. Langlois, "Compensation in variable ratio current mirrors " Solid-State Circuits, IEEE Journal of, V32, Issue 10, 1997. p1573 - 1575

[3] J.J. LoCascio, Mesa; R.B, Jarrett; "current mirror circuit", US patent 4297646, Oct. 1981.