GAIN AND BANDWIDTH BOOSTING TECHNIQUES FOR HIGH-SPEED OPERATIONAL AMPLIFIERS

Mezyad M. Amourah and Randall L. Geiger
Dept. of Electrical and Computer Engineering
Iowa State University, Ames, IA, 50011 USA

ABSTRACT

CMOS continuous-time and switched-capacitor filters which operate at high frequencies with high Quality factor Q are difficult to realize. The finite gain and the finite bandwidth of the integrator amplifiers are the main limitation. This paper describes two techniques to simultaneously increase bandwidth, transconductance, and DC-gain of an amplifier without changing the excess bias or the power dissipation. Implementations of a continuous-time band-pass filter to demonstrate the high frequency capabilities of the proposed architectures are described.

1. INTRODUCTION

Accuracy and high speed are often the two most important properties of analog and mixed-signal circuits. A wide variety of analog and mixed signal systems have performance that is limited by the settling behavior of a CMOS operational amplifier (Op-Amp). These include switched-capacitor filters, algorithmic A/D converters, sigma-delta converters, sample and hold circuits, and pipeline A/D converters [1], [2], [3]. The settling behavior of the Op-Amp determines the accuracy and the speed that can be reached. Conventional teachings indicate fast settling requires single pole settling behavior and a high gain-bandwidth product (GBW) [1], [2]. High accuracy also requires a high DC gain. The low values of intrinsic transistor gain achieved by short-channel MOS devices used in high speed amplifiers has made it harder to get a high DC-gain from most existing amplifier architectures. Most filters today are built with transconductance elements and capacitors [2] in integrator-based architectures. Building accurate filters at high frequencies presents several challenges [1], [2]. One major problem is the phase error of the integrators [2,4,5]. The quality factors (Q) of the poles and zeros in the filter are highly sensitive to the phase of the integrator at the pole and zero frequencies. Filter performance is also sensitive to the DC-gain of the integrators. A second challenge is to build an integrator with a sufficiently high DC-gain. These design challenges have been addressed in many publications including [1], [2]. Dynamic biasing of transconductance amplifiers has been proposed [4] as a method for enhancing gain and improving settling. However, in the existing dynamically biased amplifiers, during the last part of settling period the DC gain will be very high but the current will be very low thus settling is slowed. Dynamically biased amplifiers have limited acceptance because of these disadvantages [1], [2]. Moreover, a single-stage dynamically biased amplifier may not provide sufficient gain and cascading them is challenging [4]. Their speed is further limited by the fact that the clock period must be long enough to ensure the transfer of charge is adequately completed in one cycle. Another amplifier design approach proposed for filter applications uses positive-feedback techniques to enhance the amplifier DC-gain without limiting its high frequency performance. This approach was considered by Laber and Gray, Nuata, and others [1], [2]. However, most of the existing positive feedback implementations have suffered from two problems. First is a strong dependence of amplifier gain on transistor matching [1], [3]. Second, the amplifier transfer function will have a denominator of the form of Σg_{x_i} -gy where the g_{x_i} terms are output conductances of transistors and where g_y is the transconductance of a transistor that has it's gate directly connected to the output node of the amplifier. Since wide swing operation is generally required, this connection will make gy a strong function of the output signal level. Therefore, the DC gain of the amplifier will drop sharply as the output node swings up or down. This problem is not mentioned in the literature. The positive feedback gain enhancement method still holds potential for building fast amplifiers with high DC gain which is also suitable for low voltage applications if these limitations can be overcome. In addition to enhancing the amplifier DC gain, we will discuss methods for enhancing amplifier transconductance. In this paper we will discuss two methods that can be used to build amplifiers that have a high DC-gain with enhanced transconductance, without changing the power dissipation and without changing the excess bias at the input nodes. Amplifiers discussed will be applicable to both continuos-time systems and to switched-capacitor systems as well.

2. TRANSCONDUCTANCE, Gm, AND DC-GAIN ENHANCEMENT TECHNIQUES

Amplifier transconductance, Gm, is in general a function of the transconductance of transistors at the input stage. It is well known that the transconductance can be increased either by increasing the biasing current of the input transistors or by increasing the size of the input transistors [5]. It can be shown that both approaches will result in increasing the power dissipation and the parasitic capacitance at the input nodes and limiting the input/output swings of the amplifier. Using the previous methods to increase the transconductance may also result in decreasing the amplifier output impedance this will adversely affect the amplifier performance. In this work we will discuss two methods that can be used to enhance amplifier's transconductance. The first technique, which is applicable to amplifiers without cascoding, depends on connecting the active load transistors to the input signal rather than to a fixed biasing voltage. This connection will require a DC shift for the input voltage to be proper to drive the active load transistor. The DC-shift is easy to implement in the fully differential cases. Finally to eliminate the requirement of a common feedback circuit (CMFB), we use a resistive connection to the supply. This resistive connection will also be used to provide positive feedback, which will result in negative conductance gain enhancement. These techniques allows us to substantially increase the amplifier transconductance, Gm, without increasing the power dissipation, or reducing the excess bias on the input transistors which may limit our input/output swing as we will

show in the filter application. As an example of the first technique, consider the amplifier shown in Fig.1.a, which has a transconductance, Gm, equal to g_{m1}. The amplifier shown in Fig.1.b, though not practical because of biasing challenges (good CMFB circuit required) and common-mode range limitations, is useful for demonstrating the transconductance enhancement concept. This circuit has a transconductance, Gm, of gm1+gm2, which can be much larger than gm1. Since amplifier gain bandwidth product, and DC gain are proportional The amplifier of Fig.1.b has a larger DC- gain and a larger unity gain frequency than the circuit of Fig1a but both amplifiers have the same power dissipation. Note that transistor M2 serving as a biasing transistor in the circuit of Fig.1a, but serves additionally as an amplifier in the circuit of Fig.1.b. Modifications of the circuit of Fig.2.b that address the problems identified above will now be considered. [5].

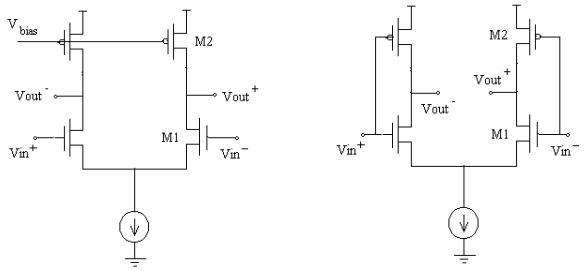

Figure 1 differential pair OTA a. basic, b. enhanced Gm

Modifications on Fig.1b are shown in Fig. 2. These amplifiers do not require a CMFB circuit for biasing. The amplifiers in Fig. 2.a and Fig. 2c have a limited output swing compared to amplifiers in Fig. 2.b and Fig. 2.d and they have an enhanced transconductance of Gm≈2g_{m1}. The amplifiers shown in Fig. 2c and Fig. 2d have positive feedback for negative conductance gain enhancement. Concentrating on amplifier 2.d. it has a very high unity gain frequency as will be shown in the next section. However, it has a disadvantage of nonlinear distortion over a wide swing operation, because the resistance of transistor M3 is directly affected by the output voltage-level. Moreover, the positive feedback is not controllable. Amplifier of Figure 2.d can show a DC gain of more than 60dB which makes it suitable for filter applications where very high speed operation with low power dissipation are the key features. The drawback of this technique is the big increase of the amplifier input-capacitance, which reduces the effective speed enhancement. The second technique is applicable on second order amplifiers. In our implementation we targeted amplifiers that have two poles, one of them is dominant with one level of cascoding. The basic idea is shown in Fig3, transistor M1 in the cascode is to be used as an amplifier. The current of value K2•Vin is a feedback taken from the node of the secondary pole. Amplifier shown in Fig4.a with assumptions shown below has a transconductance of the form

$$G_m = \frac{g_{m1} g_R K1 + (g_{m1} + g_{o1}) K2}{g_{m1} + g_R + g_{o1}} \approx 2 g_{\min} \ , \qquad (1)$$

assuming that $K2 \propto g_{\min}; K1 \propto \frac{g_{\min}}{g_R}; g_{m1} \approx g_{m6} \approx g_{\min}$

The realization of this concept is done in a way such that the feed-back tail-current has a value that is dependent on the output voltage level, Vout. This term is necessary to get the desired positive feedback property. Examples of implementation of this technique on folded cascode and telescopic amplifiers are shown in Figure4.a, 4.b. for the rest of this paper, we will concentrate on amplifier of Figure4.a. Small signal analysis of shows that the proposed amplifier has a transconductance, Gm, of the form

$$G_m = \left\{ \frac{2\left[\begin{array}{c} g_{m6} g_{m3} (g_{o1} + g_{o2} + g_{o4}) + g_{m6} g_{m4} (g_{o1} + g_{o2} + g_{o3}) \\ + g_{m1} g_{m3} (g_{o4} + g_{o5} + g_{o6}) + g_{m1} g_{m4} (g_{o3} + g_{o5} + g_{o6}) \end{array}\right]}{[g_{m3} (g_{o4} + g_{o5} + g_{o6}) + g_{m4} (g_{o1} + g_{o2} + g_{o3})]} \right\} \qquad (2)$$

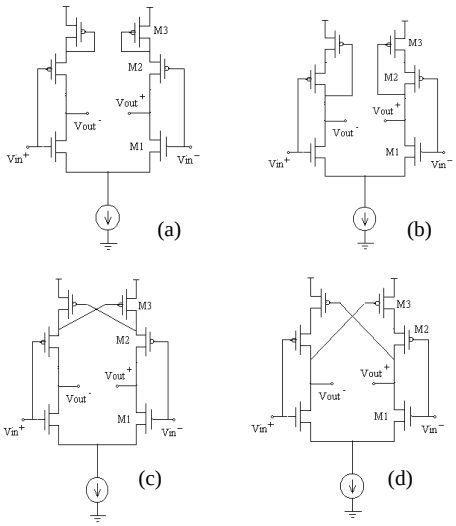

Figure 2 Modifications on Fig.1.b, No CMFB required, a, b have negative feedback, and c, d with positive feedback.

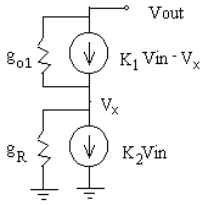

Figure 3. Model for Technique 2.

This Equation shows that amplifier Gm is in the range of 2(2gm1+2gm6). While the regular folded cascode has a Gm value of gm1. But, note that biasing currents are different. Comparison between the two architectures-transconductances shows that we have an enhancement factor in the range of 2 to 2.66 times Gm of the folded cascode. Moreover, estimating the DC-gain, Av, results in;

$$A_v = \left\{ \frac{\left[\begin{array}{c} (g_{m3} + g_{m4})[g_{m6} (g_{o1} + g_{o2}) + g_{m1} (g_{o5} + g_{o6})] \\ + (g_{m1} + g_{m6})(g_{m3} g_{o4} + g_{m4} g_{o3}) \end{array}\right]}{[(g_{o1} + g_{o2} - g_{o5} - g_{o6})(g_{m3} g_{o4} - g_{m4} g_{o3})]} \right\}, \qquad (3)$$

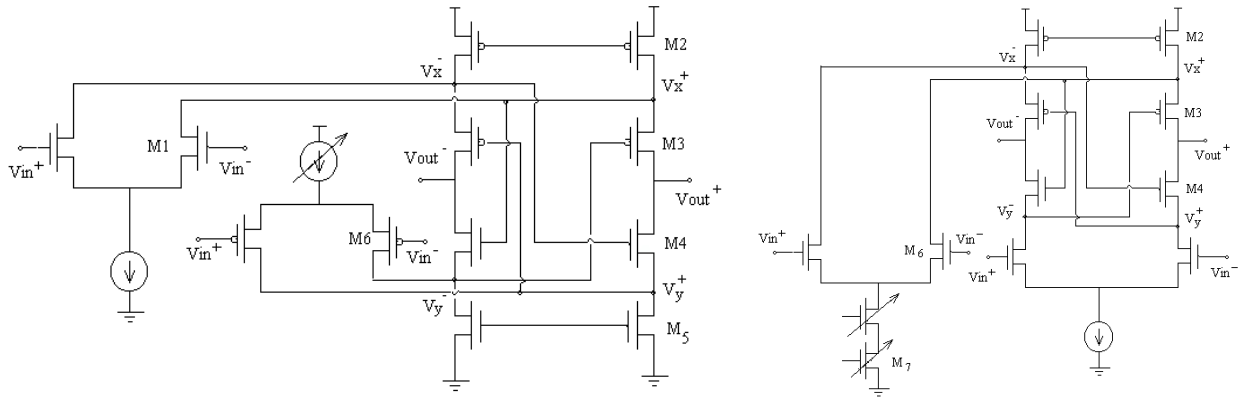

Fig. 4. Second Gm enhancement technique with positive-feedback applied to a. folded cascode, b. telescopic amplifiers.

Equation (3) shows that the proposed amplifier exhibits a positive feedback property. In our design we concentrated on getting our high gain by making the term, go5+go6, very close to the term, go1+go2. Looking at Figure.4.a we see that by controlling the current source we are controlling both go5, and go6. This option allows us to control the amplifier gain, not become totally depending on the transistor matching issue. Biasing amplifiers shown in Figure 4.a, and Fig.4.b requires a replica biasing scheme if we want to make sure that a very high DC-gain is to maintained always. Finally the main drawback of amplifiers in Figure 4 are the increased input capacitance of the amplifier, and the requirement of a replica biasing circuit. The output parasitic capacitance of the proposed amplifier in Figure 4.a is lower than that of the regular folded by a factor of one third approximately, due to smaller biasing currents flowing through transistors M3, and M4. In the next section we describe simulation results of the proposed amplifiers, also we show an application of the amplifiers shown in Figure 2.d, and Figure 4.a in a continuos time bandpass filter.

3.SIMULATION RESULTS

The amplifier shown in Figure 2.d has been simulated using TSMC 0.25u process. The amplifier has a total current of 340uA. For a load capacitor of 0.5pF, and power supply of 2.5 Voltts, the amplifier can achive a DC gain of 66dB, unity gain frequency of 842MHz with a phase margin of 87 degrees. The AC analysis result is shown in Figure 5. The modified folded amplifier of the second technique with the positive feed-back is simulated using CMOS TSMC 0.25u process. The amplifier has a total current of 1.2mA, capacitve load of 500fF, and power supply of 2.5V. Simulation shows that the amplifier has a DC gain of 107.3dB with a unity gain frequency of 805MHz. A comparison between the modefied and the traditional folded cascoded is shown in table1 where both amplifiers have approximately the same power dissipation, the same excess bias on the similar transistors, and the same load capacitance. The table shows that for the same conditions we where able to enhance both, the unity gain frequency from 433.5MHz to 805MHz, and the DC-gain from 47.23dB to 107.3dB, for the same load, and approximately the same phase margin. Results are shown in Figures 6.a and 6.b. The proposed amplifier architectures have been implemented in a continuos time 4th order Butter-worth band-pass filter. The filter is constructed by cascading two Gm-C biquads, as shown in

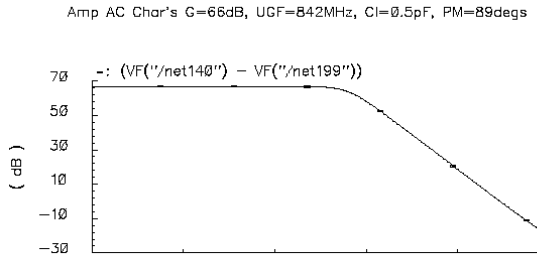

Fig.5 AC Char's of the amplifier shown in Figure 2.d.

The only difference between the two biquads is the values of the damping transconductor. the filter has a transfer function, center frequency, and bandwidth given by the following relationships.

$$\frac{Vod}{Vid} = \frac{g_{1d}\, sC_2}{s^2 C_1 C_2 + sC_2 g_{2d} + g_{1d}^2} = \frac{\frac{g_{1d}\, s}{C_1}}{s^2 + s\frac{g_{2d}}{C_1} + \frac{g_{1d}^2}{C_1 C_2}} \qquad (4)$$

$$w_0 = \frac{g_{1d}}{\sqrt{C_1 C_2}} \quad ; \quad BW = \frac{g_{2d}}{C_1} \qquad (5)$$

Table1
Comparison of Amplifier Characteristics w/wo Gm enhancement Tech.

Folded cascoded	Gm-Enhanced	Traditional
DC-gain	107.3 dB	47.23dB
Unity gain freq.	805MHz	433.5MHz
Load cap.	500fF	500fF
Phase margin	75 degrees	78.6 degrees
Total current	1.2mA	1.2mA
Supply voltage	2.5V	2.5V

The transconductance amplifier, of Figure 2.d, implemented in the filter has a total current of 4mA, Capacitors have sizes, Cl=1.2pF, C1=1pF. Simulation results are shown in Figure 8.a,b. As shown in Figure 8.a. Simulation results show that, the filter has a center frequency of 1.047GHz, and a bandwidth of 380MHz. Transient simulation shows that the filter can achieve a 360mV pk-pk output swing. Discrete Fourier analysis shows that at the maximum swing the total harmonic distortion is –30dB.

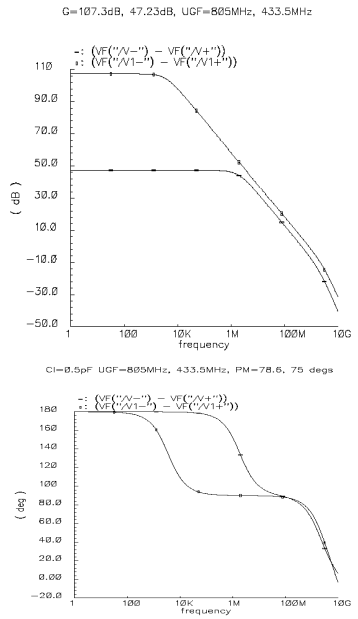

Figure. 6.a,b AC Char's of the folded cascode, and the Enhanced Gm OTA.

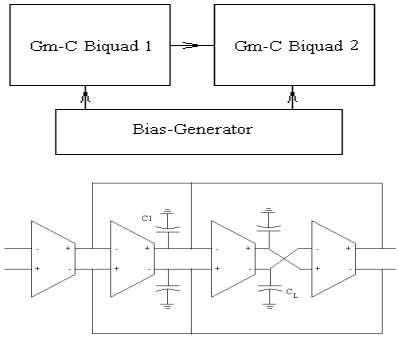

Figure 7.a,b The 4th order Band-pass filter.

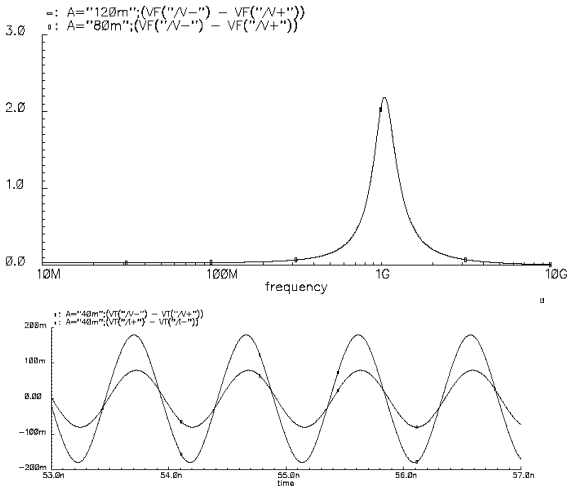

Figure 8.a, b (a) Filter characteristics, using OTA of Fig.2.d, magnitude and phase, (b)input waveform at 1.047GHz

The same filter architecture is implemented using the OTA shown in Figure 4.a, with a total current of 4.0mA. Capacitors have sizes, Cl=1.2pF, C1=0.6pF. Simulation results are shown in Figure 9.a,b. Simulation results show that, the filter has a center frequency of 1.216GHz, and a bandwidth of 250MHz. Transient simulation, shows that the filter can achieve a 300mV pk-pk output swing. Discrete Fourier analysis shows that at the maximum swing the total harmonic distortion is –32.6dB.

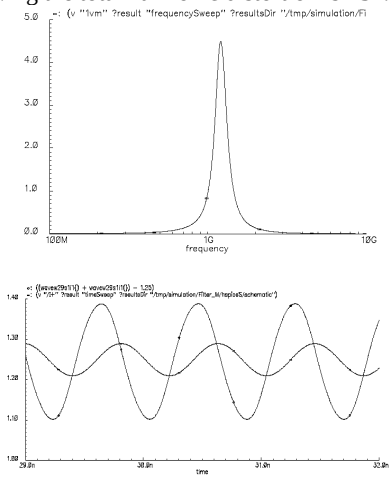

Fig.9.a, b, (a) Filter Characteristics, using OTA of Fig.4.a magnitude and phase, (b) input and output waveforms at 1.216GHz

4. CONCLUSIONS

Two techniques to enhance amplifier transconducatance in addition to Positive-feedback have been proposed to build high speed, and very high DC-gain amplifiers. The second technique shows implementation of the positive feedback technique in a manner where the gain is controllable, and the gain is not a strong function of the output voltage swing. The extra price paid was the increase of the amplifier input-capacitance. The extra price paid for the positive feedback in the second technique was the need of a replica-biasing scheme to control amplifier gain.

6. REFERENCES

[1] C. Laber, and P. Gray, "A Positive-Feedback Transconductance Amplifier with Applications to High Frequency, High-Q CMOS Switched-Capacitor Filters", *IEEE J. Solid-State Circuits*, vol. 23, no. 6, Dec. 1988, pp1370-1378.

[2] B. Nauta, "A CMOS Transconductance-C Filter Technique for Very High Frequencies", *IEEE J. Solid-State Circuits*, vol. 27, no. 2, Feb. 1992, pp142-153.

[3] D. Allstot, "A Precision Variable Supply CMOS Comparator", *IEEE J. Solid-State Circuits*, SC-17, no. 6, 1982, pp1080-1087.

[4] B. Hosticka, " Dynamic CMOS Amplifiers ", *IEEE J. Solid-State Circuits*, vol. SC-15, no. 5, Oct. 1980, pp887-894.

[5] D. Johns, and K. Martin, Analog Integrated Circuit Design, Chap16, John Wiley, and Sons, Inc.

[6] B. Kamath, R. Meyer, and P. Gray, "Relationship Between Frequency Response and Settling Time of Operational Amplifiers", *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, Dec. 1974, pp347-352.