A HIGH GAIN STRATEGY WITH POSITIVE-FEEDBACK GAIN ENHANCEMENT TECHNIQUE

Mezyad M. Amourah and Randall L. Geiger Dept. of Electrical and Computer Engineering Iowa State University, Ames, IA, 50011 USA

ABSTRACT

Several new CMOS very high DC-gain amplifiers that use internal positive-feedback techniques are presented. These amplifiers have a controllable gain and don't require perfect matching of transistors to achieve the high DC gain. An implementation of a sample and hold circuit constructed using one of the proposed amplifiers is described. Simulation results predict a DC gain larger than 100dB is possible without limiting the speed of the amplifier.

1. INTRODUCTION

High gain and high speed are two most important properties of analog circuits. Many different analog and mixed signal components and systems have performance that is limited by the settling behavior of a CMOS amplifier. These include switched capacitor filters, algorithmic A/D converters, sigma-delta converters, sample and hold circuits, and pipe-lined A/D converters [1], [2], [3]. In these circuits the settling behavior of the Op-Amp determines the accuracy and the speed that can be reached. Conventional wisdom also teaches that fast settling requires single pole settling behavior and a high gain-bandwidthproduct [1], [2] or equivalently a high unity-gain frequency. Correspondingly, high accuracy requires a high DC gain. Conventional wisdom also teaches that the high unity gain frequency calls for a single stage design with short channel devices biased at high current levels [2], [4]. The high DC gain can be achieved with one or more of the following techniques. Cascading of gain stages, Dynamic biasing or output impedance gain enhancement. Cascading two or more stages will result in a very high DC gain but the required frequency compensation will seriously limit the high frequency performance [1], [2]. Dynamic biasing was reported to combine a high DC gain with fast settling speed [4]. However, in the reported dynamically biased amplifiers, the settling is slowed when the DC gain becomes large. Dynamically biased amplifiers have found limited acceptance because of this disadvantage [1], [2]. Moreover, a single stage dynamically biased amplifier may still not provide sufficient gain, and cascading dynamically biased amplifiers is difficult [4]. Output impedance enhancement is typically achieved cascoding (stacking transistors at the output node) using gain-boosting techniques or by adding a negative conductance, generated with a positive feedback structure. Cascoding is a wellknown and widely used method of enhancing the amplifier output impedance, with cascading, the amplifier output impedance, and correspondingly the dc gain of single stage amplifiers, becomes proportional to the square, or to the cube of the intrinsic transistor gain, gm/go. Unfortunately, one level of cascoding doesn't provide sufficient DC-gain in many applications. Double or triple cascoded amplifiers do have a large DC gain but correspondingly, they have a very limited output swing, and are not applicable to low-voltage circuits. Moreover as we go deep in

sub-micron processes, the intrinsic transistor resistance becomes smaller and smaller which limits the advantages of cascoding. Enhancing amplifier gain by gain-boosting which is actually an extension of the single -level cascading, is one of the most successful ways of boosting amplifier gain without limiting the high frequency performance [2]. However, gain-boosting technique needs at least one level of cascoding, which makes it less favorable for low voltage applications. Moreover, boosting amplifiers add their own poles and zeros to the final amplifier which generally exhibits zero-pole doublets that affect amplifier settling and which can make it slow when accurate. The negative conductance compensation with positive feedback conceptually offers potential for obtaining a very high DC gain, ideally an infinite gain, without degrading the high frequency performance. However most of the positive feedback implementations have suffered from two problems. First is a very strong dependence of the amplifier gain on transistor matching [1],[2],[3] and on maintaining a specific relationship between distinct process parameters. Second, the amplifier transfer function will have a denominator of the form of $\Sigma g_x - g_y$, where the g_x terms are

output conductances of transistors and where g_y is the transconductance of a transistor that has it's gate directly connected to the output node of the amplifier. Since we are

looking for wide swing operation, this connection will make g $_{y}$

a strong function of the output signal. It can be shown that the wide swing on the gate voltage of the feedback element will cause the magnitude of The DC gain of the amplifier to drop sharply as the output node swings up or down. Although this problem is not mentioned in the literature it is a second major obstacle that limits the practical utilization of existing negative conductance amplifier. However, since the other gain enhancement techniques face fundamental limitations in low voltage processes, the positive feedback method still holds potential for building fast amplifiers with high DC gain suitable for low voltage applications if the limitations identified can be overcome. This work focuses on overcoming these limitations.

2. BACKGROUND OF POSITIVE FEEDBACK SCHEMES.

The concept of applying a positive feedback to generate a compensating negative conductance for the purpose of enhancing the amplifier gain has been discussed in several publications. Most of the proposed structures share the common characteristic of generating a negative resistance by feedback from the output node that is used to compensate some positive resistance at the output to achieve the very high DC gain. The simple example proposed by Allstot [3]. Will be used to illustrate the concept. In this implementation cross-coupled active-load PMOS transistors are applied to a simple differential pair as

shown in figure 1. The negative conductance, $-g_{m3}$, generated by the cross coupling used to boost the DC gain. The small signal model of this amplifier is shown in figure 2. The small signal analysis shows that the DC gain of the amplifier can be written as $A = \frac{-g_{m1}}{g_{m1}}, \qquad (1)$

$$A_{v} = \frac{-g_{m1}}{g_{o1} + g_{o2} + g_{o3} + g_{m2} - g_{m3}} \quad , \tag{1}$$

If $g_{m3} = g_{o1} + g_{o2} + g_{o3} + g_{m2}$ then the amplifier will exhibit an infinite DC gain. Note that no additional nodes and consequently no additional poles are added with this negative conductance gain enhancement scheme. However to get the very high DC gain we need almost perfect matching mainly between g_{m3} and the sum

of $g_{o1}+g_{o2}+g_{o3}+g_{m2}$. The matching requirement can be relaxed by two methods. First, make one of the important parameters programmable. Second, use some kind of cascoding so that the amplifier DC gain is not completely dependent on the close matching requirement. Even with a relaxation in the matching requirements, a major problem still exists; transconductance of M1,2, and conductance of M1,2,3 are output level dependent. For example consider the use of this amplifier in the implementation of a sample and hold circuit that requires an output swing of 1Vp-p. If the amplifier is fully differential,



Figure 1 Regular Differential pair with positive feedback.



Figure 2. Small signal model for amplifier in Fig.1.

then the output-node voltage level will exhibit a change in value by ± 250 mV will dramatically reduce amplifier gain while settling. Almost all previously proposed negative conductance gain enhancement architectures have this property. Finally a potential problem mentioned by Labor and Gray [1] is that the dominant pole of the amplifier may move from left-half plane to right-half plane if the parameter behind the minus sign becomes larger than the term before due to temperature or process variations. The amplifier will, however, provide stable closed loop operation if sufficient negative feedback is provided by the external circuit [1]. Several new negative conductance gain enhancement structures that overcome most of the limitations identified in existing structures are introduced in the following section. These structures are second order amplifiers containing one dominant pole. The proposed amplifiers will continue to exhibit single pole settling behavior with a DC gain of greater than 100dB throughout a large input and output voltage swings.

3. CONCEPTUAL DESCRIPTION OF THE PROPOSED POSITIVE FEEDBACK SCHEME

The proposed amplifiers are realized by applying positivefeedback to several standard cascoded amplifiers. By applying a programmable positive feedback in combination with cascoding the transistor matching requirements are relaxed. . A key feature of the new amplifiers is based upon where the positive feedback signal is sensed. Instead of sensing at the output-node which inherently has a large voltage swing, the positive feedback signal used to enhance the DC-gain is derived from the extra nodes created by cascoding. This will considerably reduce the effect of the output voltage level on the amplifier gain. Figures 3.a, and 3.b show the application of the programmable transconductance cross-coupled transistors to traditional folded cascoded, and telescopic amplifiers. Fig.3.c, and Fig.3.d show the possibility of realizing high DC gain amplifiers for moderate and low output impedance with the rail to rail option as shown in Fig.3.d. All of the amplifiers presented here are fully differential. Common mode feed back circuits, and biasing circuits are not shown for simplicity. Single ended versions of those amplifiers are easy to obtain. We will concentrate on the amplifier shown in Fig. 3.a. The other amplifiers shown exhibit the same fundamental properties. The gain of the amplifier shown in Fig.3.a is programmed using replica-biasing scheme. Ignoring the bulk effect for simplicity, the amplifier shown in figure3.a has a small signal equivalent circuit shown in figure 4 this structure has an open-loop gain, Av, given by the form

$$A_{v} = \frac{-g_{m1}}{\left(\frac{g_{o3}(g_{o1} + g_{o2} + g_{o6} - g_{m6})}{g_{m3}} + \frac{g_{o4}g_{o5}}{g_{m4}}\right)},$$
(2)

Assuming that gm3=gm4, g03=go4, and go6<<go1,2 the voltage gain can be written as

$$A_{v} = \frac{-g_{m1} \cdot g_{m3}}{g_{o3}(g_{o1} + g_{o2} + g_{o5} - g_{m6})},$$
(3)

Equation (3) shows that the DC-gain of the amplifier can be infinite as gm6 approaches go1+go2+go5. Note that gm6 is fully programmable with the tail current IADJ which provides for compensation of process and temperature variations. Alternatively, the bias output conductance parameters can be adjusted by programming the current IB and/or the quiescent current in the cascaded transistors. The voltages Vx+ and Vxexperience very small swings compared to Vout+ and Voutsince Vx=Vout/(gm3/go3). For example in our design the intrinsic transistor gain of M3 is slightly larger than twenty five. So if the output voltage have a swing of one volt. Vout=Vcm± 250mV. then voltage Vx experience a swing that can be written as Vx=Vcm±10mV. From this example it is apparent that gm6 is not a strong function of the output voltage level. The amplifier shown in figure 3.c can be used where а



Figure 3 different implementations of the proposed positive feedback tech., a) folded cascode, b) telescopic cascode, c) low output impedance, and d) rail to rail implementation.



Figure 4 small signal model of half circuit of Fig.3.a

moderate gain is required with moderate to low output impedance. The low output impedance results in a very high bandwidth. Under the approximation of go<<gm, The voltage gain, can be written as

$$A_{\nu} = \frac{-g_{m1} \cdot g_{m2}}{g_{m3}(g_{m2} - g_{m6})} \quad , \tag{4}$$

again as gm6 approaches gm2, the amplifier will exhibit very high DC gain while maintaining low output impedance of approximately 1/gm3. Note that gm4 is fully programmable with the tail current IADJ although the tail current IB could alternately be used to adjust gm2 or both currents could be adjusted simultaneously to control both gm2 and gm6. If the output impedance is very low then the amplifier will have a limited output swing. The amplifier of Fig. 3d has a reasonably low output impedance and rail to rail swings on both the input and output while still having the negative conductance gain enhancement property as evidenced by the presence of transistors M6 and M7.

4. SIMULATION RESULTS

An amplifier using the folded cascoded architecture of figure 3.a was designed in the TSMC 0.25u CMOS process and simulated in HSPICE using the BISM3 device models. The amplifier consumes a total current of 800uAat a supply voltage of 2.5V, and was designed for driving a capacitive load of 0.5pF. Simulation shows that the amplifier has a DC gain of 103.6dB with a unity gain frequency of 278MHz. A comparison between the performance of the modified and the traditional folded amplifiers is shown in Table 1 where both amplifiers have approximately the same power dissipation, the same excess bias on the similar transistors, and the same load capacitance. The table shows that for approximately the same conditions we can enhance the DC-gain from 46dB to 103dB, for the same load and the same phase margin. The magnitude and phase plots for the conventional cascode amplifier and the negative conductance gain boosted amplifier are compared in Fig. 5. The same amplifier architecture was applied to a switched capacitor sample and hold circuit with two non over-lapping clocks at a frequency of 50MHz with 1nsec separation between the two nonoverlapping phases. The circuit is shown in Figure 6. The amplifier consumes a total current of 3.6mA, and each output drives an external load capacitance of 1pF. The sampling capacitors were sized to be 550fF. Simulation results are shown in Figure 7. Simulation shows that the amplifier was able to slew and settle to an error of less than 0.23mV for a 1V peak-to-peak output swing within 3nsec, which is equivalent to 11-bits of accuracy. Finally, the amplifier shown in Figure 3.c was designed to operate with total current of 450uA and output impedance of $2K\Omega$ for a supply voltage of 2.5V. Capacitive loads of 100fF and 500fF were driven. Simulation results show a DC-gain of 76.3dB and a unity gain frequency of 2GHz for the 100fF-load capacitance. For the 500fF load-capacitance the unity gain frequency is reduced to 870MHz with 67 degrees of phase margin. Simulation results are shown in Figure 8.

Table 1 Comparison of Amp Characteristics w/wo positive feedback

Folded cascoded	Positive feedback	Traditional
DC-gain	103.7 dB	46dB
Unity gain freq.	278MHz	288MHz
Load cap.	500fF	500fF
Phase margin	82.5 degrees	81.7 degrees
Total current	0.8mA	0.8mA
Supply voltage	2.5V	2.5V









100fF load capacitance. For the 500fF load-capacitance the unity gain frequency is reduced to 870MHz with 67 degrees of phase margin. Simulation result is shown in figure 8.



Figure 7. a,b S&H differential output. Hold starts at 50nS.



Open loop Char's Av=76.3dB "6.566K" CI=500fF PM=67degs with UGF=870MHz, Pd=11mW

Figure 8 AC gain, UGF of Fig.3.c with Cl=0.5pF

5. CONCLUSION

A positive-feedback negative conductance gain enhancement technique was used to boost the DC-gain of several second-order amplifiers without sacrificing the high frequency performance. The implementation was done such that the gain is controllable and not substantially affected by the output voltage swing. The proposed positive feedback technique is applicable to lowvoltage and low output impedance circuits, using this technique it is possible to increase the DC gain by more than 50dB.

6. REFERENCES

[1] C Laber, and P. Gray, "A Positive-Feedback Transconductance Amplifier with Applications to High-Frequency, High-Q CMOS Switched-Capacitor Filters", IEEE J. Solid-State Circuits, vol. 23, no. 6, Dec. 1988, pp1370-1378.

[2] K. Bult, and G. Geelen, "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain", IEEE J. Solid-State Circuits, vol. 25, no. 6, Dec. 1990, pp1379-1384.

[3] D.Allstot, "A Precision Variable Supply CMOS Comparator", IEEE J. Solid-State Circuits, SC-17, no. 6, 1982, pp1080-1087.

[4] B. Hosticka, " Dynamic CMOS Amplifiers ", IEEE J. Solid-State Circuits, vol. SC-15, no. 5, Oct. 1980, pp887-894.