MOSGRAD - A Tool for Simulating the Effects of Systematic and Random Channel Parameter Variations

Mao-Feng Lan and Randall Geiger

Department of Electrical and Computer Engineering
Iowa State University, Ames, IA 50011, U.S.A.
Email: rlgeiger@iastate.edu

ABSTRACT

A CAD tool, MOSGRAD, that can be used to simulate the effects of distributed two-dimensional systematic and random variations in device parameters on the performance of matching-critical circuits has been developed. In addition to applications for layouts with conventional rectangular transistors, this tool can predict the performance of non-conventional circuit structures in which multiple drain and/or source regions share a common channel region as well as predict the performance of non-conventional layouts that may incorporate nonrectangular transistors or segmented transistors.

1. INTRODUCTION

Iteration with device sizes and layout styles at the silicon level can provide the insight needed to improve circuit performance in the presence of random and systematic parameter variations but such an approach will not yield optimal designs and is both costly and time consuming. The seemingly simple problem of predicting the effects of systematic and random parameter variations on a MOS transistor is complicated by the unavailability of a suitable simulator and by some inconsistencies in models that have been presented in the literature [1]. Existing models and simulators provide little insight into how to change either the size or layout to improve performance. The major reason existing simulators can not be used is that there is no mechanism for incorporating either systematic or random channel variations in lateral directions of device or process parameters and it is these lateral variations that play a key role in the performance of high-end matching-critical circuits. Although process simulators are an appropriate tool for simulating the effects of parameter gradients, existing process simulators are limited to two dimensional modeling and only one of these dimensions is lateral.

In this paper, the CAD tool MOSGRAD is introduced. MOSGRAD can be used to simulate the effects of lateral parameter variations of MOS transistors on layouts of matching-critical circuits. Applications of MOSGRAD on predicting the effects of systematic and random parameter variations on the performance of current mirrors are discussed.

2. EXISTING APPROACH ON VARIATION MODELING

Lateral variations of a model parameter γ can be expressed as

$$g(x,y) = g_{NOM} + g_{PROC} + g_{WAFER} + g_{DIE} + g_{SYS}(x,y) + g_{RAN}(x,y) \quad (1)$$

where x and y represent the position on the die. In (1), γ_{NOM} is the nominal value of the model parameter and the five remaining terms are themselves random variables that some authors choose to combine together into a single random variable. The variable γ_{PROC} characterizes the variation from one lot of wafers to another. The parameter γ_{WAFER} characterizes the variation from one wafer to another wafer in a "lot" of wafers and the parameter, γ_{DIE}, characterizes the variation from die location to die location. The parameter γ_{SYS} characterizes the systematic variation from one location to another on the die and is position dependent. The variable γ_{RAN} characterizes the random part at the position (x,y). When considering devices in close proximity to each other on a die, the values of the random variables γ_{PROC}, γ_{WAFER} and γ_{DIE} are nearly constant throughout the region. Thus, almost all the matching-related researches focus only on the effects of the two rightmost terms, γ_{SYS} and γ_{RAN}, in (1).

Implicit in the functional form of (1) is the distributed nature of the model parameter. Essentially all device models and, in particular, the device models used in Spice-type simulators are based upon lumped parameter models. In most works, it is assumed that the actual values of the lumped model parameters can be obtained by integrating the position-dependent distributed model parameters over the area of the channel region of the device as given by the equation

$$\gamma(x_A, y_A) = \frac{1}{\text{Area}} \iint_{\text{Area}} \gamma(x, y)\,dxdy \quad (2)$$

where (x_A,y_A) is a point representing the location of the device on the die [2][3][4]. Although not critical in what follows, it is convenient to define (x_A,y_A) to be the geometrical centroid of the device. We will refer to this lumped parameter extraction from a distributed parameter domain as the integral model throughout this paper. Unfortunately, discrepancies and limitations with mismatch performance based upon the integral model have been reported [1][5][6]. Recently a new approach to improve the modeling of mismatch was proposed [6], however the new approach is still based on the integral model and thus the inherent limitations [1][5] of the integral model are still present in the new approach. Since both systematic effects and random fluctuations in device parameters play key roles in matching performance, it is particularly important that any accurate mismatch model should effectively incorporate these effects. It can be shown that central to the problem of predicting the effects of lateral parameter variations on rectangular transistors is the need to develop a distributed MOS transistor model. Even for rectangular transistors, it does not appear that a simple lumped parameter model extension of existing device models that accurately predicts the port I/V characteristics can be derived and the problem becomes even more challenging when the issue of modeling the mismatch performance of non-rectangular devices [7]. In this work, a finite-element approach will be introduced for predicting the mismatch performance of matching-critical circuits.

3. PROPOSED APPROACH

In this approach, the distributed channel region of a MOS transistor is modeled by an assemblage of a finite number of

lumped-element unit cells. Each cell has four edge-centered nodes that are connected to corresponding edge-centered nodes in adjacent cells as depicted in Fig. 1. If the cell is assumed to be of length ΔL and width ΔW, the size of transistors MC1 and MC2 will be ΔW/(ΔL/2) and the size of MC3 and MC4 will be ΔL/(ΔW/2). The four transistors in each unit cell have a common gate terminal. With this finite lumped-element approach, systematic variations in process or device parameters of any magnitude and at any angle relative to the cell can be readily simulated using a conventional SPICE-type simulator. Arbitrary systematic parameter variations and random parameter variations can also be accommodated. Although random mismatch is theoretically amenable to this same finite-element approach, the simulation time and memory requirements are substantial in practical layouts. An alternative method for predicting the effects of random parameter variations on mismatch that is still based on the finite-element approach is included in MOSGRAD [9].

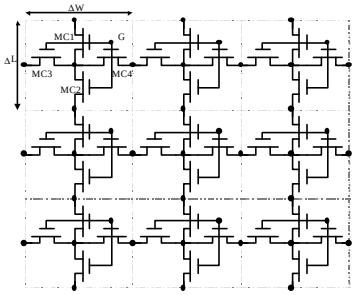

Fig. 1

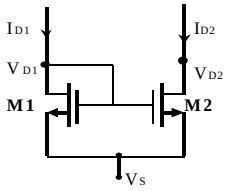

Fig. 2

Fig. 1 Finite lumped-element model of 4-transistor cells
Fig. 2. Basic Current Mirror Circuit

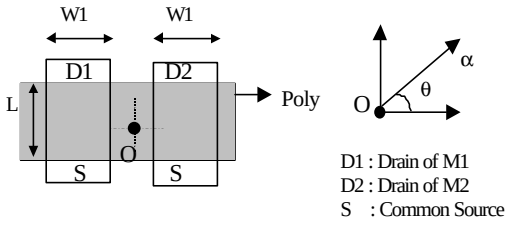

Fig. 3 Simple Current Mirror Layout

As a front end to the tool, a graphical user interface is incorporated in which the user graphically enters the circuit structure that is to be simulated. In MOSGRAD, he graphical user interface is written for convenience in MATLAB. The output of the graphical interface is a file describing the device shape and this file is sent to a Netlist-Generator. The main function of the Netlist-Generator is to incorporate systematic parameter variations in the netlist. The output from the Netlist-Generator is passed to a conventional Spice-type simulator to simulate the performance of the circuit. Although the tool was established for predicting circuit performance under linear gradients, arbitrary gradients in process parameters can also be simulated. The graphical interface with MATLAB allows users to describe arbitrary layouts of current mirrors comprised of arbitrarily shaped transistors. Thus this tool can be readily used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in either threshold voltage or mobility and can be extended to predict the performance characteristics of differential amplifiers in the presence of gradients.

4. SIMULATION AND EXPERIMENTAL RESULTS ON SYSTEMATIC VARIATION

A basic current mirror is depicted in Fig. 2. The input port is at the drain of transistor M1, the output is at the drain of transistor M2 and the sources are common. A simple layout of the basic current mirror is shown in Fig. 3. In Fig. 3, α represents the magnitude of a parameter gradient and θ the angle of a parameter gradient. The contact labeled as "D1" represents the drain contact of M1 and the contact labeled as "D2" represents the drain contacts of M2. The mismatch of drain current is defined as $(I_{D2}-I_{D1})/I_{D1}$ when $V_{D1}=V_{D2}$.

A test chip designed to verify the validity of the gradient matching prediction in MOSGRAD is shown in Fig. 4. The test circuit on this chip was a single simple current mirror using the simple layout of Fig. 3. The width and length of both transistors were nominally identical (W1=L=32μm) and the spacing between the two transistors was 4μm. This chip has been fabricated in a 2μm CMOS n-well process available through MOSIS. In the test structure, the V_T gradient was controlled via the back bias on the transistors. P-channel transistors were placed in a large circular n-well. Multiple periphery contacts where placed around the entire periphery of this n-well region. Currents were then introduced at a predetermined angle by selecting the appropriate diagonally opposing well contacts. These currents introduced a gradient voltage in the well which correspondingly induced a gradient in the threshold voltage of the test transistors.

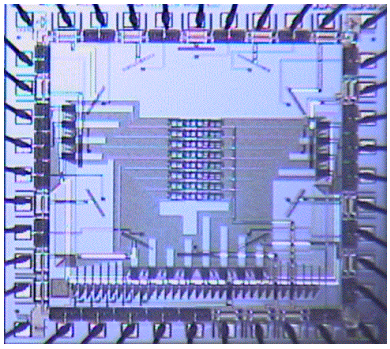

Fig. 4 Testing chip of simple structure

The test results of the simple structure, are shown in Fig. 5 From this figure, it t is apparent that there is an offset existing because of the native systematic and random variations. If the simulator outputs obtained under the assumption of no native gradients are shifted by the measured offset, it can be seen that there is a good agreement between the measured and simulated results. The peak-to-peak variation of the measured result is about 1.55% and the peak-to-peak variation of the simulation was about 1.56%. The upward shift is about 0.5% for the test structure compared to that of the simulation. In this test, a 1.189mv/u gradient in the substrate was applied at the location of the testing device and it created a threshold voltage gradient of approximately 0.322mV/μm.

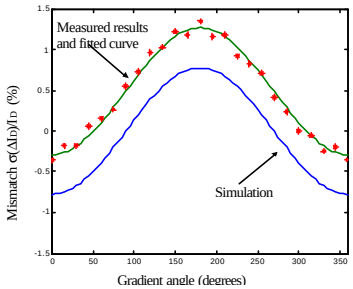

Fig. 5 experimental and simulation results

5. SIMULATION ON RANDOM MISMATCH

It is widely accepted that the variance of the random mismatch in model parameters is inversely proportional to the active areas of the transistors and this will be referred as the law of area [2]. With this approach, the random mismatch of a model parameter can be expressed as

$$s^2(g) = \frac{A_g^2}{\text{Area}} \qquad (3)$$

where γ is a model parameter and A_γ is the area proportionality constant. When $\sigma(\gamma)$ is plotted as a function of $1/\sqrt{Area}$, A_γ is equal to the slope. At this point, we have to notice that the information about $\sigma(\gamma)$ is extracted from the measured I/V characteristics based upon the lumped model with the integral approach and thus there is a discrepancy existing between the inherent area proportionality constant $\tilde{A}_g$ and extracted A_γ. In fact, $\tilde{A}_g$ is theoretically a constant for the same process no matter what the shape of a device. However, a current report [8] showed that there was a significant difference among A_γ's with different shapes, although the authors of the paper [8] declaimed that these A_γs' difference was not significant. In this section, we will discuss how to predict the random current variation for a current mirror, in particular, with non-conventional shaped devices.

In [9], it was shown that with the same V_T variation, current variation, $\sigma^2(\Delta I_D)/I_D^2$, is constant within the working region from the deep triode to just saturation, $V_{DS} \le V_{GS}-V_T$, and this constant is dependent on $\tilde{A}_g$ and $(V_{GS}-V_T)$ only because carrier density variation, $\sigma(\Delta C)/C$, is constant everywhere within the channel for this working region. The variation on drain current is directly dependent on the variation of conductance or carrier density. The constant on $\sigma(\Delta C)/C$ has a special advantage for being used in the finite-element approach. The variation on carriers and resistance of (i,j)th cell element in the region with length ΔL and width ΔW can be given by

$$\frac{s^2_{i,j}(R)}{R^2_{i,j,N}} = \frac{s^2_{i,j}(C)}{C^2_{i,j,N}} = \frac{s^2_{i,j}(V_T)}{(V_{GS}-V_{TN})^2} = \frac{\tilde{A}^2_{VT}/\Delta L_i \Delta W_j}{(V_{GS}-V_{TN})^2} \qquad (4)$$

For a rectangular device, it is easy to predict the random mismatch by a closed-form formula [9] as

$$\frac{s^2(\Delta I_D)}{I_D^2} = \frac{2\tilde{A}^2_{VT}}{(V_{GS}-V_{TN})^2(LW)} = \frac{\tilde{A}^2_{\Delta VT}}{(V_{GS}-V_{TN})^2(LW)} \qquad (5)$$

It has to be noticed that (5) is only valid with devices that have uniform current density. Unfortunately, the current density for arbitrary-shape devices is usually not uniform and it is also very difficult to find a general closed-form formula for the non-rectangular devices. Thus, the finite-element approach is a more reasonable solution for predicting the matching performance of non-rectangular devices and it can be proven in [9] that the current variation can be expressed as

$$\frac{s^2(\Delta I_D)}{I_D^2} = 2\frac{\tilde{A}^2_{VT}}{\Delta I \Delta W (V_{GS}-V_{TN})^2} \sum_{i=0}^{N_i-1}\sum_{j=0}^{N_j-1} W(i,j)^2 \qquad (6)$$

where W(i,j) represents the contribution weight of the (i,j) element to current variation. Because $\sigma(C)/C$ is uniform through the channel region, W(i,j) can be easily derived by calculating the power distribution of each element when the device is working in the deep triode region or is simply treated as a resistor [9]. Thus, during the procedure of creating a netlist, the unit cell of 4-transistor will be replaced by a cell of 4-resistor shown in Fig. 6. Then contribution weight W(i,j) can be derived from the current and voltage distribution across the region and expressed as

$$W(i,j) = \frac{dI_{D(i,j)}\, dV_{(i,j)}}{I_D (V_D - V_S)} \qquad (7)$$

where $dI_{D(i,j)}$ and $dV_{(i,j)}$ represent the maximum current through and the maximum voltage across the cell element (i,j) shown in Fig. 6 respectively. $dI_{D(i,j)}$ and $dV_{(i,j)}$ can be inferred by data in the HSpice output file.

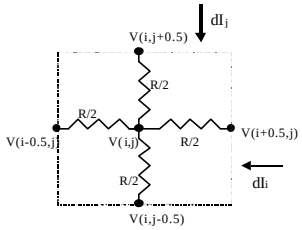

Fig. 6 Unit Cell of 4-Resistor

Next, several simulation results for current mirrors with rectangular and non-rectangular shapes will be shown by using this simulation tool. One rectangular and two non-rectangular devices, named as rectangular, trapezoid and waffle respectively, are shown in Fig. 7. The simulation results with different area sizes for the device shapes shown in Fig. 7(A), 7(B), and 7(C), are summarized into three tables, Table 1(A), 1(B), and 1(C), respectively. In these simulations, $\tilde{A}_{VT}$ is assumed as 10mV·μm ($\tilde{A}_{\Delta VT}$ as 14.14mV·μm), V_G as 2.8V, V_D as 1.7V, V_S as 0V, and V_T as 0.8V. The simulation results are plotted as a function of $1/\sqrt{Area}$ in Fig. 8. From the Fig. 8, the rectangular devices basically follow the law of area, but the trapezoid and waffle devices do not follow the law of area exactly because of the non-uniform current density. Since it is shape dependence, it will result in discrepancies on the extraction of A_{VTO} and $A_{\Delta VTO}$.

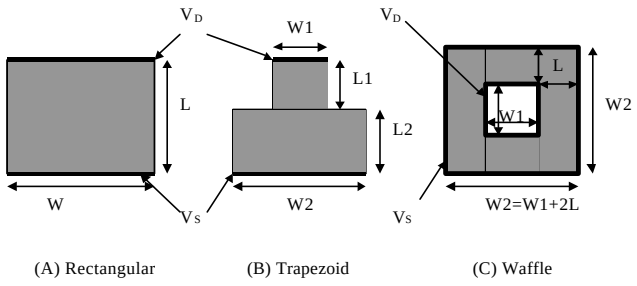

Fig. 7 Device Shapes of Current Mirrors

Table 1(A) Simulation Summary of Rectangular Device

	W (μm)	L (μm)	Area (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_D$ (%)
1	20	20	400	4.1595e-2
2	20	30	600	3.3962e-2
3	40	20	800	2.9412e-2
4	40	40	1600	2.0797e-2

Table 1(B) Simulation Summary of Trapezoid Device

	W1 (μm)	W2 (μm)	L1 (μm)	L2 (μm)	Area (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_D$ (%)
1	10	30	10	10	400	5.7841e-2
2	10	30	10	20	700	4.8211e-2
3	10	40	20	20	1000	4.3557e-2
4	20	60	20	20	1600	2.9093e-2

Table 1(C) Simulation Summary of Waffle Device

	W1 (μm)	L (μm)	Area (μm^2)	Random Mismatch $\sigma(\Delta I_D)/I_D$ (%)
1	5	8	416	5.0445e-2
2	5	10	600	4.4909e-2
3	10	10	800	3.3480e-2
4	15	16	1664	2.5659e-2

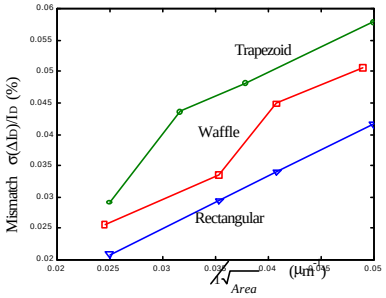

Fig. 8 Simulation Results with Different Shapes and Area Sizes of Current Mirrors

6. CONCLUSION

A CAD tool, MOSGRAD, suitable for predicting the mismatch performance of matching-critical circuits in the presence of arbitrary parameter gradients and random parameter variations has been introduced. The tool is applicable to both conventional layouts and layouts that employ arbitrarily shaped or segmented transistors. A comparison of experimental and simulation results showing the effects of linear parameter gradients showed good correlation

ACKNOWLEDGEMENT

This work was supported, in part, by National Semiconductor and the R. J. CARVER Trust. Simulation results were obtained, in part, from Avant!'s HSPICE program made available through the company's university program.

REFERENCES

[1] Mao-Feng Lan, and R. L. Geiger, "Impact of Model Errors on Predicting Performance of Matching-Critical Circuits ," in Proc. MWSCAS, Lansing, Michigan, Aug 8-11, 2000.

[2] Pelgrom, M.J. et. el. "Matching Properties of MOS transistors", IEEE J. of Solid State Circuits, Vol. 24, No. 5, pp. 1433-144-, Oct. 1989.

[3] Felt, E. et. el. "Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's", Proc. ACM, pp. 272-277, 1994.

[4] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," IEEE J. Solid-State Circuits, vol. SC-21, pp. 1057-1066, 1986.

[5] Mao-Feng Lan, Anilkumar Tammineedi, and R. L. Geiger, "A New Current Mirror Layout Technique for Improved Matching Characteristics," in Proc. MWSCAS, Las Cruces, New Mexico, Aug 8-11, 1999.

[6] Jurgen Oehm, Ulrich Grunebaum and Klaus Schumacher, "A Physical Approach to Mismatch Modeling and Parameter Correlations," Proc IEEE Int. Symp. on Circuits and Systems, pp. IV337-IV380, Geneva, Switzerland, 2000.

[7] Patrice Grignoux and R. L. Geiger, "Modeling of MOS Transistors with Nonrectangular-Gate Geometries," IEEE Transactions on Electron Devices, VOL. ED-29, No. 8, pp. 1261-1269, August 1982.

[8] Anne Van den Bosch, M. S. J. Steyert and W. Sansen, "A High-Density, Matched Hexagonal Transistor Structure in Standard CMOS Technology for High-Speed Applications," IEEE Transactions on Semiconductor Manufacturing, VOL. 13, No. 2, May 2000.

[9] Mao-Feng Lan and R. L. Geiger, "Modeling of Random Channel Parameter Variations in MOS Transistors," in Proc. ISCAS, Sydney, Austria, May., 2001.