Current Mirror Layout Strategies for Enhancing Matching Performance

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ABSTRACT

This paper proposes new current mirror layout strategies to reduce the matching sensitivity to the linear parameter gradients. Effects of threshold gradients across a mirror on the matching characteristics of current mirrors are discussed. The performance of new and existing layouts are compared for threshold voltage gradients at arbitrary angles through the active area. Simulation results show a significant improvement in matching characteristics of the proposed structures over what is achievable with existing layout techniques in demanding applications.

I. INTRODUCTION

Paralleling the increasing demand for cost-effective integrated high-end linear and mixed-signal systems is the need for improved matching performance in basic circuit blocks because the system performance is dominated by the matching characteristics of basic circuit blocks such as current mirrors and differential amplifiers. Researchers have proposed models for predicting the matching characteristics of closely-placed devices [1-3], but these models have been used almost exclusively to assess performance characteristics of circuits and layout techniques that have been well-known for over two decades. Further, these models have fundamental limitations in characterizing the effects of systematic parameter variations through the channel region of transistors.

It is generally agreed that the matching characteristics of closely placed devices can be attributed to systematic and random variations in both geometric parameters and process parameters. The traditional approach for managing the affects of random variations is to increase the area of the matching-critical devices to the level that the random mismatch effects are reduced to an acceptable level. It is often more difficult to compensate for the systematic variations which may be random at the wafer or even die level but which are highly correlated at the basic circuit block level. Because the area and pitch of a current mirror is relatively small to that of a die, systematic variations are generally assumed to be represented by linear gradients in the matching-sensitive part of the circuit and common centroid layout techniques such as that of Fig. 1 is widely used to minimize the effects of the linear gradients. The most standard common centroid layout technique for a current mirror or a differential pair uses two cross-connected pairs of rectangular transistors. Felt et. al. [3] have reported that the effects of systematic variations are often comparable to the effects of random variations even with good layout techniques thus affirming the need for managing simultaneously the effects of both systematic and random variations. Some of the systematic variations are often mistakenly assumed to be random (an assumption that can cause significant errors in a statistical analysis because of the inherent correlation of these parameters). We believe that the impact of not correctly handling the systematic variations is even more significant than suggested by Felt et. al, in the design of high-end linear circuits.

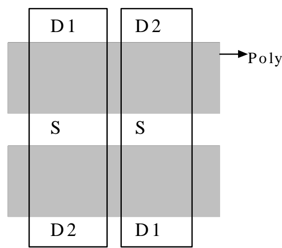


Fig.1. Common Centroid Layout

Although variations in threshold voltage (V_T), mobility (u), C_{OX}, along with some other parameters affect mirror matching, the dominant effects are generally threshold voltage variations. In this paper, only the effects of spatially dependent threshold voltage variations are considered for various layouts to compare matching characteristics but the reduced sensitivity to gradients in other parameters parallel that observed for V_T gradients in the proposed structures.

A basic current mirror is depicted in Fig. 2. The input port is at the drain of transistor M1, the output is at the drain of transistor M2 and the sources are common. Five different common layouts for this current mirror are shown in Fig. 3. Fig. 3(a) shows the simple layout technique. Although parameter gradients that occur in the direction from drain to source (designated as "vertical" in Fig. 3) cause no device matching problems with this structure, the matching performance degrades substantially if there are substantial "horizontal" components of the gradient. The interdigitized layout structures of Fig. 3(b) and Fig. 3(c) have a reduced sensitivity to horizontal components of the gradient. The two-segment interdigitized structure of Fig. 3(b) is a common centroid layout and, as such, most existing models predict linear parameter gradients will not cause any mismatch if this is used to form a current mirror or cause any offset voltage if it is used as the source-coupled pair in a differential amplifier. In what follows, it will be

shown that the gradient effects are still substantial on the interdigitized layout of Fig. 3(b) and 3(c). The two-segment common centroid layouts of Fig. 3(d) and Fig. 3(e) generally offer better matching performance than the other structures presented in the figure. The common centroid layout technique is currently being widely used and it does reduce systematic gradients when compared to the simple and interdigitized techniques. Since these structures both have a common centroid, most existing models predict complete immunity to linear gradient effects. In what follows, it will be shown that even the structures of Fig. 3(d) and 3(e) have a systematic mismatch component that can be significant in application with stringent matching requirements.

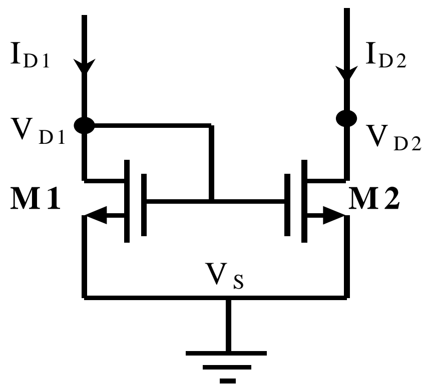
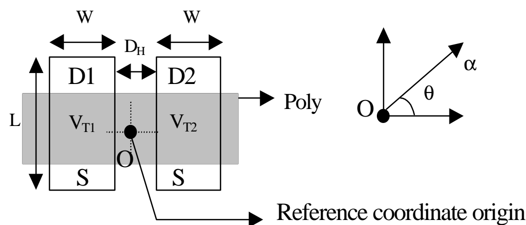
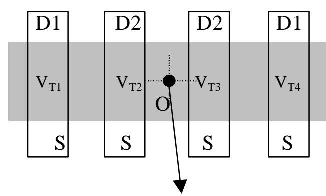
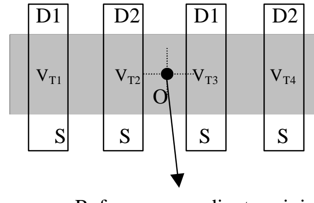


Fig. 2. Basic Current Mirror Circuit

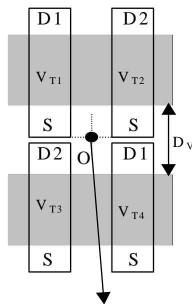


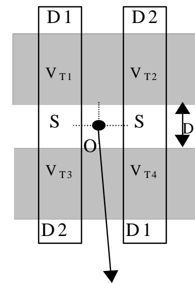
(a) Simple Layout





(b) Interdigitized Type I (c) Interdigitized Type II





(d) Common Centroid Type I (e) Common Centroid Type II

Fig. 3. Existing Current Mirror Layout Techniques (D1 is Drain of M1, D2 is Drain of M2, S is Common Source, and O : Reference Point)

In this paper, several new common-centroid layout techniques are introduced. One uses an interconnection of two 4-segment rectangular transistors. The balance are non-rectangular structures in which the active region is continuously distributed between the input and output ports of the current mirror and in which there is no obvious equivalent lumped two-transistor equivalent circuit. In contrast to existing mirror circuits in which the matching-sensitive part of the circuit is comprised of two source-coupled transistors, the nonrectangular structures discussed in this paper are 4-terminal devices that can be viewed as dual-drain transistors. It will be show that the proposed layout

structures can be designed so that the mirror gain is less sensitive to the linear parameter gradients than what is achievable with the widely used two-segment common centroid structures.

II. GRADIENT MODELING

In this section, the effects of threshold voltage gradients on the matching performance of current mirrors are investigated. In particular, the effects of threshold voltage gradients at any angle across a wafer for interdigitized and common-centroid layouts are compared with the matching characteristics of a simple mirror layout. The parameter gradients are commonly modeled in a distributed way through the active devices themselves and thus threshold voltage is modeled as a distributed position-dependent parameter through the active devices, $V_T(x,y)$. The widely used approach for predicting the effects of the threshold gradient is based upon deriving an equivalent threshold voltage [1] for the device as given by the following equation.

$$V_{Teq} = \frac{\iint_{Active\ Area} V_T(x, y)\,dxdy}{Active\ \ Area} \tag{1}$$

and using this threshold voltage in the existing lumpted-parameter models of a trtansistor.

If the threshold gradient amplitude is α and the gradient direction is θ as indicated in Fig. 3, it follows that for the simple current mirror structure (Fig. 3(a)):

$$V_{T1} = V_{TN} - \alpha\left(\frac{W}{2} + \frac{D_H}{2}\right)\cos\theta \tag{2}$$

$$V_{T2} = V_{TN} + \alpha\left(\frac{W}{2} + \frac{D_H}{2}\right)\cos\theta \tag{3}$$

where

1) D_H is the minimum separation, usually 4 lambda, between the two drain diffusions, D1 and D2.
2) V_{T1} and V_{T2} are the threshold voltages of the two transistors of equal sizes W/L
3) V_{TN} is the threshold voltage at the coordinate reference point O in Fig. 3(a).

If the equivalent V_T equation (1) is applied to the Type I interdigitized layout of Fig. 3(b), transistors M1 and M2 have the same threshold voltage given by the following equation.

$$V_{TD1} = V_{TD2} = V_{TN} \quad (4)$$

This equivalent threshold voltage was expected since this is a common centroid layout. This model predicts perfect matching can be achieved using this layout structure. However, experimental results have not been in accordance with the perfect matching prediction thus leading to the conclusion that this simple integral model can significantly skew matching results. An alternative approach to modeling the mismatch effects using a segmented integral model does give better results. In this approach, instead of treating transistor M1 as a single transistor and using equation (1) to predict the equivalent threshold voltage, we will assume M1 is modeled as the parallel connection of two lumped transistors in which the integral model of (1) is used to independently obtain the equivalent threshold voltage of each of the two components. For a multi-segment layout, the equivalent threshold voltage for each segment is predicted using the integral model of (1) and these transistors are then placed in parallel to form a circuit that represents the transistor designed as M1 or M2 in Fig. 2. We refer to this modeling approach as the segmented integral model. In general, using this approach, there does not exist an

equivalent threshold voltage for the transistor M1 and the I-V characteristics of the parallel-connected segments are not identical to the I-V characteristics of an equivalent single transistor if the same functional form for the lumped model is used for modeling all segments. Formally, the threshold voltage for the Kth segment in the segmented integral model is given by

$$V_{Teq,K} = \frac{\iint_{Active\ Area,K} V_T(x,y)dxdy}{Active\ Area,K} \tag{5}$$

Using this approach, the threshold voltages for the simple structure remain the same as before while those of the four unit transistors for the Type I interdigitized structure are given by,

$$V_{T1} = V_{TN} - \boldsymbol{a}\left(\frac{3W}{4} + \frac{3D_H}{2}\right)\cos\boldsymbol{q} \tag{6}$$

$$V_{T2} = V_{TN} - \boldsymbol{a}\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\boldsymbol{q} \tag{7}$$

$$V_{T3} = V_{TN} + \boldsymbol{a}\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\boldsymbol{q} \tag{8}$$

$$V_{T4} = V_{TN} + \boldsymbol{a}\left(\frac{3W}{4} + \frac{3D_H}{2}\right)\cos\boldsymbol{q} \tag{9}$$

where V_{T1} and V_{T4} correspond to the two segment transistors of M1 and V_{T2} and V_{T3} correspond to the two segment transistors of M2. The four expressions also hold for the Type II interdigitized layout of Fig. 3(c) where V_{T1} and V_{T3} correspond to the two segment transistors of M1 and V_{T2} and V_{T4} correspond to the two segment transistors of M2. Similarly, threshold voltages for the four segment transistors were determined for the common centroid Type I and Type II layouts of Fig. 3(d) and 3(e) and are given by,

$$V_{T1} = V_{TN} - \boldsymbol{a}\left(\frac{W}{4} + \frac{D_H}{2}\right)\cos\boldsymbol{q} + \boldsymbol{a}\left(\frac{D_{V/S}}{2} + \frac{L}{2}\right)\sin\boldsymbol{q} \tag{10}$$

$$V_{T2} = V_{TN} + \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta + \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (11)$$

$$V_{T3} = V_{TN} - \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta - \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (12)$$

$$V_{T4} = V_{TN} + \alpha(\frac{W}{4} + \frac{D_H}{2})\cos\theta - \alpha(\frac{D_{V/S}}{2} + \frac{L}{2})\sin\theta \quad (13)$$

where D_V and D_S are the minimum required distances between the two channels as shown in Fig. 3(d) and Fig. 3(e) respectively. V_{T1} and V_{T4} correspond to the two segment transistors of M1 and V_{T2} and V_{T3} correspond to the two segment transistors of M2. It is apparent from these equations that the threshold voltages of the individual segments differ and are dependent upon the magnitude and angle of the gradient as well as the geometries of the segments. What is less apparent is how these threshold variations affect matching performance.

The above equations were used to simulate mismatch for the five mirror layouts and for a gradient of fixed amplitude but arbitrary direction. In these simulations, it was assumed that V_{TN}=0.7339V, α=1mV/um, W=40um, L=40um, and D_H=4um. The gradient direction was varied between 0° and 360°. For a fair comparison, mismatch for all the structures were measured with the same active area and the same equivalent W/L. Here, mismatch is defined by,

$$Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100 \ \% \quad (14)$$

where I_{D1} and I_{D2} are the input and output currents as depicted in Fig. 2. The simulation results for an input current of I_{D1}=77.5μA are shown in Fig 4. In these simulations, the voltages V_{DS2} was set equal to the resultant V_{DS2} to remove mismatch due to the output impedance.

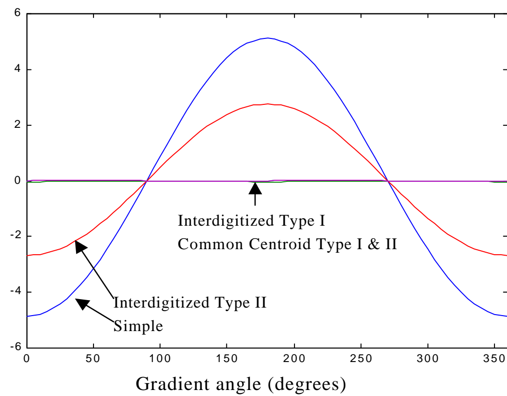


Fig. 4. Comparison of Systematic Mismatch for Simple, Interdigitized and Common Centroid Layouts

From these simulation results, it can be seen that interdigitized Type I, common centroid Type I and common-centroid Type II have very good matching characteristics relative to the other two structures. An expanded view of the latter three results is shown Fig. 5. From these simulation results, it can be observed that the interdigitized Type I layout has mismatch characteristics with minimum deviations at θ = 90° and 270° and maximum deviations of about –0.04% at 0° and 180°. Further, the mismatch is always negative. The common centroid Type I and II layouts have better and similar matching performance with maximum mismatch magnitudes of about 0.02% occurring at θ = 45°, 135°, 225° and 315° for the 1 mV/μm gradient.

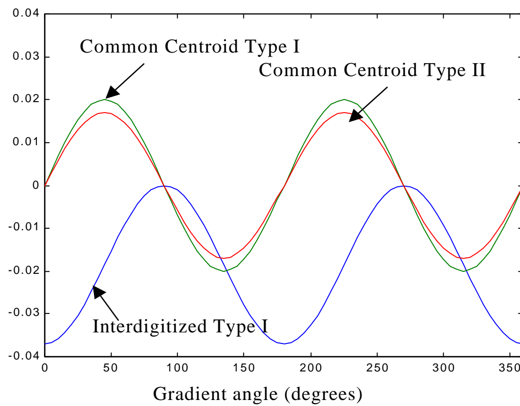


Fig. 5. Comparison of Interdigitized and Common Centroid Layouts in closer detail

The simulation results show that the matching characteristics are strongly a function of the angle of the threshold voltage gradient across a die and that, for any angle, the effects of the threshold gradient for the common centroid layouts is small. The results also show, in contrast to the well-accepted premise that the effects of linear gradients can be readily modeled [4] and are inherently canceled in common centroid structures [3], that the threshold gradients through the devices themselves create an angle-dependent gradient even in common centroid structures. The issue of the validity of using the segmented integral model does deserve attention since it was shown that the integral model itself introduces substantial errors in matching-critical applications. The results that were presented in this section that are based upon simple closed-form expression for lumped model parameter such as (6)-(9) or (10)-(13) are in close agreement to what is attainable with a full two-dimensional simulation [5] of the distributed device parameters for the common centroid and interdigitized structures of Fig. 3. Simulation results for these structures based upon a two-dimensional simulation are discussed later in this paper.

III. PROPOSED LAYOUT TECHNIQUES

A. Four-Segment Layout Structure

A new four-segment common centroid structure that offers improvement in matching over what is achievable with the two-segment common centroid techniques is shown in Fig. 6. The proposed layout technique has the property that it also minimizes the mismatch at 45°, 135°, 225° and 315° angles where the two-segment common centroid structures exhibit maximum mismatch. It can be observed that in the common centroid layout technique of Fig. 3(d) and Fig. 3(e), the layout is the same when rotated by 180°, thus canceling the mismatch at 90° while having a maximum at 45°. In the proposed technique, the layout is the same when rotated by 90°, thus canceling the mismatch at 45°. In the proposed structure, each transistor is segmented into 4 unit transistors since the source and the gate are common for the current mirror, the source and gate are shared for all the eight unit transistors.

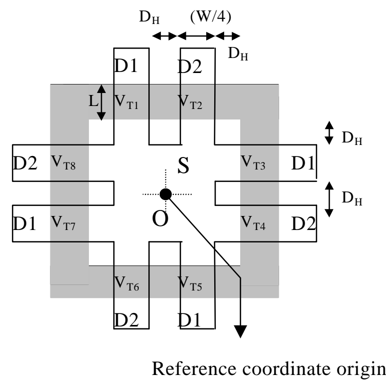


Fig. 6. Proposed Current Mirror Layout Technique – Four-Segment Structure

The segmented integral model was used to evaluate the matching characteristics of the proposed technique paralleling the analysis for the layout techniques of Fig. 3 discussed in the previous section. The threshold voltages of eight unit transistors in Fig. 6 are given by:

$$V_{T1} = V_{TN} - \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\cos\boldsymbol{q} + \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\sin\boldsymbol{q} \quad (15)$$

$$V_{T2} = V_{TN} + \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\cos\boldsymbol{q} + \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\sin\boldsymbol{q} \quad (16)$$

$$V_{T3} = V_{TN} + \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\cos\boldsymbol{q} + \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\sin\boldsymbol{q} \quad (17)$$

$$V_{T4} = V_{TN} + \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\cos\boldsymbol{q} - \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\sin\boldsymbol{q} \quad (18)$$

$$V_{T5} = V_{TN} + \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\cos\boldsymbol{q} - \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\sin\boldsymbol{q} \quad (19)$$

$$V_{T6} = V_{TN} - \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\cos\boldsymbol{q} - \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\sin\boldsymbol{q} \quad (20)$$

$$V_{T7} = V_{TN} - \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\cos\boldsymbol{q} - \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\sin\boldsymbol{q} \quad (21)$$

$$V_{T8} = V_{TN} - \boldsymbol{a}(\frac{3D_H}{2} + \frac{W}{4} + \frac{L}{2})\cos\boldsymbol{q} + \boldsymbol{a}(\frac{D_H}{2} + \frac{W}{8})\sin\boldsymbol{q} \quad (22)$$

With this model, it can be readily shown that the mismatch for the proposed technique is zero at 45°, 90°, 135°, 180° and so on, giving a big improvement in matching characteristics over that of the two-segment common centroid layout of Fig. 3. A disadvantage of the proposed technique is the requirement of more silicon-area. When the silicon area increases, the assumption that the gradient remains linear throughout the entire matching-critical region may not be completely justifiable. Nonlinear gradients are, in general, not inherently cancelled with common centroid layouts. Some new layout

structures that require less area than what is required for the four-segment layout of Fig. 6 are discussed in the following section.

For the same reason the integral model gives incorrect results with segmented transistors, even the errors caused by the segmented integral model become significant when close matching is expected. A two-dimensional simulator [5] was developed for predicting matching characteristics in the presence of either linear or non-linear gradients through the active area of the devices. The simulator can be used to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients in threshold voltage or any other process parameters.

The four-segment structure (Fig. 6), the interdigitized Type I layout, the common centroid Type I layout and the common centroid Type II layout were simulated with this two-dimensional simulator for the 2μm CMOS process available through MOSIS. The mismatch characteristics as a function of angle are shown in Fig. 7. In this simulation, the same device size and gradient parameters used in Section II were used. It can be seen that the four-segment layout improves the matching performance by at least two orders of magnitude over what is achievable with the two-segment common centroid layouts in the presence of linear threshold gradients. The simulation results for the proposed four-segment layout structure in Fig. 7 are expanded in Fig. 8. It is observed that the mismatch of the proposed four-segment structure is zero at angles of 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. Table 1 summarizes the worst case mismatch in the structures simulated. Also shown in this table is a comparison of the results as predicted by the simple integral model, the segmented integral model and the actual distributed parameter model. The maximum effective achievable resolution is calculated from the results of the simulator

such that the worst case mismatch is less than ½ LSB relative to full-scale. It can be seen that in the presence of perfectly linear gradients at 1 mV/µm, the two-segment common centroid structure can achieve only about 12-bit resolution while the proposed structure can achieve 18-bit resolution showing a big improvement in matching with the new layout. It should be emphasized that the results are valid only for a perfectly linear gradient of 1mV/µm and the resolution would be lower if the gradient is non-linear or if other non-idealities such as random variations in either dimensional or process parameters were included.

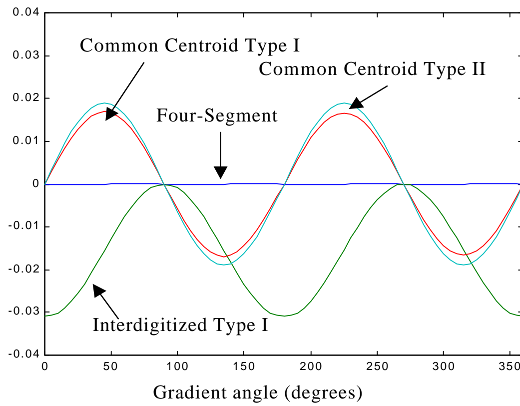


Fig. 7. Comparison of Interdigitized, two-Segment Common Centroid and Four-Segment Layouts

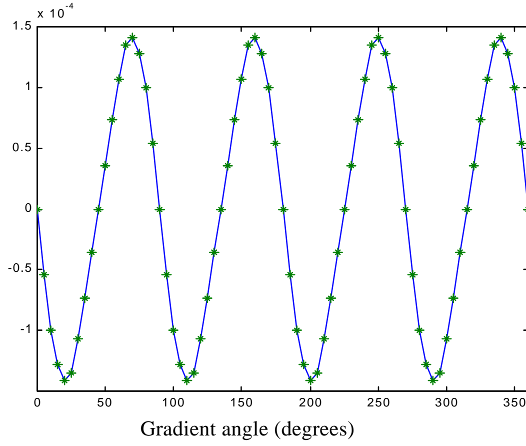


Fig. 8. Simulation result of Proposed Four-Segment Common Centroid Layout

Table 1. Comparison of various structures with a linear gradient of 1mV/um

Structure	Worst Mismatch (%)			
	Simple integral model	Segmented integral model	Distributed simulator	Effective Resolution
Simple	5.1092	5.1092	4.8807	3-bit
Interdigitized Type I	0	3.6918e-2	3.0885-2	11-bit
Interdigitized Type II	2.7552	2.7547	2.6329	4-bit
Two-Segment Common centroid Type I	0	2.0005e-2	1.6966e-2	12-bit
Two-Segment Common	0	1.6928e-2	1.8949e-2	12-bit

centroid Type II				
Four-Segment Common Centroid Structure	0	2.0966e-14	1.4090e-4	18-bit

B. Non-Rectangular Structure

A non-rectangular layout of a current mirror is shown in Fig. 9. In this circuit, the polysilicon region (gray) and the two regions labeled D1 are connected together and serve as the input current node. The diffusion labeled S is thought of as the 'source' for the device and is connected to ground. The two regions labeled D2 are connected together and serve as the output current node. This is a special case of what is occasionally termed a "waffle transistor" and will be designated as a "waffle structure" throughout the remainder of this paper. To avoid possible confusion, the distinction between the waffle structure of Fig. 9 and the conventional waffle transistor will be clarified. In a waffle transistor, the diffusion "islands" internal to the gate polysilicon are alternately source and drain connections. In the waffle layout of the current mirror of Fig. 9, there is no inherent two-transistor equivalent circuit but instead it is a distributed two-segment dual-drain device in which the source comprises the perimeter of the polysilicon region and the dual drains are alternately connected islands internal to the gate polysilicon.

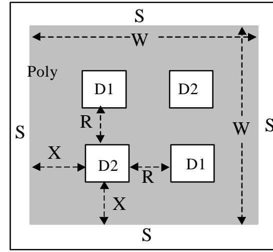


Fig. 9. Non-Rectangular Current Mirror Layout Technique (Waffle Structure)

The active region is shared between the two drains in this layout. In what follows, it will not only be shown that this two-segment dual-drain device performs as a current mirror but that in the presence of parameter gradients, if properly designed, it can offer better matching performance than what is achievable with the standard two-segment common controid layouts of Fig. 3(d) and Fig. 3(e). Without going into a rigorous definition of what constitutes a “common centroid” characteristic in a distributed dual-drain transistor, it is suffice to say that it can be shown that the waffle structure is also a common centroid layout.

Because the waffle mirror is not representable with two distinct source-connected transistors, standard modeling techniques cannot be applied to the structure. Because the simulator [5] is able to predict the matching characteristics of an arbitrary layout of any size for arbitrary gradients, it will be used to predict the matching characteristics of the waffle mirror structure in the presence of linear threshold gradient.

For the waffle structure of Fig. 9, the drain current and matching performance are affected by both the size and the positions of the drain diffusions in the layout. The relationship between the drain current (with gate tied to D1 and D2 left open) and the positions of the drain diffusions for the 2μm CMOS process available through MOSIS

was evaluated using the simulator. Results are given in Fig. 10. In this figure, the y axis is the magnitude of drain current and the x axis is given by the ratio of X divided by W, where X (shown in Fig. 9) is the space from a diffusion to the source edge and W is the width of the device that is assured to be square. In this simulation, the total active area was kept fixed at (80μmx80μm-4x8μmx8μm)=6144 μm^2 as was the size of the drain diffusions which were 8μm x 8μm. It is observed that the drain current increases when the drain contacts approach to the edge of source.

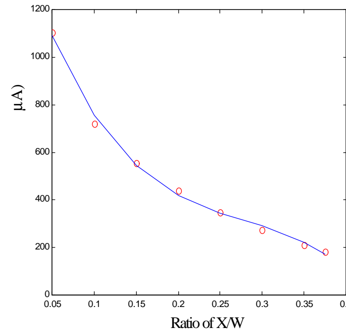


Fig. 10. Drain Currents with the Positions of Drain Contacts

As described in the previous section, the waffle layout structure is the same when rotated by 180°, thus canceling the mismatch at 90° while having a maximum mismatch at 45°, 135°, 225° and 315° as was the case for the two-segment common centroid structures of Fig. 3(d) and Fig. 3(e).

The worst-direction matching characteristics of the waffle structure for a gradient of α=1mV/μm when used as a current mirror were simulated and are shown in Fig. 11 as a function of the total active area. In this simulation, the distance X was kept at (3/16)W, R was (3/8)W and the drain diffusions were square with a side length of (1/8)W. It is well known that in current mirrors implemented with rectangular transistors, the standard

deviation of the random mismatch decreases with the square root of the total active area. The effects of random mismatch for the waffle structure were simulated with a value of A_{VTO} of 5.3mV. μm. The standard deviation of the mismatch expressed in percent is also shown in Fig. 11.

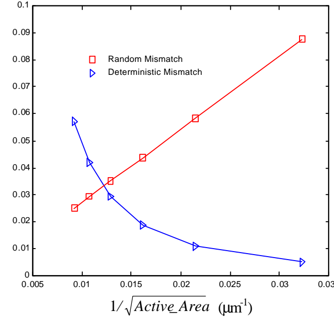


Fig. 11. Deterministic and Random Mismatches of Waffle Structure

The results show that the random mismatch is linearly proportional to $(1/\sqrt{Active_Area})$ and the systematic mismatch is approximately inversely proportional to $(1/\sqrt{Active_Area})$. Thus, tradeoffs must be made between increasing the active area to reduce random mismatch effects and decreasing the area to minimize worst-case gradient effects. These same tradeoffs must be made when using conventional layout structures [1].

To evaluate the matching performance, the matching characteristics of the waffle structure will now be compared with those of the two-segment common centroid structure of Fig. 3(e). In order to make a fair comparison on the matching performance, the two-segment common centroid structures are designed to have the same active areas, the same nominal drain current and the same excess bias (V_{GS}-V_T) as the waffle structures. The comparison is made for a waffle structure that is 80μm x 80μm as a

function of the parameter X in Fig. 12. The drain diffusions were fixed at 8μm x 8μm. Since changing the parameter X will result in a change in either current or excess bias voltage, we kept the excess bias fixed and allowed the current to vary while keeping the current the same in both the waffle structure and the corresponding common centroid structure of Fig. 3(e). The comparison of the worst-direction matching performance is shown in Fig. 12 for a gradient magnitude of α=1mV/μm. This figure shows that the two-segment waffle structure can offer significantly better matching performance than the two-segment common centroid structure in the presence of linear parameter gradients but also that the positioning of the drain diffusions is important. It is also observed that the matching performance of the waffle mirror structure for a fixed active area improves when the drain contacts are moved farther from the source contact.

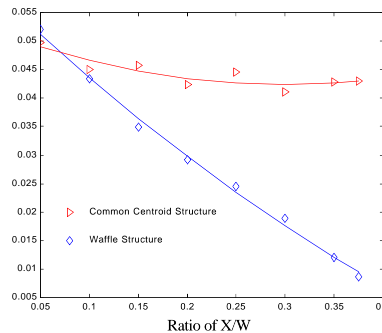


Fig. 12. Comparison of Waffle and Common Centroid Structure with a Fixed Active Area

Fig. 13 shows the mismatch as a function of angle for a waffle structure with W=80μm, X=20μm and with 8μm drain diffusions as compared with that of the two-segment common centroid structure of Fig. 3(e). As before, the same active area, current and excess bias were used for both layouts.

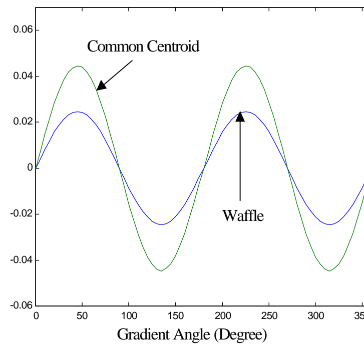


Fig. 13. Performance Comparison of Common Centroid and Waffle Structure

From a practical viewpoint, it must be emphasized that the comparative results presented in Fig. 12 are obtained for a specific parameter gradient and a specific total active area. The relative performance of the two structures is strongly dependent upon both active area and the relative positioning of the drain diffusions in the waffle structure. Different parameter gradients and/or different relationships between the excess bias and the nominal drain current will affect where the crossover in Fig. 12 in performance between the common centroid layout of Fig. 3(e) and the waffle structure occurs.

The issue of optimality of the proposed waffle structure has not yet been determined. As is apparent from Fig. 10, even for a given active area, tradeoffs between the size and location of the drain diffusions can be made. Optimal structures should offer even better performance than what was presented here.

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IV. LAYOUTS BASED ON THE PROPOSED TECHNIQUES

As mentioned previously, the proposed four-segment layout of Fig. 6 is not particularly area efficient because it requires considerable area around the individual/common source regions. The two-segment waffle layout technique is quite compact but does not have as good of matching properties as the four-segment structure of Fig. 6. Thus, the question naturally arises if it is possible to combine the advantages of these two layout techniques to generate new layouts that have improved matching and yet area efficient. The answer is yes. Three layouts combining the advantages of two techniques are shown in Fig. 14. Although each layout configuration in Fig. 14 has different area requirements, these three layouts all not only have better area budget than the four-segment layout but also have similar matching characteristics. These layouts are common-centroid four-segment distributed channel structures. For all these structures, mismatches are minimized for linear gradients at 45°, 135°, 225° and 315°. It is beyond the scope of this paper to fairly compare the three layouts in Fig. 14 since the structures do not have the same active area, the same drain currents and the same excess bias. A general idea about how these three layouts perform, however, can be developed from the following simulations. Simulation results for the three layouts of Fig. 14 for special device dimensions and a threshold gradient of α=1mV/μm appear in Fig. 15. For the simulation of the layout of Fig. 14(a) shown in Fig. 15(a) it was assumed that X=20μm. In the simulation of the layout of Fig. 14(b) shown in Fig. 15(b), the dimensions of X=20μm and Y=4μm were used. The simulation results for the circuit of Fig. 14(c) shown in Fig. 15(c) were based upon a device dimension of X=8μm. In all cases, the voltage of the output node, drain D2, was set equal to that at the input node, drain D1.

The input currents are 117μA, 195μA, and 744μA for the layouts in Fig. 14(a), Fig. 14(b), and Fig. 14(c) respectively. It is apparent that these three layouts have at least two orders of magnitude better matching performance in the presence of linear threshold gradients than the two-segment common centroid layouts of Fig. 3(d) and 3(e) even without optimization.

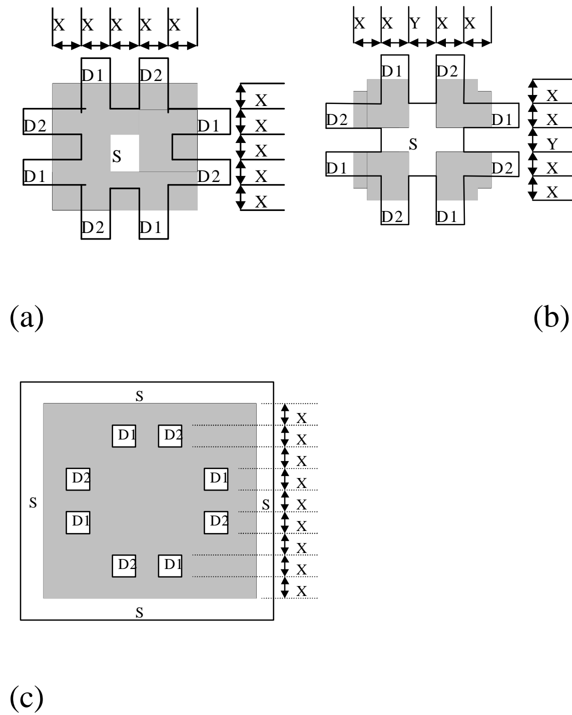
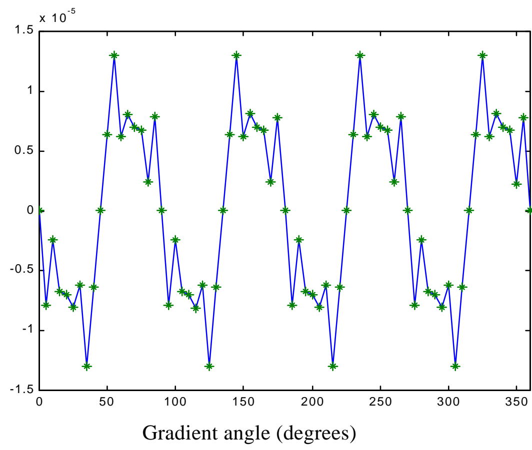
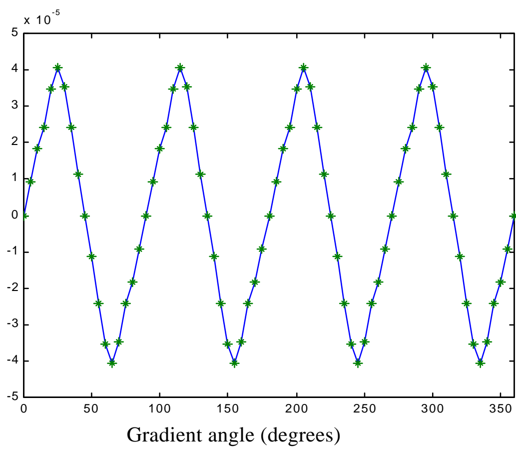


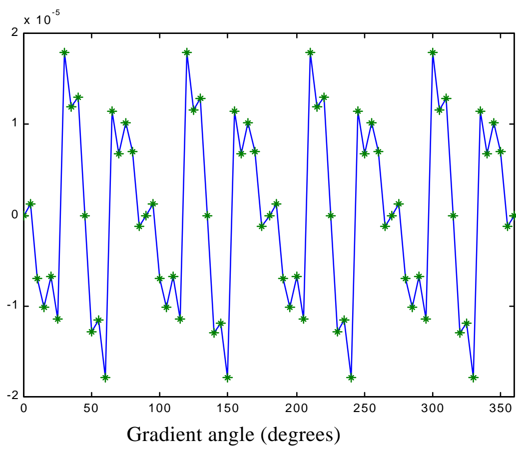
Fig. 14. Proposed Current Mirror Layout Techniques



(a)



(b)



(c)

Fig. 15. Simulation Results for Mirror Layouts of Fig 14

V. CONCLUSION

Several new current mirror layout techniques have been introduced that offer substantial improvements in matching characteristics over what is achievable with the simple, interdigitized and the two-segment common centroid structures in the presence of linear parameter gradients. The layout techniques include a four-segment rectangular structure and several non-rectangular layout structures that utilize a distributed-channel dual-drain device. Simulation results showed an improvement in worst case matching of at least two orders of magnitude over what is attainable with the standard two-segment common centroid layout scheme in the presence of linear threshold gradients. The four-segment dual-drain distributed-channel structures have similar matching characteristics to the four-segment rectangular structure but a better overall area budget. A comparison of the performance of several layout structures has shown substantial differences in the sensitivity of the mirror gain due to parameter gradients.

ACKNOWLEDGEMENT

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