A Low Temperature Sensitivity Switched-Capacitor Current Reference

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Abstract **- A current reference with low temperature sensitivity based on a switched-capacitor technique has been developed. The implementation is targeted for a 0.18μ CMOS process. HSPICE simulations using level 49 models valid over a wide temperature range were used to verify the design. The simulation results predict variations of less than 0.029% over a temperature range of –40 °C to 125 °C.**

1 Introduction

Current references are needed in many analog signal processing applications including operational amplifier (opamp) and data converter bias circuits. These applications often require a reference current with low temperature dependence.

Unlike voltage references that can be derived from intrinsic physical values of the process, no intrinsic current reference is available in CMOS [1]. As a result, reference currents are often obtained by applying a temperature stable voltage (obtained from a voltage reference) across a resistor. The resistor is either integrated on-chip or may be supplied off-chip for improved control over temperature characteristics. However, both cases have drawbacks. On-chip resistors typically exhibit large temperature dependence while off-chip resistors are often not a feasible option for many applications due to cost and area considerations. This work circumvents the need for an accurate on-chip resistor by using a switched capacitor technique to generate a temperature independent current

The previous work in the area is briefly surveyed in section 2. The newly proposed structure is introduced in section 3. Design considerations and modifications to handle certain requirements are detailed in section 4 while simulation results are presented in section 5 followed by conclusions.

2 Background

Approaches that use a resistor to generate a temperature independent current reference have been reported in [1]-[3]. Due to the large temperature coefficients of polysilicon and well diffusions, monolithic resistors exhibit large temperature dependence. To overcome this problem, resistorless architectures have also been developed [4][5]. Integrated capacitors can be fabricated with greater precision and exhibit significantly lower temperature dependence than integrated resistors. Therefore, switched capacitor methods of generating temperature stable currents have emerged [6]-[8]. This paper presents a current reference using switched-capacitor based circuit to deliver and maintain a stable current.

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3 Current reference architecture

Precise crystal-based clocks and temperature independent voltage references are commonly available on-chip. Given that fact, a temperature stable current can be developed using a switched capacitor technique. The concept involves periodically dumping a fixed amount of charge onto a circuit node whose time-average value is held fixed by a feedback network. The schematic diagram of the proposed circuit reference is shown in Fig. 1.

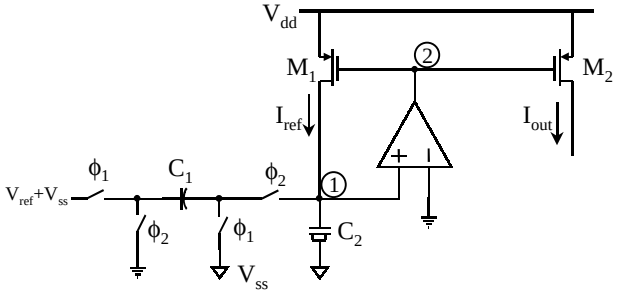

Figure 1: Proposed current reference

The circuit operates as follows. ϕ_1 and ϕ_2 are non-overlapping clocks of frequency f_{clk}. The amplifier is assumed to have a single pole response. Its speed (unity gain frequency) is intentionally set very low so that it is fast enough to respond to temperature variations yet slow enough to be unable to effectively respond to signals operating at the clock frequency. During ϕ_1, C_1 charges to V_{ref}. During ϕ_2 the charge on C_1 is dumped onto node 1. The instantaneous change in voltage on node 1 due to this charge is given by

$$\Delta V = -\left(\frac{C_1}{C_1 + C_2}\right)\cdot\left(V_{ref} + V_1\right) \qquad (1)$$

where V_1 is the voltage on node 1 immediately preceding the charge transfer, as shown in Fig. 2. The

amplifier responds to the low-frequency component of the signal on node 1. Over time, it adjusts the bias on M_1 so that the time average value of the signal present on node 1 is zero. In steady state, the signal on node 1 looks like the one shown in Fig. 2.

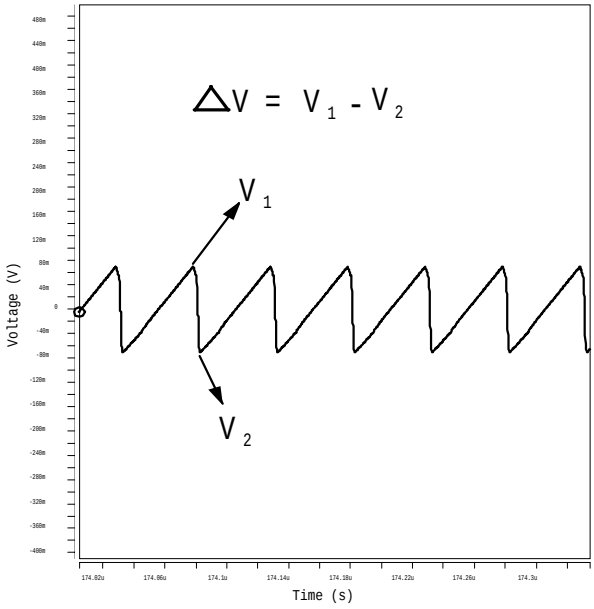

Figure 2: Voltage at node 1 of Fig. 1

It is a sawtooth type waveform centered about zero. The sawtooth shape arises due to the steady charging of M_1 interrupted by the periodic charge transfers from the switched capacitor network. The peak-to-peak magnitude of the signal is given by (1). Since it is centered about zero, the voltage on node 1 just prior to the charge transfer, V_1, is approximately given by

$$V_1 = -\frac{\Delta V}{2} \qquad (2)$$

Substituting (2) into (1) and solving for ΔV yields the peak-to-peak magnitude of the ripple on node 1 in terms of fixed parameters. This ΔV is given by

$$\Delta V = -\left(\frac{2C_1}{C_1 + 2C_2}\right) \cdot V_{ref} \qquad (3)$$

Thus, the ripple on node 1 can be controlled via the ratio C_2/C_1. A large C_2 results in reduced ripple at the expense of increased die area. The current delivered by the switched capacitor network is approximately given by

$$I_{ref} \cong C_1 \cdot V_{ref} \cdot f_{clk} \qquad (4)$$

Due to process variability, the actual post-fabrication value of the current can exhibit significant deviation from the designed value. However, due to the low temperature coefficient of monolithic capacitors, for a given die the current should remain relatively constant over temperature variations.

4 Design Considerations

Design choices affect the transient startup time, the amount of output ripple, and the stability in presence of a temperature dependent load. To help the designer make intelligent tradeoffs, each of these issues is discussed in this section

4.1 Increasing the output resistance

Due to the finite output impedance of M_2, some temperature dependence is introduced if the drain voltage of M_2 is allowed to vary. This is an especially important issue if the load is temperature dependent. To address this issue, output impedance enhancement may be required. One possible method, the regulated cascode, is shown in Fig. 3. In less sensitive situations, standard cascoding may suffice.

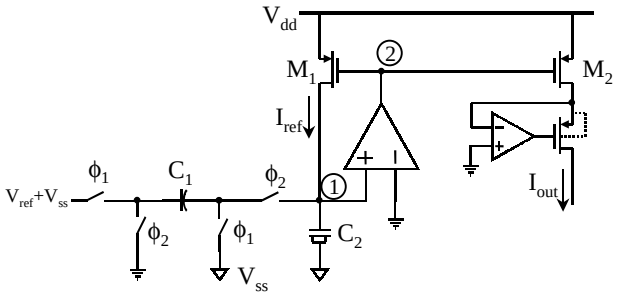

Figure 3: Proposed circuit with improved output resistance

Note that in Fig. 3, drain voltage of M_2 is fixed at 0V thereby facilitating accurate current mirroring of the reference current. Cascoding not only improves the output resistance of the current reference but also reduces the sensitivity to supply voltage variations.

4.2 Hold capacitor and ripple

Since the amplifier is intentionally made slow, it attenuates the high-frequency components of the signal present on node 1. However, its response is not zero at those frequencies. Consequently, some ripple will be present in the output current. Fortunately, the magnitude of the ripple can be managed by controlling the ratio C_2/C_1 and the gain-bandwidth product of the amplifier. Reducing the gain-bandwidth product of the amplifier will result in less output current ripple but it will also affect how fast the system will respond to temperature changes. Since temperature changes

are generally low frequency in nature, reducing the speed of the amplifier is acceptable but it will extend the length of the transient startup period.

For applications with very low ripple requirements, a filter can be inserted as shown in Fig. 4. A simple filter such as one shown in Fig. 5 can be used. Since precise filter characteristics are not required in this application, capacitors can be implemented as MOSCAPs [9] and resistors can be implemented using triode region transistors.

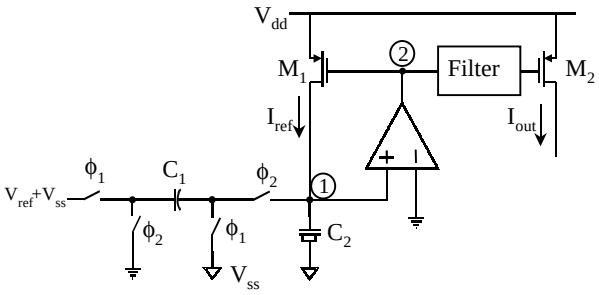

Figure 4: Proposed circuit with filter

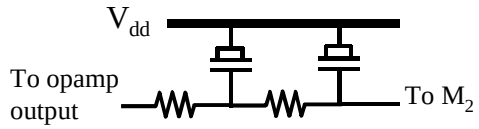

Figure 5: A simple 2nd order filter using MOSCAPs

4.3 Improving the settling time

As previously mentioned, the opamp was intentionally made slow in order to reduce the ripple present in the output current. The inevitable consequence of this choice is a longer time for the output of the opamp to settle to its final value. The long settling time has a major impact on the amount of time it takes for the circuit to start up. Once locked to its final value, the output should track slow changes in temperature.

In applications that require faster startup, the proposed circuit can be modified to achieve that without increasing the output ripple by including the filter (as shown in Fig. 4) and increasing the gain-bandwidth product of the amplifier.

5 Simulation results

The circuit of Fig. 1 was simulated using HSPICE with level 49 models for a 0.18µ CMOS process. The models were valid from –40 °C to 125 °C. By using a clock frequency of 20MHz, a V_{ref} of 1.25+V_{ss}, and a C_1 of 0.25pF, a reference current I_{ref} of 6.25µA was expected. Since a single-pole behavioral model was used to model the opamp, the possible temperature dependence of the amplifier is not represented in the results. Furthermore, since models for the temperature variation of poly-poly or metal-metal capacitors were not available, C_1 was modeled as temperature independent. However, the temperature dependence of these capacitors is expected to be small in practice.

The circuit was simulated at several points over a temperature range from –40 °C to 125 °C. As shown in Fig. 6, the current is very stable over the entire temperature range. The maximum deviation from the midpoint current value is 0.029%.

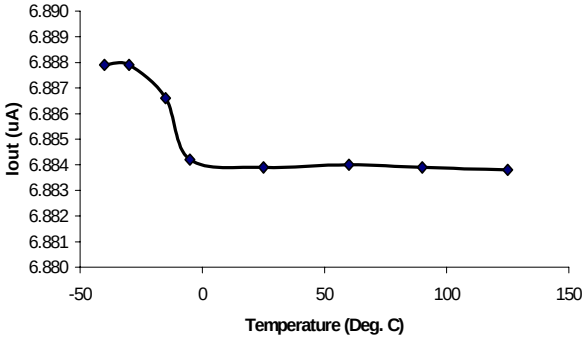

Figure 6: Average output current vs. Temperature

The actual value of the current obtained was approximately 6.88µA instead of 6.25µA. The reason for this discrepancy is the non-ideal nature of the virtual ground established at node 1 of Fig. 1. As shown in Fig. 2, the voltage at node 1 is non-zero despite having an approximate average value of 0. As mentioned in section 4.2, increasing the size of capacitor C_2, i.e., the ratio C_2/C_1, can reduce the voltage change on node 1. As the ripple on node 1 becomes smaller, a more accurate charge transfer from C_1 to C_2 takes place and the reference current approaches its intended value

6 Conclusions

A new temperature stable current reference was developed. The proposed circuit uses switched capacitor technique to establish the reference current. Simulation results show that the output current varies less than 0.029% over a temperature range of –40 °C to 125 °C.

Acknowledgments

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