Transfer Characterization of CMOS Ring Voltage Controlled Oscillators

Huiting Chen, Randall Geiger

Department of Electrical and Computer Engineering Iowa State University

Abstract-One of the most important properties of any voltage controlled oscillator (VCO) is the transfer characteristic, the relationship between the control voltage and the frequency of the output signal. In a voltage controlled ring oscillator, a number of identical delay stages are used. The most common delay stage is a delay cell with a pair of differential inputs and diode-connected loads paralleled with adjustable current sources. In this paper, a detailed analysis of the transfer characteristics based on the actual transistor operating regions is presented. It is shown that the relationship between the control voltage and the oscillation frequency is not monotonic. Simulation results verify the theoretical development. A design strategy is introduced that assumes that the VCO operates in the monotonic transfer characteristic region.

1. Introduction

Voltage controlled oscillators (VCO) are widely used in phase locked loop (PLL) and PLLs are widely used for frequency synthesis, data recovery in microprocessors and communication circuits. [1]-[7] One of the most common CMOS VCOs used in high-speed microprocessors and communication circuits are ring oscillators. Monolithic CMOS ring voltage oscillators have advantages in terms of relative high spectral purity (compared to relaxation oscillator), high frequency capability, large tuning range, good matching and low fabrication cost. Fig. 1 shows the block diagram of a ring oscillator. If the delay stage is single-ended inverter, the number of the stages is odd. If the delay stage is differential structure, the number of the stages can be even. Fig. 2 shows a commonly used delay cells.

In Fig. 2, a differential input structure with current source paralleled with diode-connected load is used to reduce the supply and ground noise. Two control voltages V_{biasn} and V_{biasp} provide large operation frequency tuning range. Diode connected

PMOS transistors provide fixed common mode and swing. One of the key properties of any VCO is the transfer characteristic, the relationship between the control voltage and the frequency of the output signal. Although the delay cell in Fig. 2 is widely used in the VCO design, the accurate transfer function has not been presented yet. Some designers thought the operation frequency is directly proportional to the control voltage V_{biasp}, while others thought that the operation frequency is reversal proportional to the control voltage V_{biasp}. In some applications, it is not required that the VCO has a linear relationship between operation frequency and control voltages. But for almost all the applications, the monotonic relationship between the frequency and the control voltage is necessary. This paper will provide a detail analysis about the transfer characteristic of the VCO. The results show that the transfer characteristic is not monotonic. A design strategy is introduced that assumes that the VCO operates in the monotonic transfer characteristic

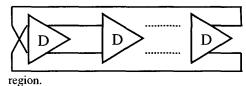


Fig.1: The block diagram of a ring VCO

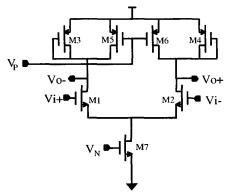


Fig. 2: Commonly used delay cell

In Section 2, the detailed analysis of the transfer characterization will be presented. The simulation results will be presented in Section 3. Finally, conclusions are made in Section 4 regarding this work.

2. Transfer Characterization of the CMOS Ring Oscillators

Voltage control ring oscillator is a nonlinear oscillator. The design and analysis of a nonlinear oscillator are complicated tasks, because transform methods (s-plane) cannot be applied directly. Nevertheless, like sinusoidal oscillators, the ring oscillators can be analysis by two steps. The first step is a linear one, and frequency-domain methods of feedback circuit analysis can be readily employed. Subsequently, a nonlinear mechanism for amplitude control can be provided. The operation frequency of the oscillator is determined in the first step, while the swing of the output signal is determined in the second step.

Fig. 3 is the behavior model of a ring VCO. Although in an actual oscillator circuit, no input signal will be present, an input signal here is included to help us analyze. Let $A_n(s)$ be the transfer function of one delay stage, and $A_t(s)$ is the transfer function of the n delay stages. $\beta(s)$ is the feedback factor. The closed loop transfer function $A_f(s)$ is

$$A_f(s) = \frac{A_f(s)}{1 - A_f(s)\beta(s)} \tag{1}$$

The loop gain of the circuit is defined

$$L(s) \equiv A_{\epsilon}(s)\beta(s) \tag{2}$$

The characteristic equation thus becomes

$$1 - L(s) = 0 \tag{3}$$

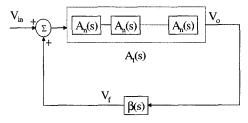


Fig. 3: The model of a ring oscillator

According to Barkhausen criterion, at the oscillation frequency ω_0 , the phase shift of the loop gain is 2π and the magnitude of the loop gain is unity. Thus the condition for the circuit in Fig. 3 to provide a stable oscillation at frequency ω_0 is that

$$L(j\omega_0) \equiv A_r(j\omega_0)\beta(j\omega_0) = 1 \tag{4}$$

In the ring oscillator case, $\beta(j\omega_0)=1$. To satisfy equation (4), we have that

$$A_{i}(j\omega_{0}) = |A_{i}(j\omega_{0})| \angle \phi = 1 \tag{5}$$

where $\phi = \angle A_i(j\omega_a)$, so that

$$\begin{aligned} |A_{r}(j\omega_{0})| &= 1\\ \phi &= 2\pi \quad or \quad \pi \end{aligned}$$
 (6)

For the delay cell shown in the Fig. 2, the transfer function is that

$$A_n(s) = \frac{v_o}{v_i} = -\frac{g_{m1}}{sC + 1/R}$$
 (7)

where g_{m1} is the transconductance of the differential input transistor, C is the total capacitance at the output node of the delay stage, R is the total resistance at the output node, so the total transfer function $A_i(s)$ is that

$$A_{t}(s) = \left(A_{n}(s)\right)^{n} = \left(-\frac{g_{m1}}{sC + 1/R}\right)^{n} \tag{8}$$

from equation (8), the amplitude and the phase of the transfer function A_i(s) can be expressed as

$$|A_{r}(j\omega)| = \left(\frac{g_{m1}}{C} \sqrt{\omega^{2} + \frac{1}{R^{2}C^{2}}}\right)^{n}$$

$$(9)$$

At the oscillation frequency ω_0 , the amplitude of the gain equals to unity and the phase shift ϕ is 2π or π , so the VCO operation frequency is

$$\left(\frac{g_{m1}}{C}\right)^n = \left[\sqrt{\omega_0^2 + \left(\frac{1}{RC}\right)}\right]^n \tag{10}$$

$$\omega_0 = \frac{1}{RC} \tan \left(\frac{2\pi}{n} \right) \quad or \quad \frac{1}{RC} \tan \left(\frac{\pi}{n} \right)$$

Equation (10) shows that the operation frequency is determined by the number of delay stages in an oscillator, the total capacitance and resistance at the output node of the delay stage. The total capacitance and resistance at the output nodes depend on the operating regions of transistors in a delay stage. These transistors will operate in three regions as the control voltage $V_{\rm biasp}$ changes. We will analyze the circuit in three cases:

Case 1: M5 and M6 are in the saturation region

Case 2: M5 & M6 are in the triode region

Case 3: M5 and M6 are in the cutoff region

Case 1: M5 and M6 are in the saturation region.

If all the transistors are in the saturation region, the input and output swing must be less than threshold voltage $V_{\rm th}$. So small signal model can be used in the analysis. The small signal model of the

half circuit of the delay cell is shown in Fig.4, and g_m

$$g_{m1} = \sqrt{\frac{2\mu_n C_{ox} w_1}{l_1}} I_1 = \sqrt{\frac{\mu_n C_{ox} w_1}{l_1}} I_{tail}$$
 (11)

$$I_{tail} = \frac{\mu_n C_{ox} w_7}{2l_7} (V_{biasn} - V_m)^2$$
 (12)

Substitute equation (12) into (11),

$$g_{m1} = \sqrt{\frac{\mu_n^2 C_{ox}^2}{2} \cdot \frac{w_1}{l_1} \cdot \frac{w_7}{l_7}} \cdot (V_{biasn} - V_m)$$
 (13)

Equation (13) shows that g_{m1} is proportional to the control voltage V_{biasn}.

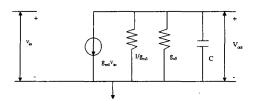


Fig .4: small signal of delay cell when all transistors operator at saturation region

From Fig. 4, the resistance and capacitance at the output node are shown in equation (14) and (15), respectively.

$$R = (1/g_{o5}) / (1/g_{m3}) \approx 1/g_{m3}$$
 (14)

$$C=C_{gd1}+C_{db1}+C_{gs3}+C_{bs3}+C_{gs5}+C_{bs5} \qquad (15)$$
 where g_{m3} is the transconductance of M3 and g_{o5} is

the conductance of M5.

$$g_{m3} = \sqrt{2 \frac{\mu_p C_{ox} w_3}{l_3} (I_{m1} - I_{m5})} = \sqrt{2 \frac{\mu_p C_{ox} w_3}{l_3} (\frac{I_{nail}}{2} - I_{m5})}$$
 (16)

where I_{m1} is the current of M1 and I_{m5} is the current

$$I_{m5} = \frac{\mu_p C_{ox} w_5}{2l_5} (V_{biasp} - V_{dd} - |V_{tp}|)^2$$
 (17)

Substitute equation (12) and (17) into (16

$$g_{m3} = \sqrt{2 \frac{\mu_p C_{ox} w_3}{l_3} \left[\frac{\mu_n C_{ox} w_7}{4 l_7} (V_{biasm} - V_m)^2 - \frac{\mu_p C_{ox} w_5}{2 l_5} (V_{biasp} - V_{dd} - |V_{pp}|)^2 \right]}$$
(18)

Finally substitute equation (19) into (10), the operation frequency of the oscillator is

$$\omega^{9} = \sqrt{2 \frac{10^{10} \text{Courte}}{h}} \left[\frac{\mu^{10} \text{Courte}}{Ahr}, \left(\frac{1}{\text{Misson-Visit}} \right)^{2} - \frac{10^{10} \text{Courte}}{2h}, \frac{1}{\text{Missin-Visit}} \right]^{2} \cdot \frac{1}{\text{Carter}} \left(\frac{2\pi}{h} \right)^{2} \cdot \left($$

Equation (19) shows that the oscillation frequency is directly proportional to control voltage V_{biasn} and V_{biasp} if all the transistors operate in the saturation region.

Case2: M5 and M6 are in the triode region

The transcondance of the input transistors gml is the same as that in Case 1, the total resistance at the output node is different. Consider the current through M1 (shown in Fig. 2) is

$$I = -\frac{\mu_{p} C_{ox} W_{3}}{2 L_{3}} \cdot \left[\left(V_{o} - V_{dd} \right) - \left| V_{pp} \right| \right]^{2} - \frac{\mu_{p} C_{ox} W_{5}}{L_{5}} \cdot \left[\left(V_{bianp} - V_{dd} - \left| V_{pp} \right| \right) \left(V_{o} - V_{dd} \right) - \frac{1}{2} \left(V_{o} - V_{dd} \right)^{2} \right]$$
(20)

So the small signal impedance r is

$$\frac{1}{r} = \frac{\partial I}{\partial V_o} = \frac{\mu_p C_{ox} W_3}{L_3} \left[V_{dd} - V_o + |V_{pp}| \right] + \frac{\mu_p C_{ox} W_5}{L_5} \cdot \left[\left(V_{dd} - V_{biasp} + |V_{pp}| \right) - \left(V_{dd} - V_o \right) \right]$$
(21)

let
$$W_3 = x \cdot W_5$$
 & $L_3 = L_5$

$$\frac{1}{r} = \frac{\mu_p C_{ox} W_5}{L_5} \left[\left(V_{dd} - V_{biasp} + \left| V_{tp} \right| \right) + (x - 1) \left(V_{dd} - V_o \right) + (x + 1) \cdot \left| V_{tp} \right| \right]$$
(22)

Substitute equation (22) into (10), the operation frequency of the oscillator is

$$\omega_{o} = \frac{1}{RC} \tan(\frac{2\pi}{n}) = \frac{1}{C} \cdot \tan(\frac{2\pi}{n}) \cdot \frac{\mu_{p} C_{ox} W_{5}}{L_{5}}.$$

$$\left[\left(V_{dd} - V_{biasp} + \left| V_{vp} \right| \right) + (x - 1) \left(V_{dd} - V_{o} \right) + (x + 1) \cdot \left| V_{vp} \right| \right]$$
(23)

Here, there are three cases.

(i): x=1, i.e., the active load is a symmetric load
$$\omega_o = \frac{1}{RC} \tan(\frac{2\pi}{n}) = \frac{1}{C} \cdot \tan(\frac{2\pi}{n}) \cdot \frac{\mu C_{ox} W_5}{L_5} \cdot \left[\left(V_{dd} - V_{biasp} + \left| V_{ip} \right| \right) + (x+1) \cdot \left| V_{ip} \right| \right]$$
(24)

The frequency is reversal proportional to the control voltage V_{biasp}.

(ii), x<1, i.e. the size of the diode-connected transistor M3 is smaller than that of the PMOS current source transistor M5

Because that V_{dd} - V_o is increased when V_{biasp} is increased, the frequency is also reversal proportional to the control voltage V_{biasp}.

(iii) x>1, i.e. the size of the diode connect transistor M3 is larger than that of the PMOS current source transistor M5

When V_{biasp} is increased, the first term in equation (24) is decreased, but the second term is increased, so the relationship of the frequency and the control voltage is undetermined.

Case3: M5 and M6 are in the cutoff region

In this case, equation (16) can be rewritten as

$$g_{m3} = \sqrt{\frac{\mu_p C_{ox} w_3}{l_3} I_{tail}}$$
 (25)

Substitute equation (12) into (25), than

$$g_{m3} = \sqrt{2 \frac{\mu_p C_{ox} w_3}{l_3} \left[\frac{\mu_n C_{ox} w_7}{2l_7} (V_{biasn} - V_{in})^2 \right]}$$
 (26)

The operation frequency of the VCO is given by

$$\omega_{0} = \sqrt{2 \frac{\mu_{p} C_{ox} w_{3}}{l_{3}} \frac{\mu_{n} C_{ox} w_{7}}{2 l_{7}} (V_{biase} - V_{m})^{2}} \cdot \frac{1}{C} \cdot \tan\left(\frac{2\pi}{n}\right)$$
 (27)

where n is the stage number of the VCO. So, the frequency of VCO is independent on the V_{biasp} .

3. Simulation Results

The analysis conclusions are verified by using Hspice simulator. The simulation results are based on $0.35~\mu m$ CMOS process.

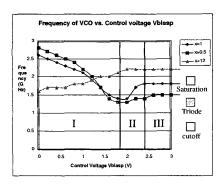


Fig. 5: Frequency of VCO vs. control voltage V_{biasp} where $x=W_3/W_5$.

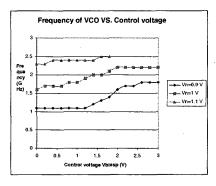


Fig. 6: Transfer Characterization of VCO (x=12)

Fig. 5 shows the relationship of the operation frequency of the VCO and the control voltage V_{biasp}. The simulation results show that, if the size of M5 and M6 is larger or equal to that of M3 and M4, the whole voltage control range can be divided into three part, In part I, the transistor M5 & M6 are in the triode region, and the operation frequency is reversal proportional to the controlled Voltage V_{biasp} . In part II, M5 & M6 are in the saturation region, and the operation frequency is directly proportional to V_{biasp}. In part III, M5 & M6 are in the cutoff region, and frequency is independent on the V_{biasp} . If the size of M5 and M6 is smaller than that of M3 and M4, the operation frequency will be directly proportional to control voltage V_{biasp} in the whole control voltage range. So in order to make the VCO have a monotonic relationship of the frequency and controlled voltage Vbiasp, careful design is required.

Fig. 6 shows the relationship of the oscillation frequency of the VCO and the control voltage V_{biasn} and V_{biasp} . This result shows that the oscillation frequency of the VCO is proportional to control voltage V_{biasn} . By Combining controlled voltage V_{biasn} and V_{biasp} , the VCO operation frequency tuning range will be from 1.1 GHz to 2.5 GHz at normal temperature and typical process.

4. Conclusion

Transfer characterization of VCO is studied in detailed. Unlike most designers believe that the relationship of the frequency and the control voltage is monotonic relationship, we find, the relationship is based on the design size and the operation region of the transistors. The Hspice simulation results verified the analysis results.

Refrences:

- [1]. M.Thamsirianunt and T. a. Kwasniewski, "CMOS VCO's for PLL frequency synthesis in GHz digital mobile radio communications," IEEE J. Solid-State Circuits, vol. 32, No. 10, oct.1997. p1511-1524.
- [2]. P. larsson, "A 2-1600-MHz CMOS clock recovery PLL with low-Vdd capability," IEEE J. Solid-State Circuits, vol. 34, No. 12, Dec. 1999. p1951-1960.
- [3] J. Craninchx, Michel S. J. Steyaert. "A 1.8-GHz CMOS Low-phase-noise voltage -controlled oscillator with prescaler," IEEE J. Solid-State Circuits, vol.30, No. 12, Dec. 1995. P1474-1482.

- [4]. S.Wang, R.Sheen, O T.-C. Chen and K.C. Tao, "A 1.8 V 900 MHz CMOS RF Receiver," ISCAS, 1998.
- [5]. M. Rau, T. Oberst, R. Lares, A. Rothermel, R. Schweer, and N. Menoux. "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE J. Solid-State Circuits, vol. 32, NO. 7, July 1997.
- [6] A. Djemouai, M. Sawan and M. Slamanni, "A 200 MHz Frequency-locked loop based on new frequency-to-voltage converters approach," ISCAS, 1999. II-89.
- [7] J. Parker and D. Ray, "A low -Noise 1.6 GHz CMOS PLL with on-chip loop filter," IEEE 1997 custom integrated circuits conference. P407-410.