Open Loop Pole Location Bounds for Partial Positive Feedback Gain Enhancement Operational Amplifiers

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Abstract--*For conventional op amps design open loop poles are usually in the left-half plane. For amplifiers with negative impedance gain enhancement the open loop pole is adjustable and it can be in the left-half plane or in the right-half plane. In this paper, we justify that it does not require a left-half plane open loop pole for designing a stable close loop amplifier. As a matter of fact, the amplifier exhibits both faster and more accurate settling when the open-loop pole is modestly in the right-half plane. New open loop pole bounds are derived for amplifiers with adjustable open loop pole to guarantee stability and to enhance settling time performance.*

INTRODUCTION

The negative impedance voltage gain enhancement technique, i.e., applying negative impedance at the output of the op amp to cancel its original positive impedance, has been around for quite a while [1,2,3,7]. Generally negative impedance is created by using an internal positive feedback loop. In the context of very low voltage circuits, this technique offers potential for overcoming some of the hurdles that are inherent in other more popular gain enhancement approaches. Although the negative impedance gain enhancement technique does have potential for simultaneously achieving very high DC open loop gain and high bandwidth, it has only received little attention.

The basic concept of the well-known gain enhancement technique by negative impedance compensation is shown in Fig.1. Negative resistor R_n is placed in parallel with the output impedance of the basic amplifier. It follows from the small signal equivalent circuit that the overall dc gain of the amplifier is

$$A_v = \frac{V_o}{V_i} = \frac{-g_{m1}}{g_{ds1} + 1/R - 1/R_n} \qquad (1)$$

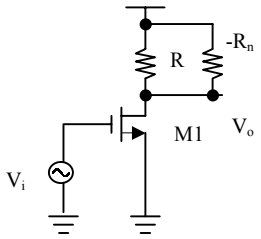

Fig. 1 Conceptual circuit of the negative impedance compensation technique

The overall output impedance will change as the value of negative resistor R_n varies. To achieve DC gain enhancement it is necessary to match the negative resistance R_n to the intrinsic resistance R_p at the output node.

$$R_p = R\,//(1/g_{ds1}) \qquad (2)$$

The relationship between the value of R_n and the overall dc open loop gain is shown in Fig. 2.

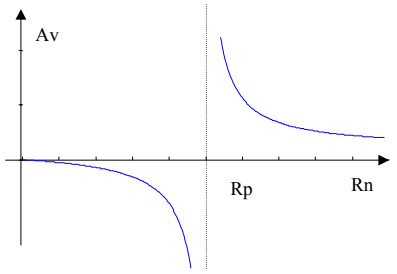

Fig. 2 DC open loop gain versus negative resistor R_n

If perfect cancellation occurs, i.e., R_n=R_p, the DC open loop gain of the circuit becomes infinity. In this case, the overall output impedance is infinite and the dominant pole is at the origin. If R_n>R_p, the DC open loop gain is enhanced by a factor of $1/(1-R_p/R_n)$. If R_n<R_p, the DC open loop gain of the circuit has a finite value but is negative. The overall output impedance is finite and negative and the dominant pole is in the right-half plane.

For conventional op amps design open loop poles are in the left-half plane. For amplifiers with negative impedance gain enhancement the

open loop pole is adjustable and it can be in the left-half plane or in the right-half plane.

Several researchers have applied the negative impedance compensation technique to achieve dc gain enhancement in CMOS op amps design [1-8]. However, there are two major concerns that limit this gain enhancement technique from being a popular application. The first concern is that excessive internal positive feedback can cause instability [3]. This is the case where $R_n<R_p$ and the amplifier has a dominant pole in the right-half plane. In a resent discussion of this technique, Gregorian [4] also suggested that a practical boosting of gain by 3 to 4 was possible to avoid a circuit with a right-half plane pole. Nevertheless, Gray [2] had previously observed that the right-half plane open loop pole is not of major concern since the feedback will actually move the close loop pole into the left-half plane. The second concern is metastability. When the amplifier has a right-half plane open loop pole it will have metastablity problem for open loop configuration. Since most high gain amplifiers are used in close loop configurations, as long as the external network provides enough negative dc feedback and moves the close loop poles into the left-half plane, metastability will not be a concern either.

In this paper, we will justify that it does not require a left-half plane open loop pole for designing a stable close loop amplifier. Open loop pole location bounds for amplifiers with the negative impedance compensation will be derived.

OPEN LOOP POLE LOCATION BOUNDS FOR PARTIAL POSITIVE FEEDBACK OP AMPS

Let A(s) denotes the transfer function of an amplifier with negative impedance compensation. Assume it is a first order system and its open loop transfer function can be written as

$$A(s) = \frac{A_0}{\frac{s}{p} - 1} = \frac{A_0 p}{s - p} \tag{3}$$

Where

$$A_0 = \frac{g_m}{g_x} \tag{4}$$

$$p = \frac{g_x}{c_L} \tag{5}$$

$$g_x = \frac{1}{R_p} - \frac{1}{R_n} \tag{6}$$

The open loop pole p is adjustable and it can be in the left-half plane or in the right-half plane. If $R_n>R_p$, the amplifier has open loop pole in the left-half plane; If $R_n<R_p$, the amplifier has open loop pole in the right-half plane. The product of A_0 and p is the gain-bandwidth product of the amplifier and it can be denoted as a constant K. Then the open loop transfer function of A(s) can be rewritten as

$$A(s) = \frac{K}{s - p} \tag{7}$$

Fig. 3 shows the signal flow graph of the close-loop configuration. If the feedback ratio is β, the close loop transfer function can be written as equation (8).

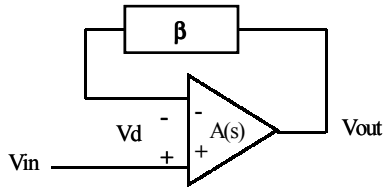

Fig. 3 Signal flow graph for close-loop configuration

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)} = \frac{K}{s - p + \beta K} \tag{8}$$

Then the close loop pole p_f can be written as

$$p_f = p - \beta K \tag{9}$$

The stability of the close loop amplifier will be determined by the location of the close loop pole p_f.

Case 1. A(s) has a LHP pole, i.e., $p < 0$
Since $\beta K > 0$
Then $p_f < 0$

The open loop amplifier is stable and the close loop amplifier is guaranteed to be stable.

Case 2. A(s) has a RHP pole, i.e., $p > 0$
Since $\beta K > 0$
Then $p_f < 0$ if $0 < p < \beta K$

The open loop amplifier is unstable while the close loop amplifier is stable if $0 < p < \beta K$.

The dc open loop gain of A(s) is plotted versus the open loop pole location in Fig. 4. The phase reversal occurs when the pole crosses the imaginary axis.

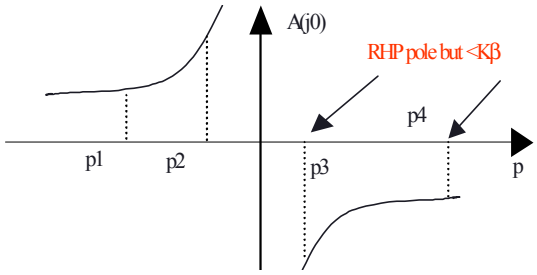

Fig. 4 Open loop dc gain versus open loop pole location

Fig. 5 shows the relationship between the dc gain of the close loop amplifier and the open loop pole p. The close loop gain is exactly 1/β when the open loop pole is at the origin. The close loop amplifier remains stable provided the open loop pole is less than βK. When an amplifier with negative impedance compensation is designed, the open loop pole should be designed within the region around origin to achieve high dc gain. Since this region is far from βK so the close loop amplifier is stable.

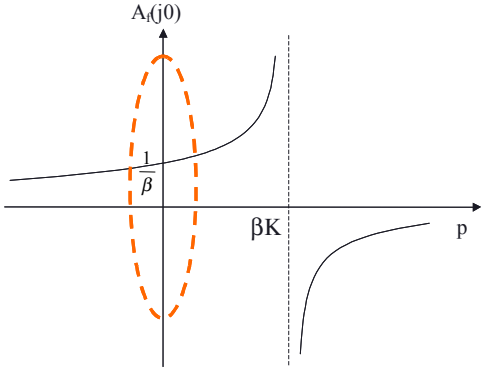

Fig. 5 Close loop dc gain versus open loop pole location

The transient response of the close loop amplifier is an important design objective. The typical criterion to evaluate this behavior is the step response. The unit step response for an over-damped system is shown in Fig. 6. The settling time t_s is defined as the time required to settle within the settling windows which are depicted by the (1+ε) and the (1-ε) bounds around the ideal value of 1/β where ε is the settling accuracy and is determined by application requirement.

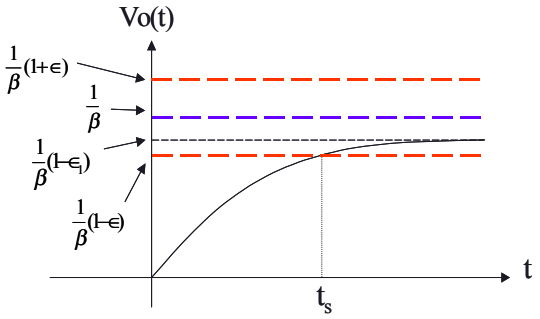

Fig. 6 Unit step response for over-damped system

For accurate settling, the close loop dc gain should meet the inequality

$$\frac{1}{\beta}(1-\varepsilon_1) < A_f(j0) < \frac{1}{\beta}(1+\varepsilon_1) \qquad (10)$$

This is equivalent to the inequality for open loop pole p

$$-\frac{\varepsilon_1 K\beta}{1-\varepsilon_1} < p < \frac{\varepsilon_1 K\beta}{1+\varepsilon_1} \qquad (11)$$

$$p_{\min} = -\frac{\varepsilon_1 K\beta}{1-\varepsilon_1} \qquad (12)$$

$$p_{\max} = \frac{\varepsilon_1 K\beta}{1+\varepsilon_1} \qquad (13)$$

Inequalities (12) and (13) establish new bounds for the open loop pole. The open loop pole of an op amp with negative impedance gain enhancement should be designed within the bounds given in (12) and (13) to guarantee stability and to enhance settling time performance.

The unit step response of the close loop amplifier $A_u(t)$ can be found by taking the inverse Laplace transform of $A_u(s)$.

$$A_u(s) = A_f(s).\frac{1}{s} \qquad (14)$$

$$A_u(t) = \frac{K}{(\beta K - p)}(1-e^{-(\beta K-p)t})u(t) \qquad (15)$$

For different open loop pole locations shown in Fig. 4, the corresponding unit step response is shown in Fig. 7. The amplifier with an open loop right-half plane pole p3 exhibits both faster and more accurate settling. Expression 15 and Fig. 7 indicate that the amplifier shows both faster and more settling when the open-loop pole is designed modestly in the right- half plane.

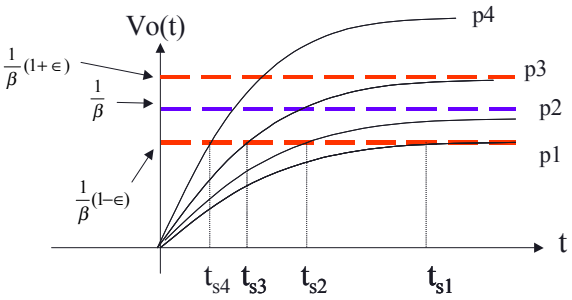

Fig. 7 Step responses

CONCLUSION

This paper justifies that the right-half plane open loop pole is generally not a major concern when designing an amplifier for close loop application. Moreover, the amplifier exhibits both faster and more accurate settling when the open-loop pole is modestly in the right-half plane. New open loop pole bounds are derived for amplifiers with adjustable open loop pole to guarantee stability and to enhance settling time performance.

REFERENCES

[1] D. Allstot, "A Precision Variable Supply CMOS Comparator", *IEEE J. Solid-State Circuits*, Vol. SC-17, pp 1080-1087, Dec.1982.

[2] C. Laber and P. Gray, "A Positive Feedback Transconductance Amplifier with Applications to High-Frequency, High-Q CMOS Switched-Capacitor Filters", *IEEE J. Solid-State Circuits,* Vol. SC-23, pp. 1370-1378, Dec. 1988

[3] E. Wang and R. Harjani, "Partial Positive Feedback for gain Enhancement of Low-Power CMOS OTAs", Analog Integrated Circuits and Signal Processing, 8, pp21-35, 1995

[4] R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*, Wiley Interscience, New York, 1999.

[5] B.Nauta and E.Seevinck, "Linear CMOS transconductance element for VHF filters", *Electron.Lett*., 1989, 25, pp448-450

[6] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies", *IEEE J. Solid-State Circuits*, vol. 27, No.2, pp142-153, Feb. 1992.

[7] S. L. Wong and C.A.T. Salama, "Voltage gain enhancement by conductance cancellation in CMOS op amps", *ISCAS' 1984*, pp1207-1210.

[8] J. Yan and Randall Geiger, "Fast-Settling CMOS Operational Amplifier with Negative Conductance Voltage Gain Enhancement", *Proceedings of 2001 IEEE International Symposium on Circuits and Systems*, Volume 1, pp228 –231, May 2001