Accurate Self Characterization and Correction of A/D Converter Performance*

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Abstract

A new algorithm based on a code density test to measure Integral Non-linearity (INL) of Analog-to-Digital (A/D) converters is introduced. This algorithm uses as an input two related but unknown 'ramp-like' signals that can be practically generated on-chip and the corresponding code-density histogram. The algorithm inherently characterizes both the A/D converter and the inconsequential input. This algorithm finds applications in Self-calibrating A/D converters as well as providing capability for Built-In Self-Test, where generation of an on-chip ramp input test signal of 8bits accuracy or more is a challenge.

I. Introduction

Over the past decade, the semiconductor industry has witnessed a reduction in the average cost of ICs. With the emergence of advanced technologies, the cost of IC production has drastically reduced, thereby placing an upper bound on the testing cost during production. With the cost of silicon in many Data Converter products becoming increasingly dominated by testing costs, Built-In Self-Test (BIST) structures offer potential for not only reducing the direct cost associated with testing, but also reducing the indirect cost associated with production time. This requires test schemes suitable for implementation as BIST structures whose performance parallels the results obtained from conventional testing methods.

Several different parameters are widely used to characterize Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters. In what follows, the two main static parameters of the A/D converter, namely Integral Non-linearity (INL) and Differential Non-linearity (DNL), are being considered and test schemes suitable for BIST implementation are described.

The traditional method for linearity measurement of an A/D converter is the code density test [1],[2],[3],[4]. A periodic signal with a known probability density function (pdf) is converted by an A/D under test at sampling times that are not synchronous with the input signal. The histogram obtained at the output is then compared to the ideal expected value and the difference is used as a measure of the converter non-linearity. For example, with a linear ramp input signal, the number of occurrences for each code (bin) should ideally be equal and variations correspond to both DNL and INL errors. Differential non-linearity is the deviation from one least significant (LSB) of the range of input voltages that give the same output code. The total number of samples *(N)* divided by the number of bins (2^B, where 'B' is the number of bits of the converter under test), gives the number of codes per bin, *P(i)*, for an ideal converter. The number of samples in the i^{th} bin divided by ideal number of samples (P(i)) gives a measure of differential linearity and the difference from unity refers to the differential non-linearity. For a monotonic A/D converter, Integral non-linearity of any code can then be obtained by the summation of DNL of all codes below it.

$$INL_i = \sum_{j=0}^{i} DNL_j \qquad (1)$$

Though this scheme works fine conceptually, it relies on the generation of a ramp signal at the input that must be substantially more linear than the A/D converter under test. Any substantial non-linearity or distortion in the ramp will change the expected number of codes in each bin. Determining the expected number of codes then requires an accurate characterization of the non-linear input signal. For most existing proposed BIST structures, a ramp is usually generated by charging a capacitor with a constant current source. This method is limited by the non-idealities of the current source. Finite output impedance of practical current source limits the accuracy of the ramp to 7~8 bits. Even though more complex schemes to improve current source output impedance and to generate a more linear ramp have been described in literature, the problem is still not completely eliminated.

In this paper, a modified histogram test is described which takes in multiple "ramp-like" inputs and gives multiple histograms as output. These outputs are then used to characterize both the A/D converter under test and the inconsequential input signal.

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II. System Identification Concept

Let **H** be the transfer characteristics of the A/D converter under test and **I** be the modifying function which generates a 'ramp-like" signal from a perfect ramp (V_{in}). The output of the converter is then related to the input as:

$$V_{out} = \mathbf{H}(\mathbf{I}(V_{in})) \quad (2)$$

It can be shown that for some fixed relationships between **H** and **I**, it is impossible to determine **H** from histogram outputs for any number of inputs. For example,

$$\text{If} \quad \mathbf{H}=\mathbf{I}^{-1}, \quad (3)$$

$$V_{out} = V_{in} \quad (4)$$

and hence, no additional information about **H** or **I** can be obtained from the output histogram.

For practical **H** and 'ramp-like' **I**, it is possible to determine **H** from histogram outputs for two related inputs. Specifically, if **H** and **I** have different spacial spectral distributions, then by using multiple inputs, sufficient information to characterize the system (both **H** and **I**) is available in the histogram outputs.

III. Algorithm

Though many algorithms may exist that can be used to identify **H** and **I**, one particular scheme aimed at Flash A/D converters is described here. The test procedure consists of the following steps:

1. A 'ramp-like' input (*I1*) is given and the output histogram H1 is obtained.
2. A related input (*I2*), obtained by shifting *I1* by a fixed number of LSBs (here 1LSB) is given as a second input and the output histogram H2 is obtained.

H1 & H2 are used to determine the A/D converter and input signal characteristics as explained below:
For sake of simplicity, the algorithm is explained using a 2-bit converter as a reference. Consider the transfer characteristics of an A/D converter as shown in Figure.1.

The various notations that are used are:

- I_i -> i^{th} transition level of Ideal ADC.
- T_i -> i^{th} transition level of actual (non-ideal) ADC.
- Δ_i -> deviation of i^{th} transition level (T_i) from ideal transition level (I_i).
- I1 -> 'ramp-like' input signal.
- I2 -> I1 shifted by a known amount (1LSB here).
- C_i -> Number of samples in i^{th} bin for ideal ADC and 'ramp-like' input (I1).
- C_i' -> Number of samples in i^{th} bin for actual ADC and 'ramp-like' input (I1).
- C_i'' -> Number of samples in i^{th} bin for actual ADC and input I2.

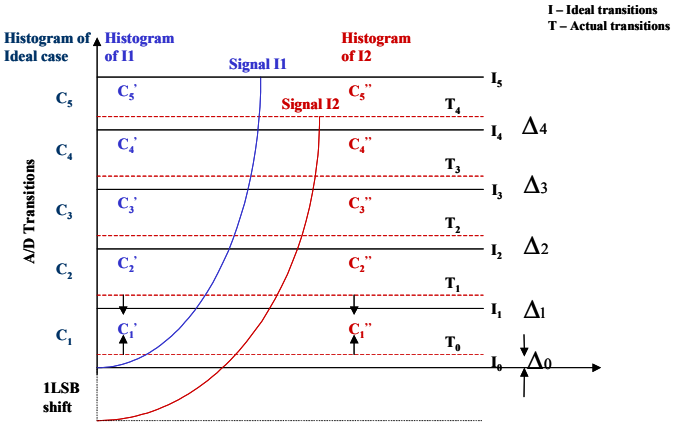

Figure.1. A/D Transfer Characteristics with Input signals and Histogram values

Note that Δ_0 refers to deviation of 0^{th} transition. In reality, there exists no 0^{th} transition. Δ_0 has been introduced to obtain a simpler mathematical representation of the algorithm. The values of C_i' and C_i'' are obtained from H1 and H2 respectively. The equations relating the various bin values and the delta values (in terms of number of samples) are :

$$C_1' = C_1 + \Delta_1 - \Delta_0 \quad (5)$$
$$C_2' = C_2 + \Delta_2 - \Delta_1 \quad (6)$$
$$C_3' = C_3 + \Delta_3 - \Delta_2 \quad (7)$$
$$C_4' = C_4 + \Delta_4 - \Delta_3 \quad (8)$$
$$C_1'' = C_2 + \Delta_1 - \Delta_0 \quad (9)$$
$$C_2'' = C_3 + \Delta_2 - \Delta_1 \quad (10)$$
$$C_3'' = C_4 + \Delta_3 - \Delta_2 \quad (11)$$
$$C_4'' = C_5 + \Delta_4 - \Delta_3 \quad (12)$$

The above equations are obtained with the assumption that even though the input signal is not a linear ramp, for a small segment consisting of adjacent LSBs, the signal is linear to first order.

The variables to be determined are
$\{C_1, C_2, C_3, C_4, C_5, \Delta_0, \Delta_1, \Delta_2, \Delta_3, \Delta_4\}$

The total number of unknowns is '10' and number of equations available is '8'. Hence, the system seems to be under-specified. An assumption of $\Delta_0=\Delta_1=0$ is made. As explained earlier, since Δ_0 is being introduced to simplify the mathematics, the assumption of it being '0' is valid. $\Delta_1=0$ implies that the first transition is perfect ($DNL_1=0$). Any error in the first transition will manifest itself as gain error that can be corrected separately and hence the assumption of $\Delta_1=0$ is also valid.

The Equations 5-12 are simplified to get the delta values as shown below:

$$\Delta_{i+1} = C'_{i+1} - C''_i + 2\Delta_i - \Delta_{i-1};\ \text{i}\ \varepsilon\ \{1\ \text{to}\ 2^{\text{Bits}}-1\} \tag{13}$$

where, $\Delta_0=\Delta_1=0$.

Once the Δ values are available, the values of C_i can be obtained which can then be used to characterize the input signal.
The deviations of A/D transitions in terms of LSBs is then given by

$$\Delta_{LSB}(i) = \frac{\Delta(i)}{C(i)} \tag{14}$$

DNL for any code is calculated using the following equation,

$$DNL_i = \Delta_{LSB}(i) - \Delta_{LSB}(i-1);\ \text{i}\ \varepsilon\ \{2\ \text{to}\ 2^{\text{Bits}}\} \tag{15}$$

and INL from Equation(1).
The INL thus obtained is then corrected for gain and offset error mathematically.

IV. Simulation Results

A complete MATLAB simulation was performed to test the proposed algorithm and results are summarized below. A 10bit flash A/D converter with a unit resistance value of 'R' was considered. Each of the resistors in the string (except the 1st one) was varied randomly between +/-10% following a uniform distribution. Any variation in the value of 'R' results in variation of the corresponding trip point of the A/D converter. Also, owing to the nature of the string architecture, the deviation of any trip point 'i' does not only depend on resistance R_i but also on the values of all resistance from '0' to 'i-1'.
A 'ramp-like' input was generated in matlab using the following function

$$\text{Vin} = \alpha_1 V + \alpha_2 V^2 \tag{16}$$

Where, α_1 and α_2 are two constants. Vin is a linear ramp if $\alpha_1=1$ and $\alpha_2=0$. A small amount of non-linearity was introduced by choosing the values of α_1 =0.95 and $\alpha_2=0.05$. The number of samples per LSB was chosen to be 100. It is assumed that the second signal is shifted exactly by 1LSB (*shift* = 1LSB). The case when the '*shift*' is not equal to 1LSB is considered later. Figure.2. shows the plot of INL values that was actually introduced in matlab to simulate a non-ideal ADC, and the INL values that was calculated using conventional histogram method and that using the new algorithm. As seen from the graph, the INL predicted by new algorithm follows closely the value that was actually introduced in Matlab. The plots almost overlap each other, indicating that the new algorithm gives nearly accurate results. On the other hand, the INL obtained by using the conventional histogram approach differs considerably, due to non-linear nature of the input signal. Once the errors in transition voltages are estimated by using the new algorithm, it can be used to correct the ADC. The INL profile, after correcting the transition values based on results obtained from the new algorithm is also given in Figure.2. It can be seen that, after correction, the INL of the residual transfer characteristics reduces to very small value (within 0.06LSB). The process of estimation and correction can be repeated until the A/D converter is completely corrected.

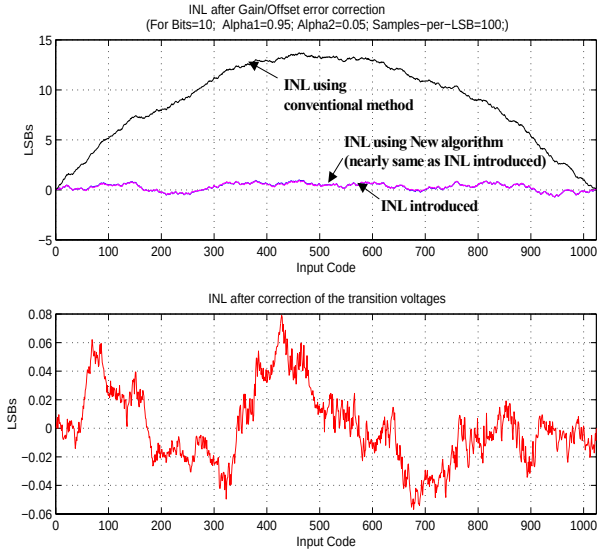

Figure.2. – Plot of INL for 10bit converter with 100 Samples per bin and second input obtained by exact 1LSB shift

To consider the effect of the Number of Samples per LSB on the performance of the new algorithm, another

simulation with the same parameter as in the previous case (Bits=10, α_1=0.95, α_2=0.05), but Samples-per-LSB equal to 250 was performed and the result is given in Figure.3. It can be seen from the graph that the INL after correction reduces to less than 0.02LSB. This is because, the more the number of points, the better the approximation as we move towards continuous input case.

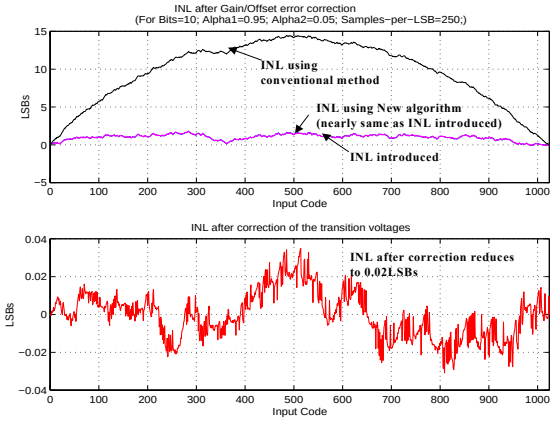

Figure.3. Plot of INL for 10bit converter with 250 Samples per bin and second input obtained by exact 1LSB shift

The results given above are under the assumption that a perfect shift of 1LSB is achievable. But in reality, this may vary by 10%. Another simulation,, in which the second input signal (*I2*) is shifted by 0.9LSB instead of 1LSB was performed. The algorithm is unchanged, since it assumes the shift to be 1LSB. Figure.4. shows the INL introduced and that calculated using conventional and new algorithm. As expected, the result differs from Figure.2., but still is better than conventional case.

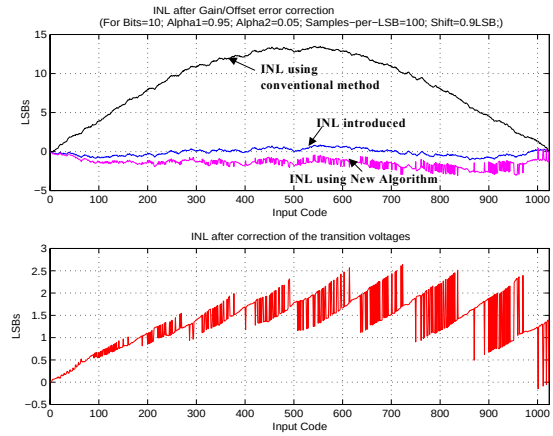

Figure.4. Plot of INL for 10bit converter with 100 Samples per bin and second input obtained by 0.9LSB shift

V. Conclusion

A new algorithm for characterizing the Integral Non-linearity (INL) of a Flash A/D converter has been described. The proposed algorithm is suitable for Built-In Self-Test (BIST) application, where on-chip generation of an input ramp of more than 7~8 bit accuracy is difficult. Unlike the conventional histogram approach, the new algorithm does not require a linear ramp as input. Simulations results for a 10bit A/D converter has been provided to confirm the functionality of the algorithm. It is conjectured that the multi-input/multi-histogram approach has applications to pipelined structures that may give even better results in either foreground or background test/calibration schemes.

REFERENCES

[1] Doernberg, J., Lee, H.-S., and Hodges, D.A.: *Full-Speed Testing of A/D Converters,* IEEE J. Solid-State Circuits, December 1984, SC-19, pp.820-827.

[2] Ginetti B., Jespers, P. *Reliability of Code Density Test for High Resolution ADCs,* Electronics Letters, Vol.27, pp.2231-2233, Nov.21, 1991.

[3] J. Blair, *Histogram measurement of ADC nonlinearities using sine waves*, IEEE Trans. Instrum. Meas., Vol.43, pp.373-383, June 1994.

[4] Kuyel, T., *Linearity Testing Issues of Analog to Digital Converters*, Test Conference, 1999. Proceedings, International, 1999, Page(s): 747-756