

Technique to Eliminate Slow-Settling Components that Appear Due to Dipoles

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Abstract – Due to their low-voltage compatibility and potential for high-speed operation, multipath compensated amplifiers offer potential for implementation in low-voltage processes. They are not practical for high-speed applications yet because they have low frequency dipoles which result in slow-settling components appearing in the transient response. This work outlines a self-calibration methodology that attempts to extend the performance of multipath compensated amplifiers into the high-speed realm by ensuring pole-zero cancellation to a certain degree of accuracy.

I INTRODUCTION

Amplifier topologies commonly used for charge transfer circuits are the telescopic cascode, folded cascode, and regulated cascode amplifiers. Their widespread adoption is due to the fact that they offer the ability to simultaneously achieve fast settling along with a large DC gain. However, these topologies rely upon stacking several devices between the voltage rails to achieve their large DC gains. For a given signal swing requirement, device stacking increases the minimum supply voltage the amplifier requires for operation.

As fabrication technology progresses to finer feature sizes, reductions in power supply voltage are required. Each reduction in supply voltage makes the cascoded structures less and less viable. At some point in the near future, barring the use of depletion devices or low- V_T transistors which are not normally available in a digital process, the realization of functional cascoded amplifiers will not be possible at all.

At that point in time, alternative amplifier architectures that are capable of operating at lower minimum supply voltages will be required. Cascading gain stages to achieve a multistage amplifier with a large DC gain is one technique that is compatible with low-voltage supplies. So far, multistage amplifiers consisting of more than two stages have found limited adoption due to the difficulty associated with compensating the amplifier to ensure stability when used in a feedback configuration.

Multistage amplifier compensation schemes [1][2][3][4] that offer combinations of speed and DC gain that rival those of the cascoded structures have not

yet been demonstrated. One compensation technique [5] has the potential to operate at high speeds with large DC gains but requires accurate pole-zero cancellations to prevent the appearance of slow-settling components in the transient response. Practical implementations of [5] have not appeared because circuit implementations that intrinsically ensure accurate pole-zero cancellation over process and environmental variations are not available. Despite the lack of intrinsic methods to ensure accurate cancellation, the technique can be implemented using a calibration routine that periodically recalibrates the circuit to ensure cancellation to a specified level of accuracy occurs. In this work, a method for implementing the required calibration for a two-stage amplifier is introduced. Later the idea can be extended to amplifiers with a larger number of gain stages.

A brief review of the multipath compensation technique is included in section II. The new compensation technique is introduced in section III and a few practical implementation issues are addressed in section IV.

II BRIEF REVIEW OF MULTIPATH COMPENSATION

Fig. 1 shows the frequency-domain block diagram of an n -stage multipath compensated amplifier. Each of the rectangular blocks represents a first-order low-pass transfer function of the form:

$$G_k(s) = \frac{A_k}{1 - s/P_k} \quad (1)$$

The system is referred to as a *multipath* system because there are multiple signal paths through the amplifier. The existence of n signal paths through the amplifier introduces $n-1$ zeros in the overall system transfer function. Prudent selection of the stage gains (A_k 's) and pole locations (P_k 's), the details of which can be found in [5], allows the multipath-induced zeros to cancel system transfer function poles. The result is an n -stage amplifier that exhibits a near first-order response.

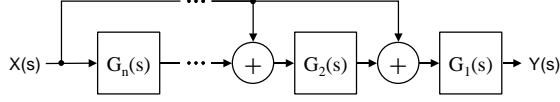


Fig. 1 Block diagram of a multipath amplifier

Fig. 2 shows the closed-loop pole and zero locations in the complex s -plane for an n 'th order multipath amplifier used in a standard feedback configuration. If perfect cancellation were possible, the system would be exactly first-order. Practically, mismatch will always exist and the system only approximates a first-order response.

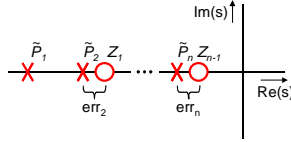


Fig. 2 Closed-loop pole and zero locations for an n 'th order multipath amplifier

Imperfect cancellation of the pole-zero pairs (dipoles) results in the appearance of extra decaying exponential components in the transient response. These additional components will decay more slowly than the desired component because they lie at lower frequencies than the *uncovered* pole.

If the magnitudes of the mismatches are small, the magnitudes of the undesirable components are also small. However, if the mismatches are large, the sizes of the undesired components are also large. Unfortunately, accurate pole-zero cancellation is not easy to ensure due to modeling errors, process variation, and environmental factors. For this reason, for applications that require fast settling, amplifiers with low frequency dipoles are avoided.

This work is an effort to extend the applicability of these structures to applications that require fast settling through the use of a calibration technique that ensures that the magnitudes of the undesired components remain small.

III CALIBRATION TECHNIQUE

The general case of calibrating an n -stage amplifier is a complicated problem. Initially the simplified case of a two-stage amplifier will be considered. In later work, the concept will be extended to amplifiers with more than two stages.

The switched capacitor gain stage shown in Fig. 3 was constructed with a two-stage multipath amplifier. If the low-frequency pole-zero pair cancels exactly, the

system will exhibit a first-order step-response like that shown in Case B of Fig. 4. No overshoot occurs. The response is a standard exponential charging from zero to the final steady-state output value.

Cases A and C of Fig 4 illustrate the effect of pole-zero mismatch on the step-response. Cases A and C correspond to the scenarios where the low-frequency pole lies on the real axis to the left and to the right of the zero respectively. Notice that when the low-frequency pole lies to the left of the zero, overshoot occurs, whereas when the pole lies to the right of the zero, undershoot occurs.

The sensitivity of the step response to the dipole mismatch can be exploited to obtain a signal that is roughly proportional to the pole-zero mismatch. This error signal can be utilized to calibrate the amplifier.

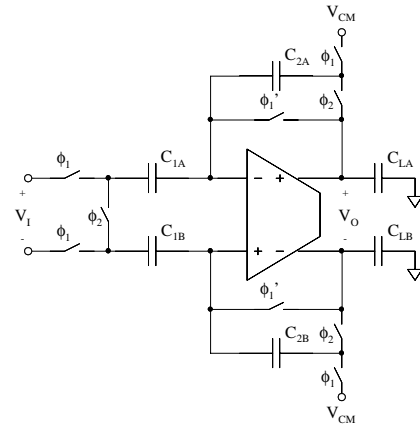


Fig. 3 Switched capacitor gain stage

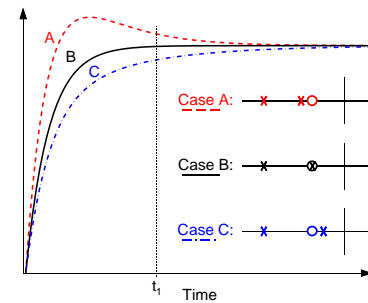


Fig. 4 Step responses for multipath amplifiers with varying degrees of pole-zero mismatch

The technique involves sensing the slope of the step response after a delay that is several times longer than the time constant of the high-frequency pole but still shorter than the time constant of the low-frequency pole. For example, consider value of the derivatives of the responses shown in Fig. 4 at time t_1 . As evident

from the figure, a negative slope indicates that the pole lies to the left of the zero while a large positive slope indicates the pole lies to the right of the zero. The mismatch information can be used to adjust an amplifier bias current and the measure/adjust process can be repeated to perform the calibration.

A. Slope Measurement

One method for sensing the slope is to use a RC-based differentiator circuit. Although conceptually elegant, this method does not work well in practice because the signals we are trying to differentiate are very fast. The RC differentiator exhibits a sensitivity/speed tradeoff. Reducing the time constant of the differentiator increases its bandwidth and improves its ability to respond to fast changing signals. However, reducing the time constant also reduces its gain which limits its sensitivity. As a result, the RC differentiator is unsuitable for this application.

As an alternative approach, a sampling scheme can be used. The waveforms shown in Fig. 5 illustrate the concept.

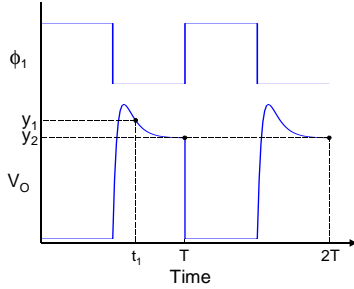


Fig. 5 Sampling scheme used to detect incomplete settling

The circuit is excited with a step input large enough to achieve a full-scale output swing. Fig. 5 shows two cycles of an output voltage swing from a hypothetical amplifier that has a large pole-zero mismatch. An inter-period sample, y_1 , is taken at time t_1 and compared to the settled value, y_2 , at time T . If $y_2 - y_1 > 0$, it is deduced that the low-frequency pole lies to the left of the zero. Conversely, if $y_2 - y_1 < 0$, the pole is assumed to lie to the right of the zero.

Unfortunately, obtaining the inter-period sample disturbs the settling, affecting the value of V_O at time T . Sampling this disturbed value would introduce an error. To avoid this problem, the system is excited with a periodic step input and the settled-value y_2 is measured at the end of the subsequent cycle, at time $t = 2T$.

The sample noise present in the samples y_1 and y_2 limits the ability to resolve an underdamped system

from an overdamped one. Averaging the difference $y_1 - y_2$ over many measurement cycles reduces the effects of random sample noise improving the resolution of the overall system.

Fig. 6 shows the block diagram of the overall system in calibration mode. The switched capacitor gain stage constructed with a two-stage multipath amplifier is excited to elicit periodic full-scale step responses. Fig. 7 shows the schematic diagram of the switched-capacitor integrators I1 and I2.

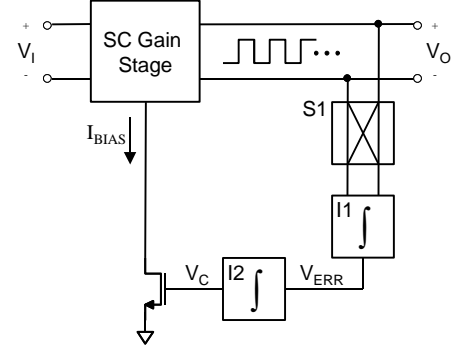


Fig. 6 Block diagram of system under calibration

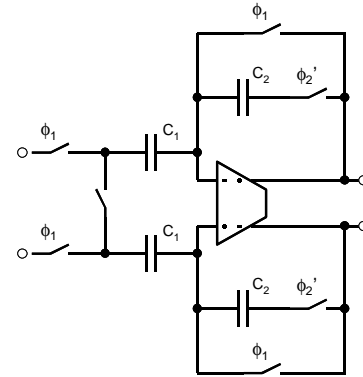


Fig. 7 Switched-capacitor integrator schematic diagram

The butterfly switch S1 and the switched capacitor integrator I1 are used to develop the averaged value of $y_2 - y_1$ over N measurement cycles. To perform the computation, switch S1 toggles integrator I1's input polarity every cycle so that for even cycles V_O is applied to I1 and for odd cycles $-V_O$ is applied. I1 is clocked to integrate an inter-period sample of the output voltage during even cycles (y_2) and an end-of-period sample during odd cycles (y_1). The result is that during even cycles the output of I1 is charged up by an amount proportional to y_2 and during odd clock cycles, charged down by an amount proportional to y_1 . The residual charge left on the output node is proportional to the desired quantity $y_2 - y_1$.

To reduce the effects of random sample noise, V_{ERR} is allowed to accumulate over N clock cycles before the switched capacitor integrator I2 is triggered to adjust the value of a control voltage based on the instantaneous value of the error voltage. During the adjustment of V_C , V_{ERR} is reset so the entire process can be repeated.

IV IMPLEMENTATION ISSUES

One implementation issue that has to be dealt with is that high-gain transconductance amplifiers are not available to realize high-quality integrators. The finite gain of the amplifiers limit the accuracy of the charge transfer operations and therefore limit the overall accuracy of the post-calibration pole-zero cancellation.

Considering the finite gain effects but neglecting amplifier offset, the charge delivered per cycle to C_2 , $Q[n]$, for the integrator shown in Fig. 7 is given by:

$$Q[n] = (1-k)C_1V_{in}[n] - kC_2V_{out}[n-1] \quad (2)$$

where $k = 1/[C_1 + (A+1)C_2]$. For large A , k approaches zero and the charge transferred each cycle is the desired value of $C_1 \cdot V_{in}$. However, for smaller DC gains, k becomes nonzero. As a result, due to the second term, the amount of charge actually delivered is slightly affected by the previous output voltage held by the integrator.

This is problematic because it leads to an undesired drift in the output voltage which can be incorrectly interpreted as a pole-zero mismatch. Fig. 8(a) illustrates the output voltage of integrator I1 for y_1 - y_2 phasing described in section III. The positive transitions are due to the integration of inter-period measurements (y_1 's) while the negative transitions are due to the end-of-period measurements (y_2 's). The desired output quantity $y_1 - y_2$ is available after the $-y_2$ transition is complete. As illustrated in Fig. 8(a), the output voltages preceding the y_2 transitions are always positive and larger than the voltages preceding the y_1 transitions. Due to the second term in (2), the y_1 and y_2 related charge transfers are not exactly equal. Despite the fact that $y_1 = y_2$, a systematic output drift occurs which can incorrectly be interpreted as a pole-zero mismatch.

Modifying the order of the charge add-subtract operations can lessen the sensitivity to the finite gain of the amplifiers and diminish the resultant output drift. Use the y_1 - y_2 - y_2 - y_1 sequence illustrated in Fig. 8(b) rather than the y_1 - y_2 sequence. Notice that the output voltages preceding one of the y_1 and one of the y_2

transitions are large in magnitude. Therefore, the errors due to the second term of (2) can be significant. However, due to the fact that the output voltages preceding those transitions differ in polarity, their effects offset each other reducing the problems with output drift. The voltages preceding the other two transitions are generally small and therefore according to (2) result in smaller errors.

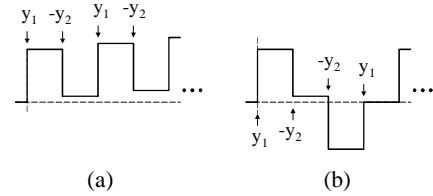


Fig. 8 Integrator output voltage waveforms for (a) y_1 - y_2 sequence and (b) y_1 - y_2 - y_2 - y_1 sequence

Offset voltage in the integrator's transconductance amplifier can lead to a static pole-zero mismatch. Therefore, integrator architectures that include offset compensation are required.

V SUMMARY

In an effort to extend multipath compensated amplifiers into the high-speed realm, a self-calibration methodology was outlined that ensures that the magnitudes of slow-settling components that occur due to incomplete cancellation of low-frequency pole-zero pairs stay bound below a certain level.

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