# Resistor Layout Techniques for Enhancing Yield in Ratio-Critical Monolithic Applications

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## Abstract

*A new strategy for the layout of integrated resistors that minimizes yield loss due to random sheet resistance variations for a given area in ratio-critical applications is introduced. The strategy is based upon the optimal partitioning of area between the resistors that must be ratio-matched and on the practical realization of the partitioned resistors with unit resistor cells. This strategy provides substantial improvements in yield over what is achievable with most existing layout strategies when large and accurate resistor ratios are required.*

## Background

It is well recognized that layout plays a key role in the yield of matching-critical circuits and techniques such as using segmented devices in a common-centroid layout are widely used [1-3] to improve resistor ratio-matching accuracy. Placement and segmentation in conjunction with centroiding can be used for minimizing the effects of first and higher-order gradients induced by process

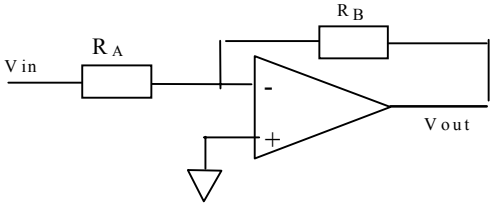


Fig. 1 Basic Inverting Amplifier

parameter variations, mechanical stress, temperature or other factors. But in precision applications where sufficiently large areas are used to make the local random mismatch effects area-dominant, the standard deviation of the current in two closely placed identical transistors [4], [6] or the standard deviation of the relative resistance or capacitance of two closely placed resistors or capacitors [4], [5] varies with the reciprocal of the area of the devices. Although there has been considerable effort devoted to statistically characterizing the matching of nominally identical transistors, resistors or capacitors, little attention has been devoted to characterizing the ratio-matching accuracy of these devices or, correspondingly, how area should be partitioned between devices that should be matched. As a result, most texts and papers that discuss matching comment on the ratio-matching accuracy of two matched devices and readers generally are led to the conclusion that similar ratio-matching accuracy is achievable when ratios greater than one are required. As a result, the issue of how area should be partitioned between the matching-critical components does not arise and an integer ratio of $\theta$ is generally achieved by starting with a unit cell and then placing $\theta$ cells in series or in parallel to achieve the desired ratio. As a result, the area allocated to the two matching-critical components will often also be either 1: $\theta$ or $\theta$: 1. Smaller unit cells are often used to accommodate common-centroiding but the 1:$\theta$ or the $\theta$:1 ratios are generally still maintained.

In what follows, we will limit our discussion of ratio-matching accuracy to resistors. A simple example will show that that area partitioning does play an important role in yield. Consider the case of a standard feedback amplifier of Fig. 1 designed for a gain of –16 where a unit rectangular resistor of active area $A_R$ is used to realize $R_A$ and where $R_B$ is the series connection of 16 of the unit resistors. As will be formalized later, it can be shown that the effect of local random variations in the sheet resistance on the gain $\theta = -R_B/R_A$ results in a standard deviation of the gain given by $\sigma_\theta = \frac{4\sqrt{17}K_\rho}{\sqrt{A_R}} \approx \frac{16.5K_\rho}{\sqrt{A_R}}$ where $K_\rho$ is a constant characteristic of the process. Correspondingly, if $R_B$ is realized as the series connection of four of the same unit resistors and if $R_A$ is realized as the parallel connection of the unit resistors, it can be shown that

$\sigma_\theta = \frac{8\sqrt{2}K_\rho}{\sqrt{A_R}} \approx \frac{11.3K_\rho}{\sqrt{A_R}}$ and the total area will be reduced from $17A_R$ to $8A_R$. Thus the second layout approach will not only reduce the standard deviation but it will also reduce the area by over a factor of 2 as well. An equal area comparison of the two layout techniques in this example may be more useful. This can be achieved if the area of the unit resistor in the second layout technique is increased by a factor of 17/8 resulting in a standard deviation in the gain of $\sigma_\theta = \frac{32K_\rho}{\sqrt{17}\sqrt{A_R}} \approx \frac{7.76K_\rho}{\sqrt{A_R}}$. Thus, with equal active area, there is a factor of over 2 reduction in the standard deviation of the gain with the second technique or, equivalently, for a given standard deviation requirement, the total active area can be reduced by over a factor of 4 with the second layout technique. The implications of this change in standard deviation on yield are significant. If the equal area partitioning is used in this example with a Gaussian resistor distribution and the area is determined for a yield of 99%, then if the same total resistor area were used but the standard layout were adopted instead of the equal area partitioning layout, the yield would be reduced to 76%. In what follows, the optimal area partitioning for minimizing the standard deviation of the ratio of two resistors will be developed and practical layout strategies that are at or near this optimum will be presented.

## Optimal Area Partitioning

Following an approach similar to that used in [4], [6], and [7], it can be shown that the standard deviation of the normalized resistance of any rectangular film resistor due to local random variations in the sheet resistance is given by the expression

$$\sigma_{\frac{R_{ran}}{R_N}} = \frac{A_\rho}{\rho_N\sqrt{WL}} = \frac{A_\rho}{\rho_N\sqrt{A_R}} = \frac{K_\rho}{\sqrt{A_R}} \quad (1)$$

where $A_\rho$ is a process parameter characterizing the local random variation in the sheet resistance, $\rho_N$ is the nominal value of the sheet resistance, W and L are the width and length of the resistor and $A_R$ is the resistor area. The parameter $K_\rho$ is the ratio $A_\rho/\rho_N$. In this derivation, the contact resistances and the edge roughness of the resistor have been neglected.

The statistics, specifically the standard deviation of the gain $\theta = -R_B/R_A$ is of interest in characterizing the yield performance of the amplifier. It can be shown that the standard deviation of the gain $\theta$ can be expressed in terms of the normalized standard deviations of the resistors $R_A$ and $R_B$ by the expression

$$\sigma_\theta = \theta_N\sqrt{\sigma^2_{\frac{R_{Aran}}{R_{AN}}} + \sigma^2_{\frac{R_{Bran}}{R_{BN}}}} \quad (2)$$

where $\theta_N$ is the nominal gain. Trivially, the total resistor area $A_T$ can be expressed in terms of the areas of the resistors $R_A$ and $R_B$ by the expression

$$A_T = A_{RA} + A_{RB} \quad (3)$$

It now follows from (1), (2) and (3) that the standard deviation of $\sigma_\theta$ can be expressed as

$$\sigma_\theta = K_\rho\theta_N\sqrt{\frac{1}{A_{RA}} + \frac{1}{A_{RB}}} = K_\rho\theta_N\sqrt{\frac{1}{A_{RA}} + \frac{1}{A_T - A_{RA}}} \quad (4)$$

By taking the derivative of $\sigma_\theta$ with respect to $A_{RA}$ and setting to zero, it follows that the standard deviation of the gain is minimized when $A_{RA} = A_{RB}$ and the minimum standard deviation is given as

$$\sigma_{\theta\,min} = \frac{2K_\rho\theta_N}{\sqrt{A_T}} \quad (5)$$

Although the standard deviation of the gain will be minimized when the resistor areas are equal, the reference unit resistor should still be used to implement $R_A$ and $R_B$. This will introduce a quantization effect that may preclude maintaining equal areas for $R_A$ and $R_B$. Since there may be several or even many ways to use a reference unit resistor to realize $R_A$ and $R_B$, the area penalty for having a non-optimal area partitioning is of interest for determining how effective a particular layout will be. If the split factor $\gamma$ is defined by the expression $\gamma = A_{RB}/A_T$, it follows from (4) and (5) that the standard deviation of the gain can be expressed in terms of the parameter $\gamma$ as

$$\sigma_\theta = \sigma_{\theta min}\frac{1}{2\sqrt{\gamma(1-\gamma)}} \quad (6)$$

A plot of the normalized standard deviation of the gain versus $\gamma$ is shown in Fig. 2. From this plot it is apparent that it maintains a very shallow minimum but that the penalty goes to infinity if the area differences are large. If we want the standard deviation to be within 0.5% off the optimal value, then $0.4502 \le \gamma \le 0.5498$. If a 1% deviation is required, then $0.4298 \le \gamma \le 0.5702$.

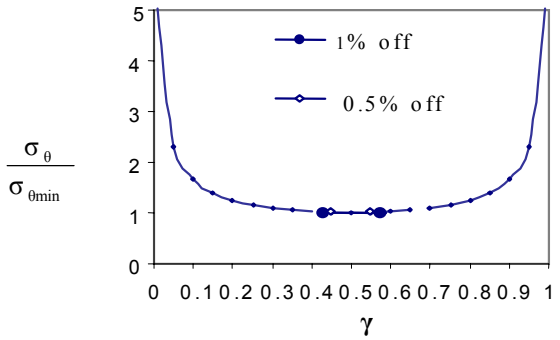

Fig. 2 Effects of Area Partitioning on Normalized Standard Deviation

Three basic resistor structures will now be considered for use in the layout of the resistors $R_A$ and $R_B$ in the

amplifier. The resistor $R_1$ will be considered to be the unit reference resistor, $R_2$ will be a parallel connection of the unit cells and $R_3$ will be a series connection of the unit cells. If the normalized variance of the resistors $R_A$ and $R_B$ are known, then the standard deviation of the gain can be obtained from (2). Now if a standard layout strategy is used, that is, $R_A$=$R_1$ and $R_B$=$R_2$ or $R_A$=$R_3$ and $R_B$=$R_1$ to get a gain of - $\theta_N$, then the total resistor area is $A_T = (1+ \theta_N) A_1$. It follows from (2) that in either case,

$$\sigma_\theta = \frac{K_\rho \sqrt{\theta_N}(1+\theta_N)}{\sqrt{A_T}} \qquad (7)$$

And for either of these layout schemes, the standard deviation of the gain is equivalent to that for a parameter $\gamma$ of

$$\gamma = \frac{1}{1+\theta_N} \qquad (8)$$

It thus follows form (8) and (6) that if $\theta_N = 1$, the standard layout is optimal but if the amplifier gain is large, the standard layouts will be far from optimal.

An appreciation of the magnitude of the yield loss associated with a non-optimal area partitioning associated with the standard layout scheme may be useful. To make this comparison, it will be assumed that the gain has a Gaussian distribution and the area is determined so that a yield of Y is achievable with an optimal area partitioning for a given gain $\theta_N$ and that the actual yield is $Y_{ACTUAL}$. It follows from (5) and (7) that

$$\sigma_\theta = \sigma_{\theta min}\left[\frac{1+\theta_N}{2\sqrt{\theta_N}}\right] \qquad (9)$$

It can now be shown that the actual yield related to the optimal yield Y by the relationship

$$Y_{ACTUAL} = \mathrm{erf}\left(\frac{\sqrt{2}\sqrt{\theta_N}}{1+\theta_N}\,\mathrm{erf}^{-1}\left(Y\sqrt{2}\right)\right) \qquad (10)$$

where erf is the standard mathematical "error function" or, equivalently, in terms of the CDF of the standard N(0,1) random variable, F, as

$$Y_{ACTUAL} = 2F\left(\frac{2\sqrt{\theta_N}}{1+\theta_N}F^{-1}\left(\frac{1+Y}{2}\right)\right) - 1 \qquad (11)$$

As an example, if an amplifier is sized for an optimal yield of 99% and if a standard layout for a gain of 5 is used, the yield is reduced to approximately 95%, if the gain is 10,25,100, then the yield is reduced to 86%, 68% and 39%, respectively.

## Comparison of performance of different layouts

In the following, amplifiers with gains from 1 to 4 with different layouts will be discussed along with a comparison of the $\gamma$ factors for these layouts.

As observed previously, for a gain of 1, if $R_A = R_B = R_1$, then the structure is optimal and has a value of $\gamma = 0.5$.

The amplifier with a gain of 2 can be implemented with $R_A = R_1$, $R_B = R_2 = 2R_1$ or $R_A = R_2 = ½R_1$, $R_B = R_1$. Obviously, the area ratio $\gamma$ is 2/3 and 1/3, respectively. They are symmetric to the point of 0.5. The gain error deviations correspondingly are denoted as 1 and 2 in Fig 3. It follows from (6) that the standard deviation is about 6% above the minimum. This yield loss is small suggesting either layout is practical. If the sizes of the resistors are large (so spacing and edge effects don't cause problems), a modest reduction of the standard deviation is possible by a more complicated layout. One way to achieve this is to use a much smaller reference resistor and use a parallel combination of two series strings of 4 of these reference resistors to realize $R_B$ and 3 parallel strings of 3 of these resistors to realize $R_A$. This would require 17 reference resistors but with this approach the $\gamma$ factor would become 0.4706, which would result in a deviation of the standard deviation of less than 0.2% from the optimal. The

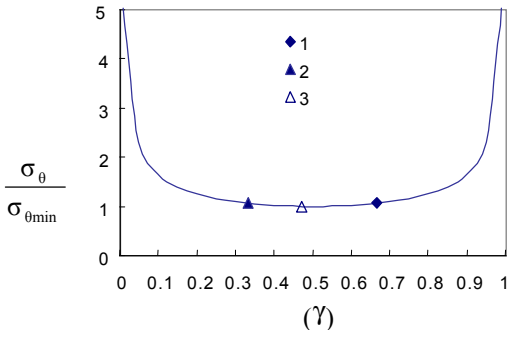


Fig. 3 Gain of 2 Amplifier 1) Series Feedback, 2) Parallel Input, 3) variance

standard deviations of the gain for the 3 layouts are depicted in Fig 3.

Similarly, there are also several methods for the layout of an amplifier with a gain of 3. For example, it can be realized with $R_B = R_3 = 3R_1$, $R_A = R_1$ with $\gamma = 3/7$ or $R_B = 3R_1$, $R_A = R_1$, with $\gamma = 48/97$.

For realizing a gain of 4, it is very easy to split the area equally. One method is to implement $R_A = ½R_1$, $R_B = 2R_1$with 4 unit resistor cells, which achieves a minimum standard deviation of the gain with $\gamma = 0.5$.

## Achieving Near-Minimum Gain Variance

It is apparent that for some gains, the minimum value of $\gamma = 0.5$ cannot be achieved but by appropriately segmenting the resistors, layouts with $\gamma$ very close to the optimum can be obtained as evidenced by the examples considered for the cases of gains of 2. Table 1 shows some near-optimal solutions for some other gains.

From the above results, a procedure for obtaining near-optimal standard deviation of the gain can be described. If the gain $\theta$ is a square of natural number, then

$R_B$ can be realized with $\sqrt{\theta}$ = n unit cells in series to get a nominal value of n $R_{1N}$ and $R_A$ can be realized with n cells in parallel to get a nominal value of $R_{1N}/n$. This will result in equal area partitioning and a minimum standard deviation of the gain. If the gain is not a square, then $R_B$ can be realized as a series connection of $\theta$ unit cells and $R_A$ will be a parallel connection of K strings of series-connected unit cells with each string containing K unit cells. There are many other ways to achieve a given gain with near-equal area partitioning. If the gain is a perfect square, the procedure described will provide a practical layout. If the gain is not a perfect square, the method described may not be the best way to do the area partitioning even though $\gamma$ will be very close to 0.5. The reason is the number of unit cells may be large and correspondingly the effects of edges and the area associated with cell spacing will limit performance.

**Table 1 some possible structures for some gains**

| Gain value | $R_{BN}$ (# of $R_{1N}$) * $R_{AN}$ (# of $R_{1N}$) in terms of $R_N$ | Area ratio $\gamma$ |
|---|---|---|
| 1 | 1(1)*1(1) | 0.5 |
| 2 | 2(8)*1(9), 2(2)*1(1) | 8/17,2/3 |
| 3 | 3(48)*1(49), 3(3)*1(4) | 48/97,3/7 |
| 4 | 4(4)*1(4) | 0.5 |
| 5 | 5(80)*1(81),5(5)*1(4) | 80/161,5/9 |
| 6 | 6(24)*1(25),6(6)*1(4) | 25/49,6/10 |
| 7 | 7(63)*1(64),7(7)*1(9) | 63/127,7/16 |
| 8 | 8(8)*1(9) | 8/17 |
| 9 | 9(9)*1(9) | 0.5 |
| 10 | 10(10)*1(9) | 10/19 |

Although increasing the number of unit cells may appear to be unattractive, it must be recognized that the basic unit cell is often segmented anyway to allow for the common-centroiding that is necessary to reduce the effects of gradients and this segmentation may provide a practical mechanism for better area partitioning.

## Extensions

Although the focus in this work was on the effects of the localized random variations in the sheet resistance and its effects on the ratio matching accuracy of resistors, the issue of random variations in contact resistances and in the statistical variation of the boundary are often major factors that affect ratio matching accuracy as well. Although beyond the scope of this work, reductions in the standard deviation of ratio-matching errors due to these nonidealities can also be achieved by appropriately partitioning the unit cells between the two elements that are to be matched. In the latter cases, both the partitioning of the unit cells between the two elements that are to be matched and the total number of unit cells and their aspect ratios play a role in determining an optimal layout.

The concepts introduced here extend to sizing of capacitors for optimal capacitor ratio matching as well as transistors for optimal current –ratio matching.

## Conclusion

It has been shown that the standard layout procedure for ratio-matched resistors often gives a large standard deviation of the gain due to local random variations in the sheet resistance of the film. The optimal partitioning of area between two ratio-matched resistors was shown to occur when the areas of the resistors were identical independent of the desired resistor ratio. Improved layout strategies were introduced that will provide yield enhancement in matching-critical applications. Although standard layout procedures will give good performance when the component ratios are small, substantial improvements in yield are possible when realizing circuits that require precise large component ratios if the new layout procedures are used.

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