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Simple CMOS transresistor

M.E. Schlarmann and R.L. Geiger

A simple highly-linear transresistor is reported. Simulation and experimental results are presented.

Introduction: Owing to the nonlinear I-V characteristics of the MOS transistor, distortion is a serious problem in MOS resistive circuits (MRCs). As a result, several linearisation techniques for MRCs have emerged. Most reported techniques have been derived by inspection of simple analytical device models to deduce the conditions under which full or partial suppression of nonlinear terms takes place (e.g. [1, 2]). In practice, these circuits do not perform as well as predicted since the simple analytical models used in their development do not accurately model the distortion characteristics of an MOS transistor [3–5]. With two notable exceptions [6, 7], neglecting mobility variation appears to be the dominant source of modelling error contributing to the residual nonlinearities [4, 5]. In this Letter we report a simple and compact transresistor with linearity characteristics that compares favourably with the most linear, higher-complexity transresistors previously reported.

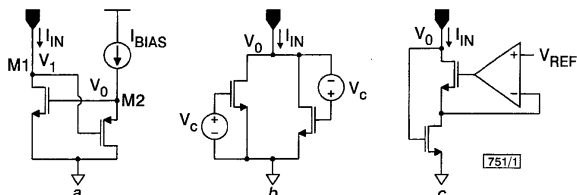


Fig. 1 Single-ended transresistors

- a Proposed
- b Banu [1]
- c Wyszynski [8]

Proposed circuit: The proposed transresistor is shown in Fig. 1a. I_{BIAS} is large enough to ensure that M2 is strongly inverted and saturated. M2 bootstraps the gate voltage of M1 to its drain. The offset provided by the bootstrap circuit is larger than the threshold voltage of M1 ensuring that for non-negative input currents M1 operates in the linear region. I_{IN} develops a voltage V_1 at the drain of M1. The relationship between I_{IN} and V_1 is highly linear. Bootstrapping V_0 to V_1 , in turn, establishes a linear relationship between I_{IN} and V_0 . The linearity is actually improved by the imperfect level-shift circuit. The channel conductance of M2 causes a slight fluctuation in the gate-drain voltage of M1. This variation partially offsets the nonlinearities.

Assuming a high-impedance current source, the transresistance gain is approximately:

$$R_T = \left(\frac{1}{g_{m1} + g_{o1}} \right) \Big|_{Q-Pt.} = \frac{L_1}{\mu_n C_{ox} W_1 (V_{1Q} - V_{T1Q})}$$

where g_{m1} and g_{o1} are the small-signal model parameters of M1,

V_{1Q} is the quiescent value of V_1 , and V_{T1Q} is the threshold voltage of M1 at the quiescent point.

Simulation results: Two of the most linear single-ended transresistors reported are included in Fig. 1. The structure of Fig. 1b from Banu [1] achieves partial cancellation of even-ordered nonlinearities in the absence of mobility degradation. The transconductor by Wyszynski [8] configured as a transresistor is shown in Fig. 1c. The latter circuit requires an amplifier but if the often used symmetric models are used for the MOSFETs, a linear transresistance is obtained.

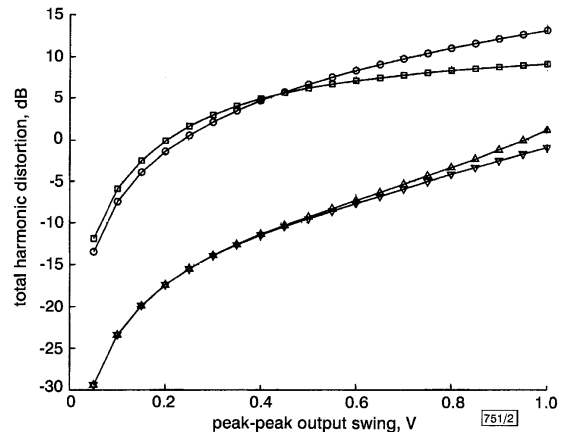


Fig. 2 Total harmonic distortion for single-ended structures

- Banu
- Pennock/Wyszynski
- ▽ proposed V_0
- △ proposed V_1

The transresistors of Fig. 1 were each designed to achieve a nominal transresistance of 10 k Ω in a 0.25 μ m 2.5 V CMOS process. Simulations were performed with HSPICE using a BSIM3 (Level 49) model. A single p -channel transistor was used to provide I_{BIAS} for the proposed circuit and a linear single-pole macro-model was used for the amplifier of Fig. 1c. A sinusoidal input current superimposed on a quiescent current of 25 μ A was applied at the inputs. Fig. 2 shows a comparison of the total harmonic distortion (THD) as a function of the output swing. From these results, it is apparent that the proposed transresistor is substantially more linear than the existing structures for signal swings up to 1 Vp-p.

Balanced versions of the transresistors of Fig. 1 were simulated by exciting two single-ended transresistors differentially. The quiescent operating points and the nominal transresistances were the same as used for the single-ended simulations. The simulations show that the THD is reduced by more than 40 dB via the use of balanced structures for differential swings up to 2 V. The linearity characteristics of the proposed circuit and the Wyszynski circuit are nearly identical. Their THDs differ by less than 0.7 dB over the specified signal range. These two circuits exhibit at least a 6 dB reduction in THD over the output signal swing range when compared with the Banu structure.

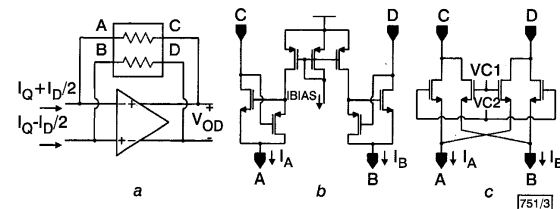


Fig. 3 Application as transresistance gain stage

- a Gain stage using transconductance feedback network
- b Balanced version of proposed circuit
- c Czarnul/Song circuit

Application in transresistance gain stage: The transresistors of Fig. 1 are not suitable for driving resistive loads because they do not have low output impedances. A low output impedance transresistor can be realised by putting a transconductor in the feedback path of an op-amp as shown in differential form in Fig. 3a.

This circuit was simulated using the subcircuits of Figs. 3b and c to realise the resistive feedback network. Fig. 3b shows a balanced version of the proposed transresistor configured as a differential-in/differential-out transconductor. Fig. 3c shows the popular Czarnul/Song [2] transconductor. Using simple analytical models for the MOS transistors, both even- and odd-ordered nonlinearities are cancelled. Practically, mobility degradation limits the performance of the circuit.

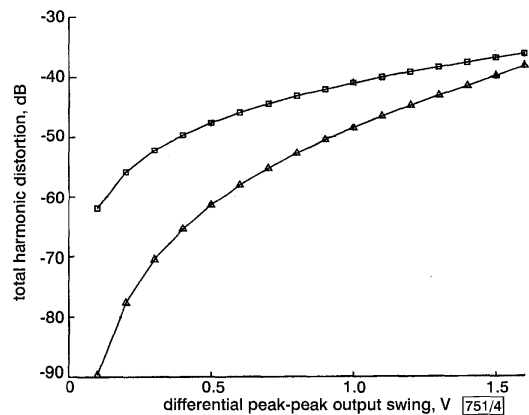


Fig. 4 Total harmonic distortion of transresistance gain stage for two different feedback networks

—△— proposed
—□— Czarnul/Song

Fig. 4 shows the simulated THD as a function of the output swing for low-frequency sinusoidal differential input currents ranging from 5 to 80 μ A. These simulations suggest the new circuit offers a significant improvement in linearity compared to the Czarnul/Song circuit.

Experimental results: The proposed circuit was constructed using a transistor array fabricated in a 5 μ m CMOS process. Since the devices were prefabricated, no attempt was made to optimise the individual or relative device sizes. Device dimensions were $W1/L1 = 42/5$ and $W2/L2 = 42/7$ in μ m. The circuit was tested at supply voltages of 5 and 10 V. For the 5 V case, the transresistance gain was 2.5 k Ω . The maximum deviation from linear relative to the full-scale deflection was $\pm 0.35\%$ for an output swing of 1.5 V. For the 10 V case, the transresistance gain was 1.6 k Ω . The maximum deviation from linear was $\pm 0.4\%$ for an output swing of 5 V. Even better performance could be achieved by optimising the device sizes and/or by implementing balanced versions of the circuit.

Conclusions: A simple, compact transresistor is introduced. Simulations show its linearity properties are attractive when compared to some of the best transistors reported in the literature. Experimental results from a single-ended structure indicate a linearity deviation bound by $\pm 0.35\%$ over a voltage swing of 1.5 Vp-p. Balanced versions of the circuit are even more linear.

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Polarisation insensitive deep-ridge vertical-groove DFB waveguide for all-optical switching

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A deep-ridge vertical-groove distributed feedback (DFB) waveguide has been fabricated. Structural birefringence of the fabricated device was completely eliminated by controlling waveguide width. Additionally, polarisation independence of the grating coupling coefficient was accomplished by adjusting grating depth.

Introduction: All-optical switches, which are not restricted by the speed of electronic devices, will be inevitable components for the implementation of ultrafast optical signal processing. We have demonstrated all-optical bistable switching [1] and thresholding operation [2] in strip distributed feedback (DFB) waveguides containing optical Kerr media. However, the state of polarisation of input light in all of those results has to be adjusted precisely, since those devices intrinsically have strong structural birefringence. Polarisation-insensitive switching operation is strongly required for the practical application of an optical communication system. For a waveguide optical switch, a most promising way to demonstrate polarisation-insensitive characteristics is to eliminate the structural birefringence of the waveguide. It has been already applied in many semiconductor-based photonic devices, such as a PHASAR demultiplexer [3], an optical ADM [4] and an optical switch [5]. In this Letter, we present elimination of structural birefringence in the GaInAsP/InP deep-ridge vertical-groove (VG) DFB waveguide for polarisation-insensitive all-optical switching. We also discuss the polarisation independence of the grating coupling coefficient (κ_c).

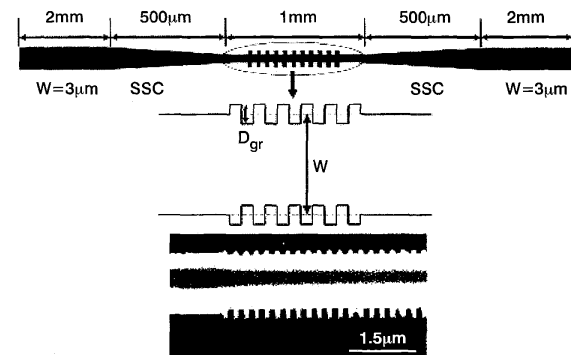


Fig. 1 Schematic diagram of deep-ridge vertical-groove DFB waveguide and SEM picture of fabricated device