A High Gain CMOS Operational Amplifier With Negative Conductance Gain Enhancement

Jie Yan and Randall L. Geiger

Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011, USA

Abstract

A fully differential CMOS operational amplifier using a negative conductance gain enhancement technique is presented. The amplifier was fabricated in an AMI 0.5 um CMOS process with an active area of 0.17 mm^2. With a 3 Volts supply, a DC gain of more than 80dB was measured. The gain exceeded 60 dB for a 240mV output swing.

1. Introduction

The realization of high-gain amplifiers with large Gain-Bandwidth-Products (GB) in processes with decreasing supply voltages is becoming a challenging task. For two decades, researchers have been enhancing amplifier gain by increasing the output impedance of a basic gain stage. This approach has proven effective for realizing high gain and high GB with favorable power dissipation. Two approaches for output impedance enhancement are widely used. One uses cascoding and the second uses a regulated cascode approach [1]. For low supply processes, these cascoded approaches are becoming unviable. A third approach, based upon negative transconductance compensation, has been discussed in the literature. Although this latter approach offers potential for the most gain enhancement, low power dissipation, low voltage operation, and excellent high frequency performance, the technique is seldom used commercially because of the high sensitivity of the gain to the negative transconductance element inherent in existing negative transconductance schemes. In this paper, we exploit a negative impedance gain enhancement technique with an approach that significantly reduces the gain variability to the compensating impedance.

2. Negative Impedance Gain Enhancement

The basic concept of gain enhancement by negative impedance compensation is shown in Fig.1 (a). Negative resistor R_n is placed in parallel with the output impedance of the basic amplifier. It follows from the small signal equivalent circuit of Fig.1 (b) that the small signal gain of the amplifier when driving a capacitive load C_L is

$$A_V(s) = \frac{v_o}{v_i} = \frac{-g_m}{sC_L + g_{ds} + 1/R_n} \qquad (1)$$

If $R_n = \frac{-1}{g_{ds}}$, the DC gain becomes infinite. Since this gain enhancement approach does not introduce additional internal nodes, it does not adversely reduce the high-frequency response of the basic amplifier so wide bandwidth can be realized.

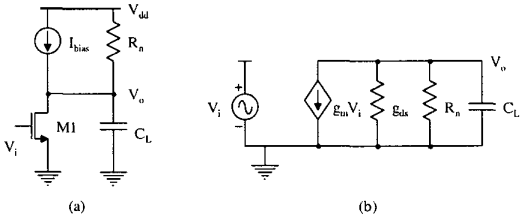

Fig. 1 Basic concept of negative conductance gain enhancement technique

Several researchers have proposed negative impedance gain enhancement circuits. Allstot [2] used a cross-drain-coupled differential pair to generate the negative impedance. Gregorian suggests this approach can practically increase the gain by only a factor of 4 [3]. Nauta applied negative resistance to a simple inverting transconductor in order to increase the DC gain of the transconductor [4], [5]. Nauta reported a DC gain of 46dB with a 10V power supply. In [6], positive feedback was applied to generate an effective negative load conductance. Although a gain of 80dB was reported with a 10V supply voltage, the gain-bandwidth-product was only 12MHz for a 5pF capacitor load. The structure in [6] requires a high frequency differential gain stage to achieve conductance cancellation. This gain stage introduces internal nodes and thus limits the high-frequency response.

These structures all share a common characteristic; a negative transconductance is used to compensate for positive output conductances. To achieve adequate gain enhancement, the negative transconductance must precisely compensate the positive output conductance. The major drawback of using negative transconductance to compensate for the output conductance is the difficulty in accurately matching these unlike terms over process and temperature. This drawback has limited the practical utilization of this approach.

A new negative impedance gain enhancement circuit was proposed that generates a negative conductance rather than a negative transconductance [7]. The negative conductance circuit is added at the output of a simple one-stage amplifier to practically achieve substantial gain enhancement. Fig. 2 shows the concept of the proposed negative conductance gain enhancement technique. A PMOS transistor M_n is placed at the output of the basic amplifier. A low gain stage A is connected between the gate and the source of M_n. Transistor M_n is biased in the saturation region and its gate-source voltage is AC shorted. Body effects are eliminated if an n-well CMOS process is used. If the gain of the low gain stage, A, is larger than 1, then a negative conductance of $(1\text{-}A).g_{dsn}$ parallels the output conductance of

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the basic amplifier. The small signal gain of this circuit is given by the expression

$$A_v(s) \approx \frac{-g_{m1}}{sC_L + g_{ds1} + g_{ds2} + g_{dsn}(1-A)} \qquad (2)$$

From this expression it is apparent that the dc gain goes to infinity as $(A\text{-}1)g_{dsn}$ approaches $g_{ds1}+g_{ds2}$ and that as $(A\text{-}1)g_{dsn}$ is increased, the open-loop pole crosses into the right half-plane when $g_{ds1}+g_{ds2} = (A\text{-}1)g_{dsn}$.

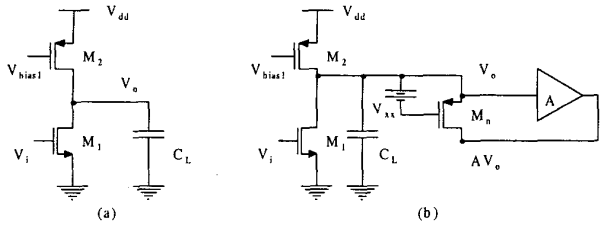

Fig. 2 A new negative impedance gain enhancement technique a) Basic amplifier, b) Basic amplifier with negative conductance gain enhancement.

The proposed gain enhancement technique generates a negative conductance that is only a function of g_{ds} and is not related to g_m. Therefore, negative g_{ds} can realistically match positive g_{ds} terms and the matching requirements for achieving very high DC gain are less stringent than for the existing –gm gain enhancement schemes. Further, this circuit has the potential for precise digital control of a large dc gain by exploiting the property that there is a phase reversal as the pole crosses the origin in the open-loop transfer function that can be detected. Since $g_{ds} \approx \lambda I_{DQ}$, the negative conductance can be easily adjustable through the adjustment of the biasing current of transistor M_n.

3. Implementation of Fully Differential CMOS Op Amp

A prototype two-stage fully differential high gain amplifier was designed based on the proposed negative conductance gain enhancement technique to validate the fundamental performance characteristics of the negative conductance gain enhancement technique. The block diagram of the amplifier is shown in Fig. 3.

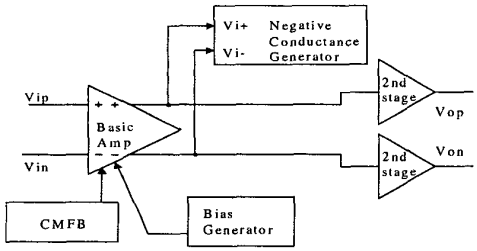

Fig. 3 Block diagram of the fully differential amplifier

The amplifier consists of five elements, a basic amplifier (the first stage), a negative conductance generator (NG), a common-mode feedback circuit (CMFB), a bias generator, and the second stage. The amplifier was designed to have most of the DC gain contributed by the first stage while the second stage only provides a gain of 2 to 3. For a given gain, the output signal swing requirements of the first stage is reduced by a factor of 2 to 3 by adding the second stage. The overall amplifier thus can maintain a large overall voltage gain over a wider output range [8].

Fig. 4 shows the transistor-level schematic of the basic amplifier and the second stage. Fig. 5 shows the transistor-level schematic of the negative conductance generator. The low gain stage A is shown in Fig. 6. The Bias generator provides biasing voltages V_{BP} and V_{BN}. The CMFB circuit provides V_{CM} for transistor M6 to control the common-mode voltage at the output of the basic amplifier. Their schematics are not shown in this paper.

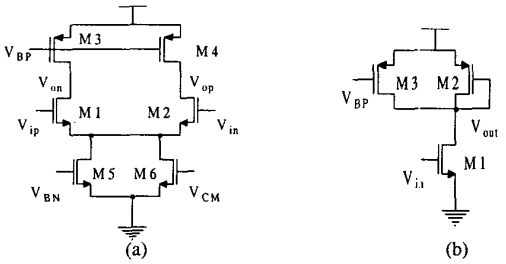

Fig. 4 Schematic of a) Basic amplifier, b) the second stage

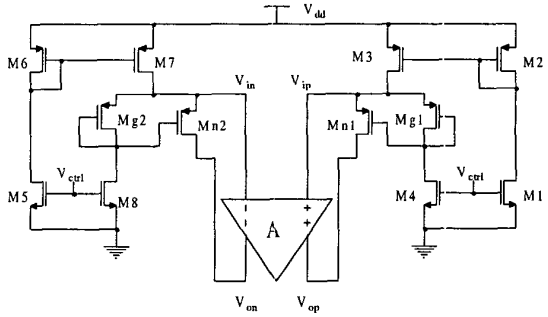

Fig. 5 Schematic of negative conductance generator

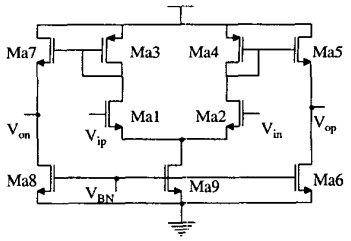

Fig. 6 Schematic of low gain stage A

The negative conductance generator generates a negative conductance which is proportional to the conductance of transistors Mn1 and Mn2. The negative conductance is

adjustable by changing the control voltage Vctl thus change the bias current of transistors Mn1 and Mn2.

A half circuit of the basic amplifier useful for determining the DC gain is shown in Fig.7. The DC gain is

$$A_{vd}=\frac{V_{out}}{V_{in}}=\frac{-g_{m1}}{(g_{ds1}+g_{ds2}+g_{ds3})+g_{dsb}+kg_{mn}+(1-A)g_{dsn}} \quad (3)$$

where $k=\frac{g_{dsb}}{g_{dsb}+g_{mg}}$ (4)

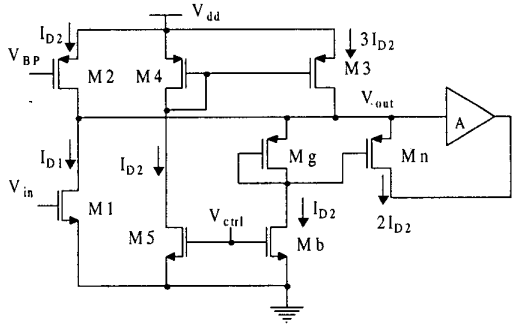

Fig. 7 The half circuit of the basic amplifier

From equation (4), if $g_{dsb} << g_{mg}$, k will be a small number and the g_{mn} term in the denominator of equation (3) can be ignored so the DC gain becomes

$$A_{vd}=\frac{V_{out}}{V_{in}}=\frac{-g_{m1}}{(g_{ds1}+g_{ds2}+g_{ds3})+g_{dsb}+(1-A)g_{dsn}} \quad (5)$$

The relationship between I_{D2} and the control voltage V_{ctrl} is given by

$$I_{D2}\approx\frac{\mu_n C_{ox}W_5}{2L_5}(V_{ctrl}-V_{tn})^2 \quad (6)$$

Since

$$g_{ds}\approx\lambda I_D \quad (7)$$

only one value of V_{ctrl} will make the denominator of the gain expression (5) zero and A_{vd} infinite.

If g_{dsb} is comparable to g_{mg} , the g_{mn} term in the denominator of the gain expression (3) should be taken into account. Since

$$g_m=\sqrt{2\mu C_{ox}(W/L)I_D} \quad (8)$$

there are multiple values of V_{ctrl} that will make the denominator of the gain of (3) zero and correspondingly A_{vd} infinite.

4. Experimental results

The amplifier was fabricated using the AMI Semiconductor (AMIS) 0.5um AMI_C5N process through MOSIS. For this process the maximum rated voltage supply is 5 Volts, however, the amplifier was designed for reliable operation at 3 Volts.

The open-loop DC gain was measured with the feedback circuit of Fig. 8 by applying a low frequency differential square wave signal at the input. The amplifier was implemented to have a closed-loop gain of one with on-chip feedback resistors. The differential error signals V_{i+} and V_{i-} at the op amp input were amplified by an off-chip amplifier with gain of 185. The output signals V_{op} and V_{on} were also measured. The open-loop differential DC gain is given by the expression

$$A_0=\frac{V_{op}-V_{on}}{V_{i+}-V_{i-}} \quad (9)$$

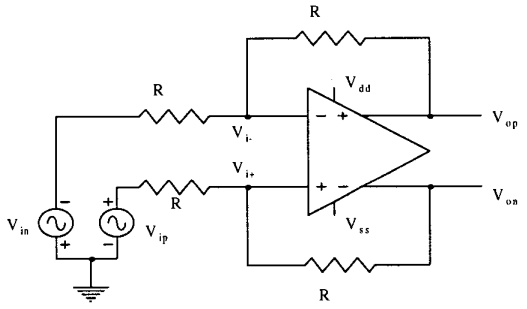

Fig. 8 Scheme for measuring open-loop DC gain

The die photo of the amplifier is shown in Fig. 9. The active area is 0.17 mm^2.

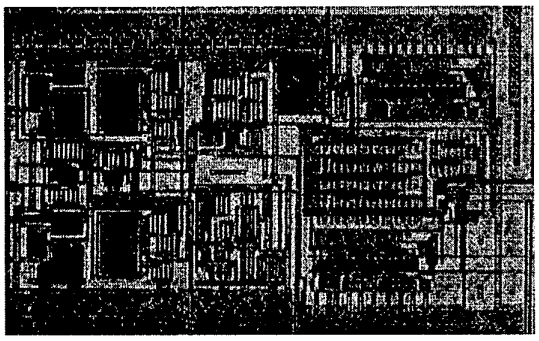

Fig. 9 Die photo of the amplifier

The amplifier was tested with ±1.5 V supply voltages. Fig. 10 shows the differential output signal (Math) and the amplified differential error signal (Ch3) for a control voltage Vctrl of –0.75871 Volt. The differential error signal is in phase with the differential output signal. The open-loop DC gain is 80.24dB. Fig. 11 shows differential output signal (Math) and amplified differential error signal (Ch3) for a control voltage Vctrl of –0.74507 Volt. The differential error signal is out of phase with the differential output signal and the open-loop DC gain is 83.76dB.

Fig. 12 shows the measured differential open-loop DC gain versus the control voltage Vctrl. The DC gain is adjustable with the control voltage. By keeping the control voltage fixed, the relationship between the DC gain and the output differential voltage Vod was measured. Results are shown in Fig. 13. Although the GB and the settling time of the amplifier were not measured because of a low bandwidth on-chip buffer, simulation results predict a GB of

153MHzwhen driving a 10 pf capacitive load with a phase margin of 52 degree for a feedback factor beta = 0.5 in excess of 60dB and settling time for a 1.2 Volts step to 0.1% in 47n sec.

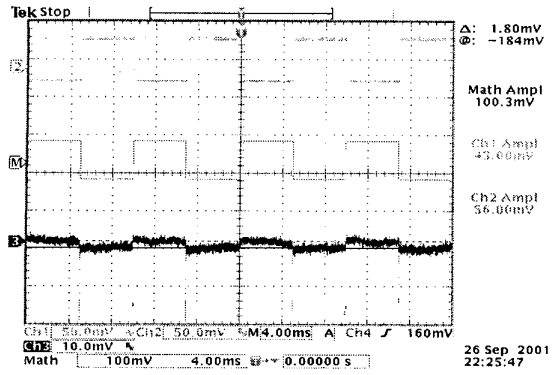

Fig. 10 Open-loop DC gain measurement results. The differential output signal (math) and the amplified differential error signal (ch3) with Vctrl = -0.75871 V.

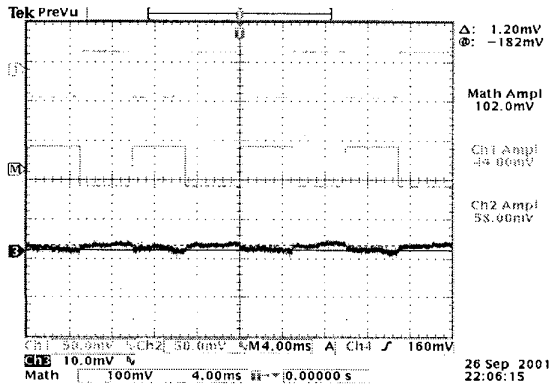

Fig. 11 Open-loop DC gain measurement results. The differential output signal (math) and the amplified differential error signal (ch3) with Vctrl = -0.74507 V.

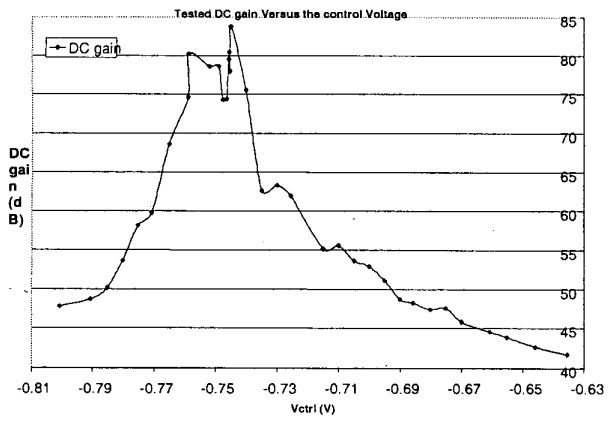

Fig. 12 DC gain versus the control voltage Vctrl

5. Conclusion

A fully differential CMOS operational amplifier using a new negative conductance gain enhancement technique was presented. The amplifier was realized in an AMI 0.5 um CMOS process and had a measured DC gain of 83dB. With a 3 Volts supply, power consumption is 45mW. The gain is over 60 dB for a 240mV output range.

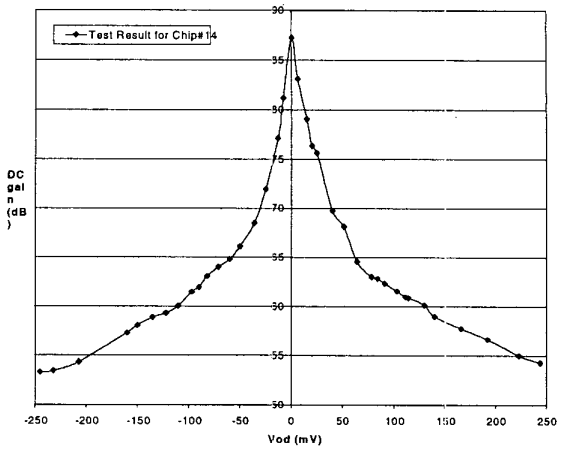

Fig. 13 DC gain versus the differential output voltage Vod

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