FORMULATION OF INL AND DNL YIELD ESTIMATION IN CURRENT-STEERING D/A CONVERTERS

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ABSTRACT

Current source mismatch is a major source of nonlinearity in current-steering Digital-to-Analog Converters (DAC). In order to achieve a given linearity specification at a given yield level, it is essential that the designer determine the minimum required matching accuracy of the unit current sources. Monte-Carlo simulations are very time-consuming and provide the designer with little insight to choose proper DAC architectures and make tradeoff between design specifications. The limited mathematical formulations that have appeared in the literature are based on nonstandard linearity definitions or oversimplifying statistical assumptions. In this paper, simple formulas are obtained that accurately describe the relationship between nonlinearity, bits of resolution, minimum required matching accuracy, and yield, which make it possible to optimize the DAC structure and achieve high performance with less cost and power consumption.

1. INTRODUCTION

Current steering DAC's are increasingly used in high-resolution and high-speed signal processing and telecommunication applications. Linearity, typically characterized by INL and DNL, is one of the most important concerns for DAC design. A major error source of DAC nonlinearity is the current source mismatch due to process and environmental variations, which includes both random and gradient errors. The gradient errors can be effectively compensated by optimizing switching schemes [1] or using local biasing techniques [2]. The random variation of current sources are determined by the inherent properties of the technology used and can be assumed to be independent from each other and follow normal distribution. If the designed value of a unit current source is I, the actual current provided by the jth unit current source can be expressed as

$$I_j = I \cdot (1 + \varepsilon_j) \qquad (1)$$

where $\varepsilon_j \sim N(0, \sigma^2)$ is the relative deviation of I_j from I. Based on Pelgrom model, for a given technology, the relative standard deviation (σ)of a current source is determined by its overdrive voltage V_{GS}-Vt and its gate area $W \cdot L$ [3]. It is essential, when designing a current steering DAC, to find the minimum required matching accuracy (or σ) of the unit current sources so that the specified INL and DNL can be achieved with an acceptable yield. With this σ, the size of the current source transistors can be decided [4][5].

In the literature, the estimation of σ is generally made through thousands of Monte-Carlo simulations[4]. These simulations are very time-consuming for high-resolution DAC's and the results are only useful for the given bits of resolution, the given DAC architecture and the given specifications. This brute-force method may be tolerable compared to the whole design procedure when the DAC architecture is simple. However, it provides designers with little insights into how the matching accuracy affects the linearity and yield when the bits of resolution and/or the segmentation change. These issues are very important for making tradeoff between different specifications, especially when calibration is used. To gain more insight, simple parametric expressions are often preferred, which make it possible to optimize the DAC structure and achieve high performance with less cost and power consumption.

In order to investigate this problem, a statistical analysis of INL and DNL in thermometer-decoded and binary-weighted current-steering DAC's is presented. Following that, simple formulas are obtained that accurately describe the relationship between nonlinearity, bits of resolution, matching accuracy, and yield.

2. STATISTICAL CHARACTERISTICS

For matching purpose, an n-bit DAC array generally consists of $N=2^n-1$ identically designed unit current sources. When only random mismatches present, the current provided by unit current source I_j ($1 \le j \le N$) can be expressed by (1). After the offset and gain being corrected, the end-point INL at digital code k ($1 \le k \le N$), is defined as the deviation of the real analog output, $I(k)$ in the units of LSB (Least Significant Bit), from the ideal output, k. The DNL at k is the deviation of the step size between k-1 and k from 1 LSB. The INL and DNL of the overall DAC are defined as the worst case among them. In the n-bit DAC array described by (1), the offset is 0 and the gain is equal to

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I(N)/N which is also the average current (denoted as $\bar{I}$) of the N unit current sources, hence

$$\bar{I} = \frac{\sum_{i=1}^{N} I_j}{N} = I \cdot (1 + \frac{\sum_{i=1}^{N} \varepsilon_j}{N}) \quad (2)$$

After offset and gain correction, the INL and DNL at digital code k are given by

$$INL(k) = \frac{I(k)}{\bar{I}} - k \quad (3a)$$

$$DNL(k) = \frac{I(k) - I(k-1)}{\bar{I}} - 1 \quad (3b)$$

If the DAC is thermometer decoded, then $I(k)$ in (3) is equal to $I\left(k + \sum_{j=1}^{k} \varepsilon_j\right)$. Through first-order approximation, (3a) and (3b) can be rewritten as

$$INL(k) \approx \frac{N-k}{N} \sum_{j=1}^{k} \varepsilon_j - \frac{k}{N} \sum_{j=k+1}^{N} \varepsilon_j \quad (4a)$$

$$DNL(k) \approx \frac{N-1}{N} \varepsilon_k - \frac{1}{N} \sum_{j=1, j\neq k}^{N} \varepsilon_j \quad (4b)$$

Since $INL(k)$ and $DNL(k)$ are both linear combinations of N independent normal random variables ε_1, ε_2, ..., ε_N, they also follow normal distributions, and

$$INL(k) \sim N(0, \frac{(N-k)\cdot k}{N}\sigma^2) \quad (5a)$$

$$DNL(k) \sim N(0, \frac{N-1}{N}\sigma^2) \quad (5b)$$

It can be seen from (5a)&(5b) that the maximum standard deviation of INL, which is equal to $\frac{\sigma}{2}\sqrt{N - \frac{1}{N}}$, occurs at the mid-code transition when k=(N-1)/2 or (N+1)/2. The standard deviation of DNL is rather small and approximately equal to σ, the standard deviation of a single unit current source. In real designs where segmented architectures are exclusively used, the DNL of a DAC is determined by the binary-weighted DAC array, while its INL are mainly dependent on the thermometer-decoded array driven by the MSB's. Being lack of significance in practice, the DNL of thermometer-decoded DAC will not be further discussed in this paper.

The INL at digital code 1,2,...,N form a N-dimensional normal distributions and can be expressed in a vector

$$\boldsymbol{INL} = [INL(1), INL(2), \cdots, INL(N)] \approx \boldsymbol{\varepsilon} \cdot \boldsymbol{B} \quad (6)$$

where , $\boldsymbol{\varepsilon} = [\varepsilon_1, \varepsilon_2, \cdots, \varepsilon_N]$ and according to (4a)

$$\boldsymbol{B} = \frac{1}{N}\begin{bmatrix} N-1 & N-2 & \cdots & 2 & 1 & 0 \\ -1 & N-2 & \cdots & 2 & 1 & 0 \\ \vdots & -2 & & \vdots & \vdots & \vdots \\ \vdots & \vdots & \ddots & 2 & \vdots & \vdots \\ -1 & -2 & \cdots & -(N-2) & 1 & 0 \\ -1 & -2 & \cdots & -(N-2) & -(N-1) & 0 \end{bmatrix}_{N\times N}$$

A simple normalization, scaling down the vector in (6) by a factor of σ, allows the analysis to be independent of σ. That is,

$$\boldsymbol{U} = \boldsymbol{\varepsilon}/\sigma = [u_1, u_2, \cdots, u_N] \sim N(\boldsymbol{0}_{1\times N}, \boldsymbol{I}_{N\times N})$$

$$\boldsymbol{INLnor} = \boldsymbol{U}\cdot\boldsymbol{B} \sim N(\boldsymbol{0}_{1\times N}, \boldsymbol{B}^T\cdot\boldsymbol{B}) \quad (7)$$

where $\boldsymbol{0}$ and $\boldsymbol{I}$ represent zeros and identity matrix respectively, and $\boldsymbol{B}^T$ is the transposition of $\boldsymbol{B}$.

With the mean and covariance matrices given above, it is easy to obtain the joint density function of ***INLnor***,

$$f_{INL}(x_1, x_2, \cdots, x_N) = \frac{1}{(2\pi)^{N/2}|\boldsymbol{C}|^{1/2}} \cdot exp(-\frac{1}{2}\boldsymbol{X}\boldsymbol{C}^{-1}\boldsymbol{X}^T) \quad (8)$$

where $\boldsymbol{C} = \boldsymbol{B}^T\cdot\boldsymbol{B}$, $\boldsymbol{X} = [x_1, x_2, \cdots, x_N]$.

It can be shown that the INL and DNL of a binary-weighted DAC follow the similar normal distributions except that the covariance matrices are different. In this case, the INL at each digital code has the same variance as that shown in (5a), while the DNL have large variance at the major carries and the worst case occurs at the mid-code transition with standard deviation around $\sigma\sqrt{N - \frac{1}{N}}$, doubling that of the INL.

3. YIELD ESTIMATION

For a given INL specification, for example INL within ±A LSB, the INL yield of a normalized DAC (σ=1) can be expressed as

$$\Phi(n, A) = P(|INL(k)| \le A, k = 1,2,\cdots,N) = \int_{-A}^{A}\cdots\int_{-A}^{A} f_{INL}(x_1, x_2, \cdots, x_N)dx_1dx_2\cdots dx_N \quad (9)$$

where $N=2^n-1$. If the relative standard deviation of each unit current source is σ, the yield of the DAC is equal to $Y = \Phi\left(n, \frac{A}{\sigma}\right)$. Alternately, to guarantee a certain yield Y, the minimum required current matching accuracy is equal to

$$\sigma = \frac{A}{\Psi(n, Y)} \quad (10)$$

where Ψ is the inverse function of Φ.

No one has reported a method of accurately calculating the integral shown in (9) without resorting to numerical methods. It appears that approximations must be made to derive a simple expression. Lakshimikumar has presented two rough bounds for INL yield estimation in binary-weighted DAC's [6][7]. One is overly pessimistic ignoring the strong correlation between different analog outputs and the other is rather optimistic only considering the contribution of the two mid-scale codes. The limitations of the two bounds were clearly shown in [8][9]. Another formula proposed by Bosch for INL yield estimation is based on a nonstandard INL definition where each current output is compared to the ideal value without correcting the gain error [9]. It is well known that gain error does not impact linearity. The same problem has been found in the Monte-Carlo simulation results of some recently reported current-steering DAC designs, e.g. [4],[5] and [10]. As a

result, the matching accuracy chosen in these DACs are significantly overestimated so that the area cost are much more than necessary and some segmentations made in the DACs are not as good as they are supposed to be. In this paper, a simple but accurate approximation of (10) is given for both INL and DNL yield in thermometer-decoded and binary-weighted DAC's through the following observations:

In thermometer-decoded DACs, the covariance matrix of the **INL** given in (6) shows that substantial correlation exists between the INL's at different digital codes. The closer the two codes are, the stronger the correlation is. As we mentioned before, the difference between the INL of two adjacent codes, *k-1* and *k*, or DNL(*k*), is approximately equal to ε_k (the relative deviation of the unit current source I_k), which is negligibly small. Therefore, picking the even samples in the INL sequence results in another INL sequence with almost the same profile as the original sequence, meaning that the two INL sequence must have very similar probability falling in [-A, A] range. Here, the unit of A (LSB) is referring to n-bit resolution. It is equivalent to A/2 LSB for n-1 bit resolution. Therefore, the n-bit DAC associated with the original INL sequence and the n-1 bit DAC associated with the new INL sequence have nearly the same probability or yield to achieve INL≤A and INL≤A/2 respectively. Of course, as part of the original INL sequence, the new sequence will have less chance to go beyond the range and hence a little higher yield than its n-bit counterpart. However, these minor differences can be neglected and will diminish with the decreasing of σ. The n-1-bit DAC (obtained from the original DAC by setting the LSB to 0) is actually formed by combining each adjacent unit current sources in the original n-bit DAC. Thus the jth unit current source in the new DAC, denoted as I_j' ($1 \le j \le 2^{n-1}-1$), is equal to $I_{2j-1}+I_{2j}=2\left(1+\frac{\varepsilon_{2j-1}+\varepsilon_{2j}}{2}\right)$ and its relative standard deviation is $\sigma'=\sigma/\sqrt{2}$. In summary, in the n-1 bit DAC, $\sigma'=\sigma/\sqrt{2}$, $A'=A/2$, $Y'\approx Y$. Putting these values into (7), we can conclude that

$$\Psi(n,Y)\approx\sqrt{2}\Psi(n-1,Y)\approx\left(\sqrt{2}\right)^n/\mathrm{Z}(Y) \qquad (11)$$

hence,

$$\sigma\approx\frac{A}{\left(\sqrt{2}\right)^n}Z(Y) \qquad (12)$$

where $Z(Y)$ only depends on the yield requirement and can be well tabulated. Fig.1 shows the plot of $Z(Y)$, which are obtained through Monte Carlo simulations assuming A=0.5LSB and n= 8,10 and 12 bit respectively. The similarity of the three curves proves that Z(Y) has little dependence on the bits of resolution, hence the validity of (12). This figure works for DACs with any bits of resolution, and with it we can predict the required current source matching accuracy for any given INL specification and achieve a certain yield. For example, for a 14-bit DAC, to achieve INL≤0.5LSB and 99% guaranteed yield, the relative standard deviation of unit current source has to be less than $\frac{0.5}{\left(\sqrt{2}\right)^{14}Z_{INL}(99\%)}\approx 0.22\%$. As we mentioned before, this formula is more accurate for high-accuracy DAC's since their unit current sources have smaller variations.

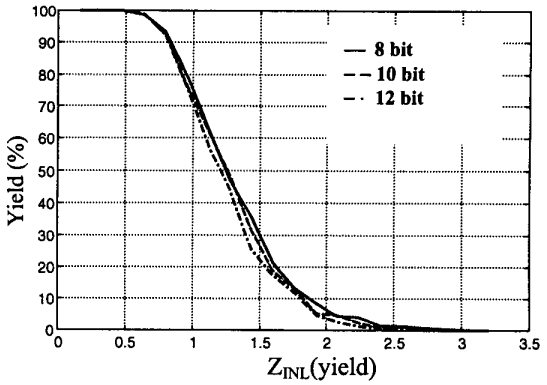

Fig.1 Z(yield) for INL yield of Thermometer-decoded DAC

Fig.1 also shows that in the region close to 100% yield level, the yield is not very sensitive to *Z(yield)* and hence the matching accuracy σ. Followed is a steep region where the yield degrades significantly when σ only increases by a small amount. This is more serious for high-resolution DAC's since $Z(Y)=\frac{\sigma}{A}\left(\sqrt{2}\right)^n$. Therefore, in real design some margin should be given to σ in order to avoid large degradation of yield due to run-to-run variations. However, being too conservative is also not preferred because small σ means large area. Besides, when σ is smaller than a certain value, the improvement of the yield becomes insignificant.

Similar results can be obtained for binary–weighted DAC's. It is well known that the nonlinearities of binary-weighted DAC are all associated with the major carries. The severity of the problem is proportional to the weight of the bit [2][10]. Therefore, the linearity of the DAC won't change much when getting rid of bit0.). In another words, the resulting n-1 bit DAC has similar INL and DNL profiles as the original DAC. The partition of the N unit current sources in the resulting n-1bit DAC is as follows:

bit0→ $I_1'=(I_2+I_3)$
bit1→ $I_2'+I_3'=(I_4+I_5)+(I_6+I_7)$
…

It is shown that the *j*th unit current source in the new DAC denoted as $I_j'(1\le j\le 2^{n-1}-1)$ is the sum of I_{2j} and I_{2j+1}, and its relative standard deviation $\sigma'=\sigma/\sqrt{2}$. Therefore, formula (12) is also valid for the INL and DNL yield of binary-weighted DAC except that $Z(Y)$ are different. Fig.2 (a) & (b) show the plots of $Z(Y)$ for INL yield and DNL yield respectively. It is observed that with the same

matching accuracy and the same yield, the DNL of a binary-weighted DAC is worse than its INL. This observation disagrees with the conclusions drawn in [10] that "if the matching of the D/A chip has been designed to achieve the INL yield specification, the DNL specification will automatically be achieved within the same yield requirement even in the extreme case of a full binary topology". We have proved that this statement is not true. Binary structure does suffer more DNL than INL. Also notice that the plots in Fig2 (a) are very similar to those shown in Fig.1. It implies that segmentation helps little for reducing INL, but may significantly reduce DNL and relax the matching requirements.

With these plots (Fig.1 and Fig.2) and formula (12), the minimum required matching accuracy and a proper segmentation can be easily determined. For a 14-bit segmented DAC, as we calculated before, to achieve INL≤0.5LSB and 99% guaranteed yield, the relative standard deviation of the unit current sources has to be less than 0.22%. If the n1-bit MSB's are thermometer decoded and the remaining 2-bit LSB's are binary weighted, based on (12) where Z_{DNL} (99%)≈0.3, n=n2+1, σ≈0.22%, to achieve DNL≤0.5LSB, n2 must be less than 11 bits. Otherwise smaller σ or larger current sources have to be used. These results (σ≈0.22% and n2<11) can be verified through Monte-Carlo simulations, which show that when n2=10, the yield for both INL and DNL less than 0.5LSB is 99.8%.

4. CONCLUSIONS

Assuming the random variations of the unit current sources in a current-steering DAC are independent and normal distributed, the INL and DNL at each digital code of the DAC also follow normal distributions. However, the strong correlation between different outputs results in a very complex expression for yield calculation. Neither this expression nor the widely used Monte-Carlo simulations can clearly reveal the relations between the nonliearity (INL and DNL), the yield and the current matching accuracy for a given resolution. To gain more insight for design optimization, simple but accurate formulas were given in this paper for both thermometer-decoded and binary-weighted DAC's. It is shown that the INL and DNL of current-steering DAC's are proportional to the relative standard deviation of the unit current sources (σ). To achieve the same linearity and yield, σ must be reduced by $\sqrt{2}$ for each extra bit of resolution. It is also shown that thermometer-decoded DAC's has similar INL yield as their binary-weighted counterpart, but much less DNL. Binary–weighted topology suffers more severe DNL than INL. It was shown that segmented architecture provides a compromise between the performance requirement and the cost of area and power. Optimal segmentation can be easily achieved using the formulas given in this paper.

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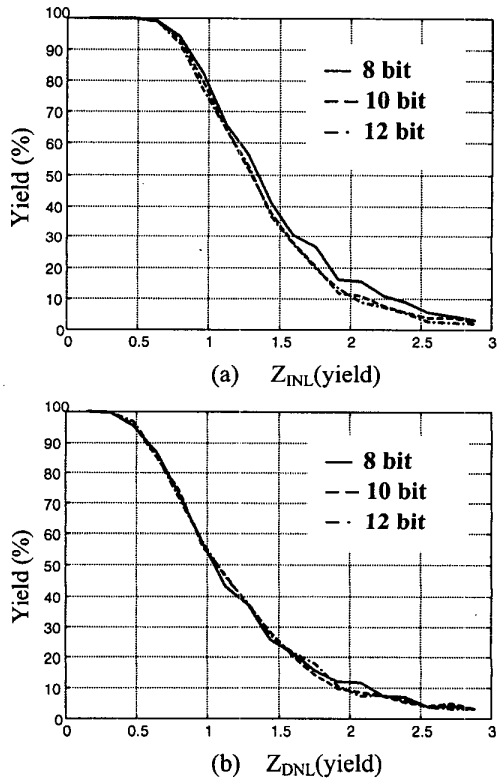

Fig.2 Z(yield) for (a) INL and (b) DNL yield of binary-weighted DAC