AMPLIFIER STRUCTURE FOR HIGH GAIN AND FAST SETTLING APPLICATIONS

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ABSTRACT

High gain amplifiers with fast settling times are needed for high-speed data converter applications. A cascaded amplifier architecture is discussed that can make use of several architecturally identical amplifies to achieve the desired gain. Only one of the amplifiers has a gain-bandwidth product requirement that is modestly higher than the rest to keep the overall structure stable in the presence of negative feedback. The performance of a three-amplifier cascade is compared with that of single amplifier performance for applications at the 10 – 22 bit level range when used as an inverting amplifier with a gain of –1.

1. INTRODUCTION

Data converter circuits require fast settling and high gain amplifiers. The high gain is needed for the output of the amplifier to settle accurately to the desired final value. Cascode amplifiers are widely used because they satisfy both requirements. The problem with using the cascode amplifiers is the limitation that occurs due to the need of a high supply voltage to provide an acceptable output signal swing. This becomes a problem especially with the technology pushing towards smaller device sizes and lower supply voltages. An alternative that does not require large supplies is to cascade amplifiers to achieve the desired gain. Various cascade feed forward schemes already exist [1][3][4][5]. However, they introduce pole-zero pairs that exhibit imperfect cancellation. This causes the appearance of slow settling components in the transient response. Unless the magnitude of the effects are sufficiently small, long settling time constants can not be tolerated in many applications.

This paper discusses a method for cascading amplifier stages to achieve the desired gain and at the same time maintain comparable settling time to that of a basic amplifier. The structure examined in this paper has different pole-zero characteristics than previously examined structures that make it possible for the output to settle quickly. In what follows, the architecture is discussed then a three stage cascaded amplifier is analyzed in some detail.

2. PROPOSED ARCHITECTURE

The amplifier architecture is based upon the cascade of a number of amplifiers (n) to achieve the desired overall gain for the amplifier. Figure 1 shows the block diagram of the cascaded amplifier structure. One amplifier (the n^{th} in Figure 1) will have to be dominant to maintain stability, while the remaining (n-1) amplifiers can be identical. The dominance factor, that is the ratio between the pole locations of the identical amplifiers and the dominant one, will be determined based on the number of stages using Routh's stability criterion. In this context, the use of the term dominance does not imply that the pole of this amplifier is at a much lower frequency than the remaining poles.

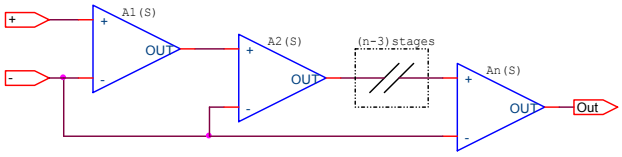

Figure 1, Cascaded amplifier architecture

The amplifier architecture of Figure 1 is similar to that discussed over two decades ago in the context of building discrete analog filters in which the sensitivity of the filter parameters to the gain-bandwidth product of the operational amplifier was reduced with this type of cascading [2]. Emphasis in the earlier work was restricted to the sinusoidal steady-state response of the filters in which the amplifiers were used with no consideration of either the settling performance or of the potential impact of long settling time constants that are of major concern in amplifiers with open-loop zeros.

The rest of this paper will focus on an example of a three-stage cascade implementation of the structure of Figure 1.

3. THREE STAGE CASCADED AMPLIFIER

Figure 2 shows a feedback configuration based upon the three stage cascaded amplifier in the inverting configuration with a gain of -1. It will be assumed that each amplifier behaves as a single-pole amplifier with transfer function A(s) that is given by

$$A_i(s) = \frac{A_o}{1 + \frac{s}{p_i}} \tag{1}$$

For all except the lowest frequencies, this can be simplified to

$$A_i(s) = \frac{1}{\tau_i s} \tag{2a}$$

where

$$\tau_i = \frac{1}{GB_i} \tag{2b}$$

and GB is the gain bandwidth product of the individual amplifier.

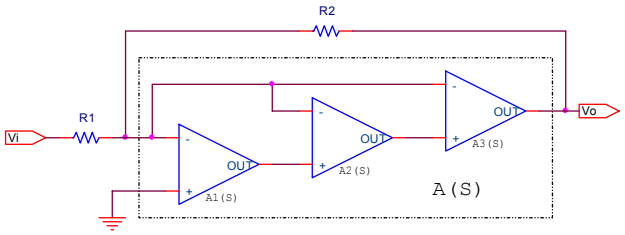

Figure 2, Three stage cascaded amplifier in inverting configuration

It follows from the model of (2a) that the open loop amplifier gain is given by

$$\frac{V_o}{V_-} = \frac{-\left(1 + \tau_1 s + \tau_1 \tau_2 s^2\right)}{\tau_1 \tau_2 \tau_3 s^3} \tag{3a}$$

and the closed loop gain is given by

$$\frac{V_o}{V_{in}} = \frac{-\left(R_2/R_1\right)\left(1 + \tau_1 s + \tau_1 \tau_2 s^2\right)}{1 + \tau_1 s + \tau_1 \tau_2 s^2 + \left(1 + \frac{R_2}{R_1}\right)\tau_1 \tau_2 \tau_3 s^3} \tag{3b}$$

If the first two amplifiers are identical and the third is dominant, then we can let

$$\tau_1 = \tau_2 = \tau \tag{4}$$

With this assumption, applying Routh's stability criterion to (3b) we get the condition for stability is

$$\tau_3 < \frac{\tau}{1 + \frac{R_2}{R_1}} \tag{5}$$

But since $R_2 = R_1$ for the unity gain feedback amplifier, we can reduce the condition of stability to

$$\tau_3 < \frac{\tau}{2} \tag{6}$$

For this design we will choose τ_3 to be somewhat less than τ so that the system is not just marginally stable. Now looking at the denominator of (3b) we can approximate the real-axis closed-loop pole approximately by

$$s = -\frac{1}{\tau} \tag{7}$$

This approximation is not real accurate but sufficient to provide insight into the operation of the amplifier.

Since the open-loop and closed-loop zeros are the same, it follows from (3a) or (3b,) that the zeros are located at

$$s = -\frac{1}{2\tau} \pm j\frac{\sqrt{3}}{2\tau} \tag{8}$$

This analysis shows that we have a real-axis pole shown in (7) and two other poles that will be approximately canceled by the zeros in (8). The question now is: will imperfect pole-zero cancellation create slow settling components in the step response? Imperfect pole-zero cancellation will cause the presence of additional settling components but since the zeros are high in frequency and since any uncancelled poles will be close to the zeros, the resultant time constants will not be particularly long.

Figure 3 below shows a pole-zero plot of the approximated closed-loop poles and zeros for (3b) with $R_2 = R_1$ and $\tau_3 = \tau/10$.

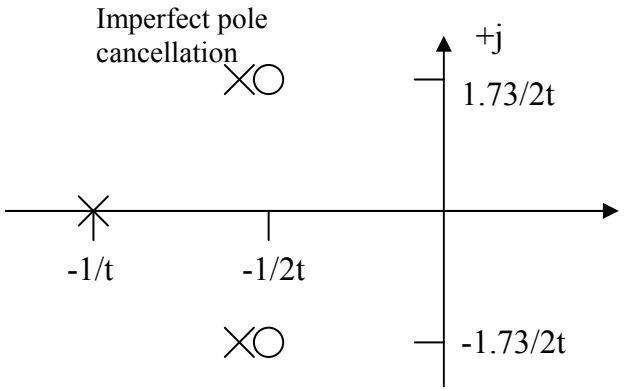

Figure 3, Closed loop pole-zero plot

4. CONCEPT SIMULATION

In order to verify the concept, simulations were run using PSpice to compare the performance of the proposed structure to that of the basic amplifier. The basic amplifier used was the same as one of the identical amplifiers in the first two stages of the structure.. It is important to note that since the single amplifier will have a low gain, the settling accuracy will be poor compared to that of the cascaded amplifier structure.

The amplifiers were simulated with an ideal gain of -1 and an input step. Each individual amplifier was modeled as a first-order block that has a transfer function given in (1.) The individual amplifiers were set to have a DC gain of 1000 and a dominant pole at 10 Hz. The dominant amplifier in the cascaded structure was set to have a DC gain of 1000 and a single pole at 100 Hz.

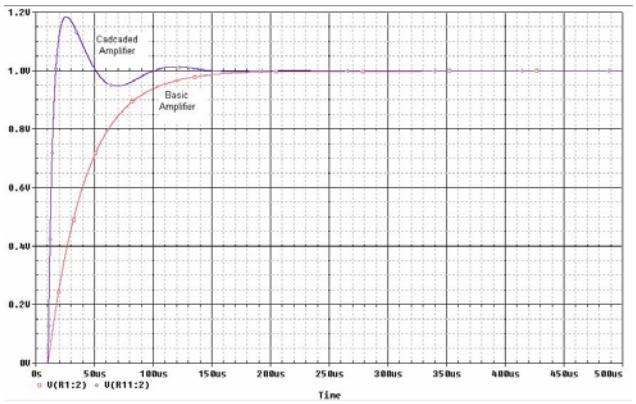

Figure 4a, Amplifiers outputs

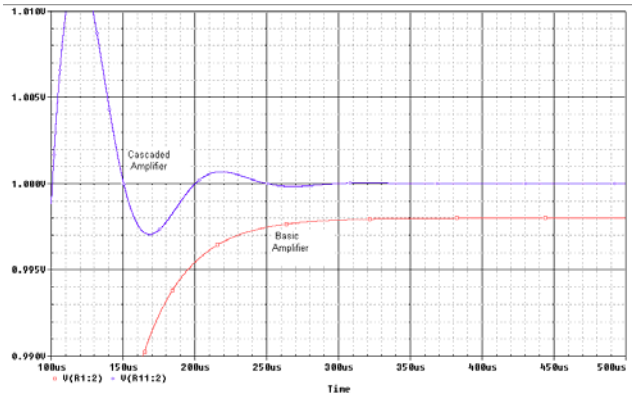

Figure 4b, Amplifiers outputs (Zoomed)

Figure 4 shows the outputs of both the basic and the cascaded structures (the outputs are inverted.) The cascade structure exhibits an under-damped response but it settles to the final value with greater than 22-bit accuracy and it exhibits a comparable settling time to that of the basic amplifier. It is important to note that the single amplifier output does not settle to the desired final value even at the 10-bit level due to inadequate dc gain. From Figure 4b we can clearly see the advantage we gain with the proposed cascaded structure.

The over shoot of the cascade can be reduced by making a more dominant n^{th} amplifier in the cascade.

The settling time was measured to be the final time in which the output enters the +/- 1 LSB accuracy window as shown in Figure 5 where, β is the feedback factor, t_s is the settling time and

$$\varepsilon = \frac{1}{2^m} \qquad (9a)$$

where

m = number of bits of accuracy (9b)

Table 1 shows the results obtained from the simulations and also does a comparison between the single amplifier and the cascaded amplifier results.

Figure 6 shows the settling time as a function of the desired bit accuracy level for the cascaded amplifier. As expected, the settling time has a linear relationship with the bit level. This is due to the fact that the slow settling components of the output have a time constant that is comparable to that associated with the real-axis feedback pole of the amplifier.

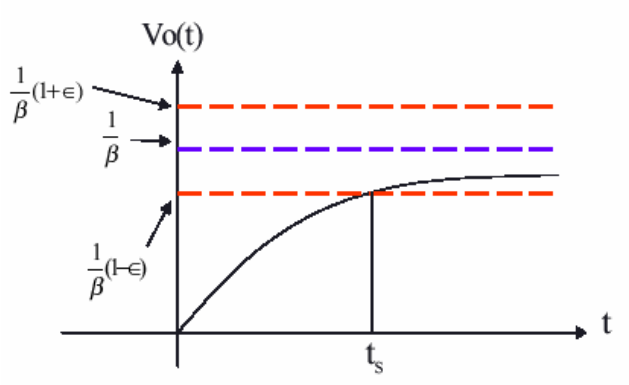

Figure 5, Settling Measurement

Table 1, Transient response data

Parameter	Basic Amplifier	Cascaded Amplifier
Final Value (V)	0.998	1.00
0.99 final value (us)	158	126
Rise Time (10%-90%) (us)	70	5
10-bit Settling (us)	Inf.	190
15-bit Settling (us)	Inf.	387
20-bit Settling (us)	Inf.	486

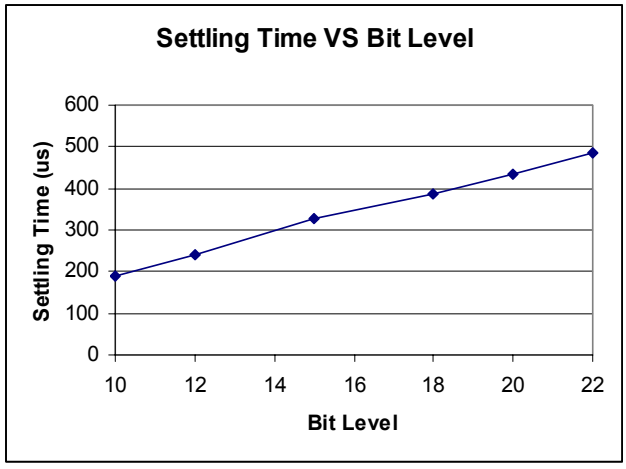

Figure 6, Settling time VS bit level

The cascaded amplifier structure achieve both high gain and fast settling, and has the advantage of not requiring the large supply voltages inherent in using cascode topologies. In particular, the level of gain boosting attainable with this technique is much larger than what can be practically achieved with either a cascode or a regulated cascode architecture even if signal swing was not of major concern in the latter structures. Although the example presented in this section focused specifically on a three-stage cascaded structure, the theory is applicable to two or four or any number of stages that may be needed to get the desired dc gain.

6. CONCLUSIONS

In this paper a method of cascading amplifiers for achieving settling times comparable to those of single-stage amplifiers while realizing very high gains with low supply level requirements was discussed.. These structures did not exhibit the long settling time constant problems inherent in most alternative structures that depend upon precise pole-zero cancellation for fast precision applications.

7. REFERENCES

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