A MODIFIED HISTOGRAM APPROACH FOR ACCURATE SELF-CHARACTERIZATION OF ANALOG-TO-DIGITAL CONVERTERS

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ABSTRACT

A new approach for measuring the INL and DNL of an A/D Converter that uses histogram information is introduced. Unlike most existing algorithms, this method does not require the generation of accurate input signals so offers potential for use in a Built-in Self-Test (BIST) environment. Multiple inputs are presented to the device under test and the histograms obtained at the output are analyzed to characterize both the device and the nonlinear input. Preliminary simulation results for a 10-bit flash ADC suggest this approach can measure INL to the 0.5LSB level with a low spectral purity input signal that is linear to less than the 4-bit level.

1. INTRODUCTION

Testing is an integral part of the IC design cycle. Every circuit that is designed and fabricated needs to be tested before it is shipped to the customer. The emergence of high-performance, high-density devices has increased the demand on the number of testing steps and the required testing accuracy. This has resulted in testing costs becoming the fastest growing portion of the manufacturing cost [1] for some classes of circuits thus causing testing to emerge as the main bottleneck limiting the reduction of IC production costs. With the rapid improvement in process technology driving the minimum feature size down, the potential now exists for practically including additional circuitry to implement BIST functions on silicon.

Built-In-Self-Test (BIST) structures offer potential not only for reducing the direct cost associated with testing but also the indirect cost associated with overall production time. Although BIST for digital circuits has reached a modest level of maturity, BIST solutions for Analog and Mixed-signal products are still in an early phase of development.

High precision data converters are one class of products that are used in a multitude of applications whose testing and characterization has been and continues to be an area of active research. Various parameters are used to characterize data converters and in this paper, two of the most important static parameters, namely INL and DNL, are considered. A strategy for measuring these parameters that offers potential for use in BIST architecture is described.

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2. EXISTING METHODOLOGY

Code density tests are traditionally used for extracting the low frequency spectral characteristics of a data converter [2][3][4]. With this approach, either a deterministic signal of known spectral characteristics or a periodic stochastic signal of known pdf is converted by the device-under-test (DUT) and the output obtained is compared to the ideal output to characterize the device. Even though sine waves are widely used as input signals in commercial testers due to the ease with which they can be generated with high spectral purity, the most common reported stimulus for BIST applications has been a linear ramp. Ideally, an equal number of occurrences should be obtained in each bin at the output of the converter when a linear ramp is used as the input and any deviation from ideal can be attributed to device non-linearity. The histogram obtained is used to generate the tally and weight arrays as explained in [5].

The reliability of this testing method that has been derived under the assumption that the input is a perfect ramp depends on how accurately the input stimulus is generated. Even though considerable research has been made towards on-chip ramp generation, unlike commercial testers, generation of a high linearity ramp on chip is still a challenge. Any substantial non-linearity or distortion in the generated ramp will result in a deviation of counts expected in each bin. These issues along with several others regarding approaches to replicate the entire commercial production testing environment on silicon have limited industrial adoption of BIST into commercial products.

This work focus on overcoming the challenge of precise input test signal generation by using a low accuracy input signal ('ramp-like') that can be easily and repeatedly generated on-chip. A modified histogram scheme is introduced

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in which multiple ramp-like input signals are given to the DUT and the corresponding output histograms are obtained. These histograms are then analyzed to characterize both the device and the inconsequential input.

3. ALGORITHM

Although the proposed strategy can apply to different types of A/D converters, emphasis in this work is on one algorithm focused on the flash A/D converter. Details about a preliminary version of this algorithm are given in [6]. In this algorithm, a low accuracy low frequency (spatial) "ramp-like" input signal $(F1)$ is given to DUT and output histogram $H1$ is obtained. A related input signal $(F2)$ obtained by shifting $F1$ by a fixed amount is presented as a second input and histogram $H2$ is obtained at the output.

These two histograms are then used to predict the A/D converter non-linearity, specifically the DNL and the INL In the context of this work, the term "low accuracy" input means that we will assume we do not know precisely what the input waveform is. For example, if it is a "ramp-like" waveform, we may only know the value of the input waveform at any time to only within a few percent and, in particular, to a much lower accuracy than the ADC that will be tested. As such, the input waveform may have second or higher-order nonlinearities that deviate from an ideal ramp by many $LSBs$ relative to the resolution of the ADC under test. It is also assumed that the amount of shift of the input waveform is not precisely known and the shifted waveform may have modestly different nonlinearities than the original ramp-like waveform. What is implicit, however, in this work is the assumption that we can practically generate low accuracy "ramp-like" waveforms on silicon.

Figure 1 gives a plot of the transfer-characteristics of the input excitation signal. Overlaid on top are the ideal and non-ideal trip points of the A/D converter and the number of samples obtained in each bin at the output. It is assumed that $F2$ is shifted with respect to $F1$ by a fixed but unknown amount X_{LSB}. The various symbols that are used in the figure are:

- $I_i \rightarrow i^{th}$ transition level of the Ideal ADC
- $T_i \rightarrow i^{th}$ transition level of the actual (non-ideal) ADC
- $\Psi_i \rightarrow$ deviation of (T_i) from (I_i)
- $\Delta_i \rightarrow$ Number of samples in Ψ_i
- $F1 \rightarrow$ 'ramp-like' input signal
- $F2 \rightarrow F1$ shifted by a fixed amount
- $C_i \rightarrow$ Number of samples in the ith bin for ideal ADC with $F1$ as the input signal
- $C_i' \rightarrow$ Number of samples in i^{th} bin for actual ADC with $F1$ as input signal
- $C_i'' \rightarrow$ Number of samples in i^{th} bin for actual ADC with $F2$ as input signal

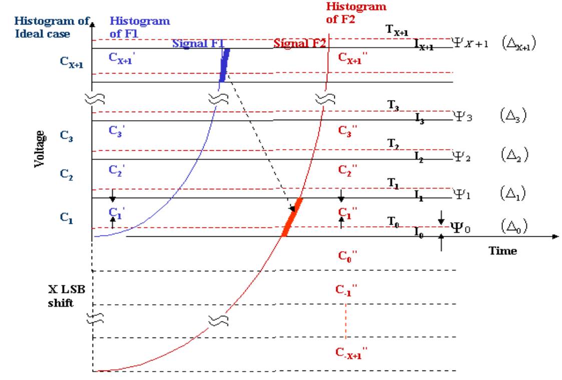

Fig. 1. Transfer Characteristics of the Input excitation signal

The counts C_i' and C_i'' represent the data used to obtain the histograms $H1$ and $H2$ respectively but the histograms are not directly depicted in the figure. We will refer to the sequences $< C_1' \ldots C_n' >$ and $< C_1'' \ldots C_n'' >$, where $n = 2^{Bits}$ as the histograms $H1$ and $H2$ and to the individual elements in these sequences as the elements of the histograms. Our goal in identifying the system is simply to determine the actual deviations of the ADC under test from that of an ideal ADC. In the context of the notation used in Figure 1, the goal is to determine the sequence $< \Delta_1 \ldots \Delta_i \ldots \Delta_n >$.

Since the input signal is assumed to have a low frequency non-linearity, for a small segment of input signal consisting of several adjacent bins, the input signal can be assumed to be locally linear. With this assumption, the elements of the histograms $H1$ can be related to the unknown Δs and Cs by the relationship:

$$C_i' = C_i + \Delta_i - \Delta_{i-1} \tag{1}$$

Since the second input is obtained by shifting $F1$ by X_{LSB}, the section of the second input that occurs in the ith bin corresponds to the section of the first signal that occurs at $(i+X)^{th}$ bin as shown by the dotted line in Figure 1. This relationship can be used to relate C_i" to the unknowns as follows:

$$C_i'' = C_{i+x} + \alpha_i \Delta_i - \alpha_{i-1} \Delta_{i-1} \tag{2}$$

where the $\alpha_i' s$ are scaling factors included to account for the slope change when $F2$ is obtained by shifting $F1$ by several LSBs. A good approximation of the difference in slope between $F1$ and $F2$ in each bin can be made as

$$\alpha_i = C_i'' / C_i' \tag{3}$$

Using (1),(2) & (3), we get

$$\begin{aligned} \Delta_{i+1} &= C_{i+1}' - C_{i+1-x}'' + \Delta_i + \alpha_{i+1-x} \Delta_{i+1-x} \\ &\quad - \alpha_{i-x} \Delta_{i-x} \quad \text{for} \quad i = 0 : 2^{Bits} - 1 \end{aligned} \tag{4}$$

where, $\Delta_0 = \Delta_{-1} = \ldots = \Delta_{-x} = 0$.

(4) requires the values of C_0", C_{-1}"...C_{1-X}", which are not available from $H2$. For small shifts an approximation can be made by assuming all of them to be equal and given by

$$C''_0 = C''_{-1} = \ldots = C''_{1-x} = \frac{Samples\,of\,F2 < 0}{Shift\,in\,LSBs} \quad (5)$$

Simulation results given in the next section confirm that this is a good approximation. Although it is assumed and justified in the algorithm explained in [6] that $\Delta_1 = 0$, a first order estimation of the actual Δ_1 can be made using C'_1 and C'_0. Once all the $\Delta's$ are obtained, the deviations of transitions in terms of LSB's are given by

$$\Psi_{LSB}(i) = \Psi(i)/LSB = \Delta(i)/C(i) \quad (6)$$

The DNL and INL for the converter are given by

$$DNL_i = \Psi_{LSB}(i) - \Psi_{LSB}(i-1); \;\; i\,\forall\,2\;to\;2^{Bits} \quad (7)$$

$$INL_i = \sum_{j=0}^{i} DNL_j \quad (8)$$

The INL obtained is then corrected for gain and offset error mathematically.

4. EXPERIMENTAL SETUP

To validate the algorithm, the entire system involving the input signal generation, A/D converter, and the histogram analysis was modeled in MATLAB. Simulations with different inputs were performed to confirm the robustness of the algorithm. Two key issues affecting the usefulness of the simulation results are the practicality of the model of the non-linear A/D and the ramp-like input signal. A 10-bit flash A/D converter based upon a resistor string with a unit resistance value of R was considered for all simulations. Random and uncorrelated errors based on a uniform distribution of $\pm 20\%R$ were added to all resistors to simulate a non-ideal ADC. Even though each resistor variation was restricted to $\pm 20\%R$, due to the nature of the flash architecture, a random walk pattern is observed in the sequential tap voltages. The errors in transition values for interior taps can vary by several LSBs, thereby requiring the algorithm to be sufficiently robust to evaluate them.

Non-ideal 'ramp-like' input signals were generated using the following equations:

$$V_{in1} = \delta_1 V_{ideal} + \delta_2 V_{ideal}^2 \quad (9)$$

$$V_{in2} = \delta_1 V_{ideal} + \delta_2 V_{ideal}^2 + \nabla S + \varepsilon \quad (10)$$

where δ_1, δ_2 are weighing constants and V_{ideal} refers to the ideal ramp signal. $\delta_1 = 1$ and $\delta_2 = 0$ corresponds to perfect ramp. ∇S refers to the amount in LSB by which the second input is shifted with respect to first signal, and ε refers to any error in shifting.

5. SIMULATION RESULTS

To identify the model errors in a conventional histogram method, an ideal 10-bit converter was initially considered. A ramp-like input signal with 4-bit linearity ($\delta_1 = 0.75$ & $\delta_2 = 0.25$) was used and the INL was evaluated using the conventional and the new algorithm. Results are given in Figure 2. Even though successful generation of ramps of $10-12$ bit linearity have been reported in literature, to reduce simulation time we have focused on a 10-bit converter with a $4-6$ bit linear ramp in this work. The concept can however be extended to higher bit converters where a $10-12$ bit linear excitation ramp will be a limiting factor. As seen in Figure 2, the new algorithm predicts the INL of the ideal converter to a small fraction of an LSB, as expected, while the conventional method predicts a maximum INL of 64LSBs due the non-linearities of the input signal. Of more interest is the ability of the algorithm to correctly predict non-linearities of a non-ideal ADC. A non-ideal ADC was modeled as explained in Section 4 by assuming that the resistors in the resistor string can be modeled as uncorrelated random variables. A second simulation that included the ADC nonlinearities was performed to see the effect of possible shifting errors. The second signal was shifted by 1LSB, but the shift was restricted to 6-bit accuracy. This can be achieved by selecting ε term appropriately. The INL predicted by proposed algorithm and the actual INL introduced is given in Figure 3. It can be seen that the algorithm still closely predicts the linearity values. However, as explained in Section (3), shifts of 1LSB may not be practical. A third simulation in which the ∇S value was set to 32LSB with a 0.5LSB error in shifting introduced to account for 6-bit shift accuracy was performed. A slightly modified algorithm was used. The converter was divided into multiple sections and the delta values were found for each section

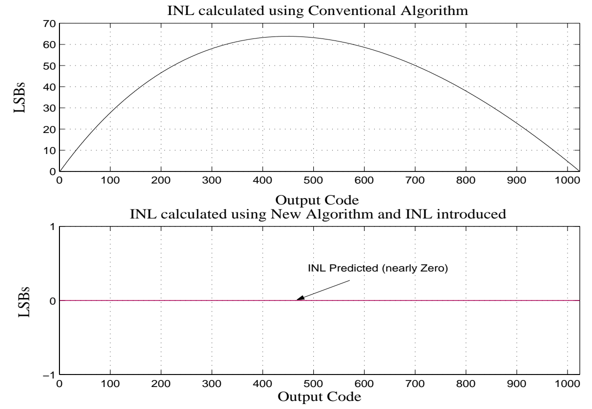

Fig. 2. INL plots for an 10-bit Ideal Converter with a Non-ideal ramp-like Input

independently before combining them. Figure 4 shows the difference between the DNL introduced and the DNL predicted using the new algorithm. A plot of the predicted

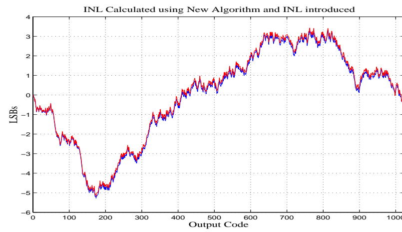

Fig. 3. INL introduced and INL calculated using New algorithm

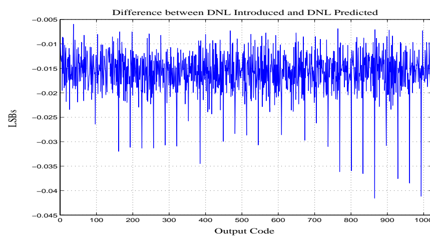

Fig. 4. Error in DNL predicted using New Algorithm

INL and the introduced INL is given in top portion of Figure 5. Once the errors in transition have been identified, the information can be used to correct them. The INL of the resultant converter after correction is shown in the bottom portion of Figure 5. Note that the INL in the ADC has been reduced from $\pm 4LSB$ before calibration to less than $\pm 0.15LSB$ after calibration. Results of multiple runs with different combinations of random values of resistances will be presented in the final paper.

In addition to a constant shifting error, a signal dependent error was introduced in V_{in2} using the following equation

$$V_{in2} = \delta_1 V_{ideal} + \delta_2 V_{ideal}^2 + \nabla S(1 + \gamma V_{ideal}) + \varepsilon \quad (11)$$

Further simulations with different number of samples per LSB, different shifting errors and input signal of varied linearity were similar to those presented here.

6. CONCLUSION

A new approach for a BIST solution for analog and mixed-signal circuits has been introduced. A modified histogram-based algorithm for evaluating the non-linearities of an A/D converter has been proposed. Unlike existing approaches, this method does not require generation of a precise and

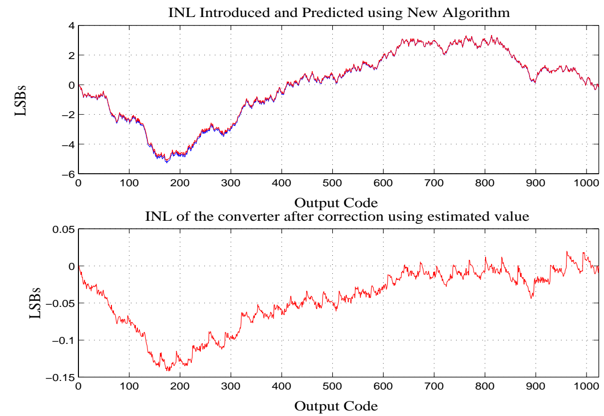

Fig. 5. INL using Iterative algorithm and INL after correction

highly accurate input stimulus. The entire system was modeled in MATLAB and simulation with various input conditions were performed. The results confirm the robustness of the algorithm. It is conjectured that this approach of using multiple imprecise and unknown input signals has applications to other common architectures like pipelined structures that may give even better results than presented here for either foreground or background test\ calibration schemes.

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