POSITIVE FEEDBACK GAIN-ENHANCEMENT TECHNIQUES FOR AMPLIFIER DESIGN

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ABSTRACT

In contrast to the widespread myth that positive feedback or even unstable open-loop amplifiers will produce unstable feedback amplifiers, it is shown that positive feedback amplifiers can be used for realizing stable and useful feedback amplifiers. The benefits of using positive feedback for DC gain enhancement without compromising the settling time or the frequency response of feedback amplifiers are discussed.

1. INTRODUCTION

Although implementations of positive feedback amplifiers occasionally appear in the literature [1][2], there is a widespread belief that systems that use positive feedback should be avoided because their sensitivity to process and environmental variations may cause them to become unstable [3][4]. This misconception is founded in the fact that standalone amplifiers using partial positive feedback do become unstable if too much positive feedback is applied. However, these amplifiers are rarely used in such a context. In practice, they will almost always be found embedded in a negative feedback configuration in which their stability is not an issue.

In this paper we will show how positive feedback can be exploited to enhance the DC gain of an amplifier without sacrificing its speed of operation. Although the concept is applicable to other applications, this paper will focus on applications of charge transfer such as switched capacitor filters or data converters.

In charge transfer circuits the critical amplifier performance parameters are the DC gain and the settling time. Large DC gains ensure the linearity of the charge transfer whereas fast settling ensures high system throughput.

Due to their ability to simultaneously achieve large DC gains and large gain-bandwidth (GBW) products, single-stage cascode amplifiers have traditionally found widespread use in charge transfer applications. With the reductions in power supply voltages associated with new and emerging processes, these architectures are becoming less viable. Recently, because of their ability to operate at lower supply potentials, two stage amplifiers have found use in charge transfer circuits [5][6]. Since it is anticipated that supply voltages will decline even further, new amplifier topologies that are compatible with low voltage supplies need to be developed. Amplifiers that use positive feedback for gain-enhancement may fill the void.

As a baseline for comparison, an amplifier with a dominant-pole response is configured in a standard negative feedback configuration. Next, the dominant-pole amplifier is replaced with one whose gain has been enhanced via the use of positive feedback. Finally, it is shown that positive feedback can be used for gain enhancement without incurring significant speed penalty.

2. BASELINE CASE

A dominant-pole amplifier configured in a standard negative feedback configuration is shown in Figure 1. The performance of this structure will form a basis for comparison with another structure that utilizes positive feedback to enhance its performance.

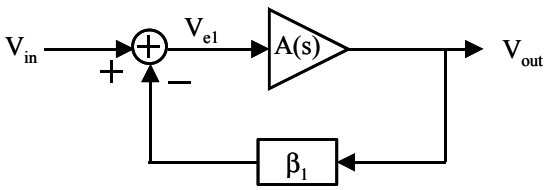

Figure 1 Standard negative feedback configuration

Assuming a frequency independent feedback network, β_1, the circuit of Figure 1 has the familiar transfer function:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A(s)}{1+\beta_1 A(s)} \tag{1}$$

For negative feedback, it is assumed that $\beta_1 > 0$. Because a properly compensated amplifier exhibits a dominant pole response, a first-order model is utilized to model the response of the amplifier of Figure 1.

$$A(s) = \frac{g_m}{g_o + sC} \tag{2}$$

where g_m and g_o are the small signal transconductance and output conductance of the amplifier respectively and C is the total capacitive load at its output. Substituting (2) into (1) yields,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_m}{(g_o + g_m\beta_1) + sC} \tag{3}$$

Examination of (3) reveals that the baseline structure has a DC gain, pole location, and GBW product given by (4), (5), and (6) respectively.

$$A_{0(baseline)} = \frac{g_m}{g_0 + g_m\beta_1} \tag{4}$$

$$P_{baseline} = -\frac{g_o + g_m\beta_1}{C} \tag{5}$$

$$GBW_{baseline} = \frac{g_m}{C} \tag{6}$$

Observe in (4) that for large amplifier gains (g_m/g_o) the closed loop gain of the baseline system converges on the desired value of $1/\beta_1$. The challenge, however, is realizing an amplifier that has sufficient gain to achieve the desired accuracy in new and emerging low voltage processes. The traditional techniques involve device stacking and are not viable. Amplifiers that use positive feedback to achieve the required gain enhancement are investigated next.

3. POSITIVE FEEDBACK STAGE

Figure 2 shows the schematic diagram of a positive feedback gain stage. The architecture is exactly the same as that of standard negative feedback configuration of Figure 1 except the polarity of the feedback is reversed. To ensure the feedback is positive, it is necessary that $\beta_2 > 0$.

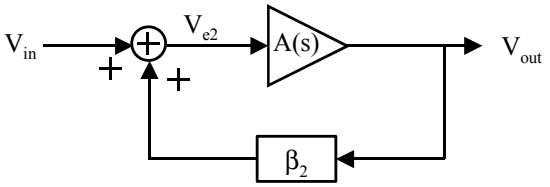

Figure 2 Positive feedback configuration

The transfer function of the positive feedback stage is the same as the negative feedback case with one sign reversal.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A(s)}{1-\beta_2 A(s)} \tag{7}$$

Making the same assumptions regarding the amplifier as was made earlier in (2), (7) becomes:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_m}{\varepsilon + sC} \tag{8}$$

where ε is defined as:

$$\varepsilon = g_o - g_m\beta_2 \tag{9}$$

The feedback factor β_2 is a degree of freedom that can be chosen, establishing the value of ε.

The pole for the positive feedback gain stage is located at:

$$P_{(\text{open-loop pos. fb})} = -\frac{\varepsilon}{C} \tag{10}$$

while the DC gain is given by:

$$A_{0(\text{open-loop pos. fb})} = \frac{g_m}{\varepsilon} \tag{11}$$

Choosing β_2 such that ε is small results in gain enhancement. Additionally, the DC gain of the amplifier diverges as ε approaches zero. Based on (9) and (11), the necessary condition for gain enhancement is given by:

$$|\varepsilon| < g_o \tag{12}$$

Applying too much positive feedback by increasing β_2 results in an ε sign reversal. As a result, the pole of the system given by (10) ends up in the right half-plane rendering the system unstable. This observation has been the primary argument against the practical use of positive feedback for gain enhancement because prior research only considered their standalone properties. However, if embedded in an overall negative feedback system, these problems are overcome as discussed in the next section

4. EMBEDDED POSITIVE FEEDBACK

Positive feedback can be exploited for gain enhancement and stability concerns can be eliminated by embedding the positive feedback gain stage in a standard negative feedback configuration as shown in Figure 3.

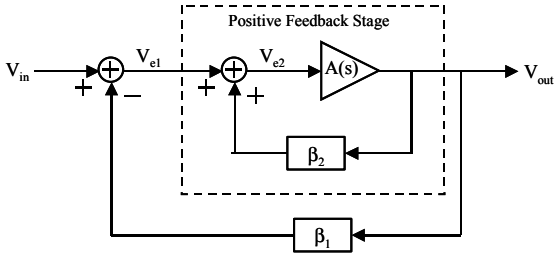

Figure 3 Positive feedback stage embedded in a standard negative feedback configuration

In this nested structure, the inner loop provides positive feedback for gain enhancement while the outer loop ensures the stability of the overall system by providing negative feedback.

The transfer function of the system of Figure 3 is given by:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_m}{(\varepsilon + g_m\beta_1) + sC} \tag{13}$$

Therefore, the DC gain of the overall system is:

$$A_{0(\text{embedded pos. fb.})} = \frac{g_m}{\varepsilon + g_m\beta_1} \tag{14}$$

and the pole location is given by:

$$P_{(\text{embedded pos. fb.})} = -\frac{\varepsilon + g_m\beta_1}{C} \tag{15}$$

If β_2 is adjusted so that $|\varepsilon|$ approaches zero, it can be seen from (14) that the overall gain of the system approaches the ideal value of $1/\beta_1$. Furthermore, since $g_m\beta_1 >> \varepsilon$, it can be observed from (15) that the stability of the system is assured. Unlike the positive feedback stage by itself, the overall nested system is not sensitive to the sign reversal of ε when too much positive feedback is applied.

5. COMPARISON

5.1 Gain Comparison

The gain enhancement due to the use of positive feedback can be found by taking the ratio of (11) to the open-loop gain of (2) evaluated at DC. The resultant enhancement is:

$$\frac{A_{0(\text{open-loop pos. fb.})}}{A(s)\big|_{s=0}} = \frac{g_o}{\varepsilon} \tag{16}$$

From (12) we know that the magnitude of ε is smaller than g_o. Therefore the gain enhancement factor is larger than 1.

5.2 Settling Performance

Various definitions of settling time exist. For this paper it is assumed that the settling time is the minimum amount of time that must elapse after a step change in the input before it can be guaranteed that the present and all future values of the output will lie within a specified tolerance of the output signal's asymptotic value. The specified tolerance is characterized by the parameter η as depicted in Figure 4.

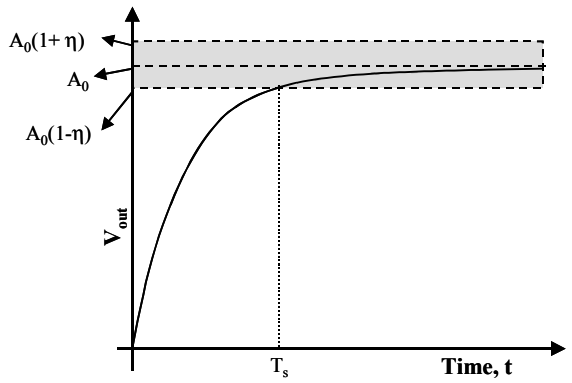

Figure 4 Graphical depiction of settling time

It can be show that the step response settling time, T_s, for the baseline case is given by:

$$T_{S(baseline)} = \frac{\ln(\eta)}{P_{baseline}} \tag{17}$$

Similarly, for the embedded positive feedback case:

$$T_{S(\text{embedded pos. fb.})} = \frac{\ln(\eta)}{P_{(\text{embedded pos. fb})}} \tag{18}$$

Insight can be gained by computing the ratio of the settling time in (18) to (17).

$$\frac{T_{S(\text{embedded pos. fb.})}}{T_{S(\text{baseline})}} = \frac{P_{baseline}}{P_{(\text{embedded pos. fb})}} \tag{19}$$

Substituting from (15) and (5), (19) reduces to

$$\frac{T_{S(\text{embedded pos. fb.})}}{T_{S(\text{baseline})}} = \frac{g_o + g_m\beta_1}{\varepsilon + g_m\beta_1} \tag{20}$$

From (12), the magnitude of ε is smaller than g_o resulting in the settling time of the embedded positive feedback scheme to be slightly larger than the baseline case. However, owing to the fact that $g_o << g_m\beta_1$, the difference is negligible implying insignificant penalty in using positive feedback for gain enhancement from a settling time point of view.

6. SUMMARY

New high-gain amplifier topologies that are compatible with low voltage supplies need to be developed. One amplifier gain enhancement technique that offers potential is the use of positive feedback. Amplifier gain enhancement via positive feedback has not yet gained widespread acceptance due to popularly held beliefs regarding the potential for instability. These conceptions are rooted in the fact that researchers have not considered using these structures as part of a larger system providing negative feedback. This paper shows how positive feedback can be used as a gain enhancement technique without significantly affecting the speed of operation.

ACKNOWLEDGMENT

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7. REFERENCES

[1] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*. New York, NY: McGraw Hill, 2001

[2] C. A. Laber and P. R. Gray, "A Positive-Feedback Transconductance Amplifier with Applications to High-Frequency, High-Q CMOS Switched-Capacitor Filters," *IEEE J. Solid-State Circuits*, Vol. 23, No. 6, pp. 1370-1378, Dec. 1988

[3] R. Wang and R. Harjani, "Partial Positive Feedback for Gain-Enhancement of Low-Power CMOS OTAs," *Analog Integrated Circuits and Signal Processing*, No. 8, pp. 21-35, 1995

[4] R. Gregorian, *Introduction to CMOS Op-Amps and Comparators*. New York, NY: Wiley, 1999

[5] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, Vol. 34, No. 5, pp. 599-606, May 1999

[6] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE J. Solid-State Circuits*, Vol. 35, No. 3, pp. 318-325, March 2000