RESISTORS LAYOUT FOR ENHANCING YIELD OF R-2R DACS

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ABSTRACT

A strategy to improve the yield of R-2R DACs by minimizing the effects of mismatch of resistors due to the local variations of sheet resistance is introduced. The approach is based on optimally distributing the area between the resistors. Simulation results show that the new strategy provide significant improvement in yield compared to the standard area allocation strategy of assigning equal area for each resistor bit-pair.

BACKGROUND

Layout plays a critical role in determining the yield of matching-critical circuits. To date, most practitioners and researchers have mainly considered the matching of two nominally identical devices with little attention focused on ratio matching or area assignment when the precise value of some resistors in a circuit is more critical than the value of others. A feedback amplifier with non-unity feedback gain is an example that presents a ratio-matching issue. In this work, it is shown that both ratio matching performance and area assignment of the resistors of a R-2R Digital - to - Analog Converter (DAC) influence the Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL).

Gradients and local random variations are the two major factors that contribute to errors in resistors. The effects of first or higher-order gradient effects on ratio matching can be minimized by appropriate placement, segmentation and common-centroiding of the layout [1-3]. After taking care of gradient effects, local random sheet resistance variations become the dominant contributor to ratio errors. The standard deviation of the resistance or capacitance in integrated devices due to local random variations [4,5] is inversely proportional to the square root of the area used for the components. For some applications requiring two or more ratio-matched components, the yield can be significantly improved [6] by appropriate area distribution. In the following, we will concentrate on the linearity of R-2R DACs by studying specifically the INL and propose a new area distribution strategy that will improve yield for a given total area. In these discussions, it will be assumed that appropriate segmentation and placement is used to make gradient effects non-dominant. A simple example shows the important role that area distribution plays in these structures. Consider the case of the 16-bit R-2R DAC of Fig.1 where the resistors without a subscript are nominally of value R and those with the '2' subscript are nominally of value 2R. It will be shown that by using the new area distribution strategy for resistor layout, the standard deviation of the INL will be reduced by 48% when compared to that attained with the standard area distribution strategy. Correspondingly, if the standard area distribution strategy was used along with the area needed to obtain a yield of 82%, the new area distribution strategy will improve the yield to 99% for the same total area. In the following, the new strategy is presented.

AREA-PARTITIONING

The standard deviation of the normalized resistance of any rectangular resistors of length L and width W can be expressed as [6]:

$$\sigma_{\frac{R_{ran}}{R}} = \frac{A_\rho}{\rho_N\sqrt{WL}} = \frac{A_\rho}{\rho_N\sqrt{A_R}} = \frac{K_\rho}{\sqrt{A_R}} \qquad (1)$$

where A_ρ is a process parameter that characterizes the random local sheet resistance variation, ρ_N is the nominal value of the sheet resistance, and A_R is the area of the resistor. For convenience, the ratio of A_ρ to ρ_N is denoted as K_ρ. Generally, there are two standard area allocation approaches for implementing a R-2R DAC. One we term the "conventional series" strategy. In the conventional series strategy, the "R" resistors are all implemented with

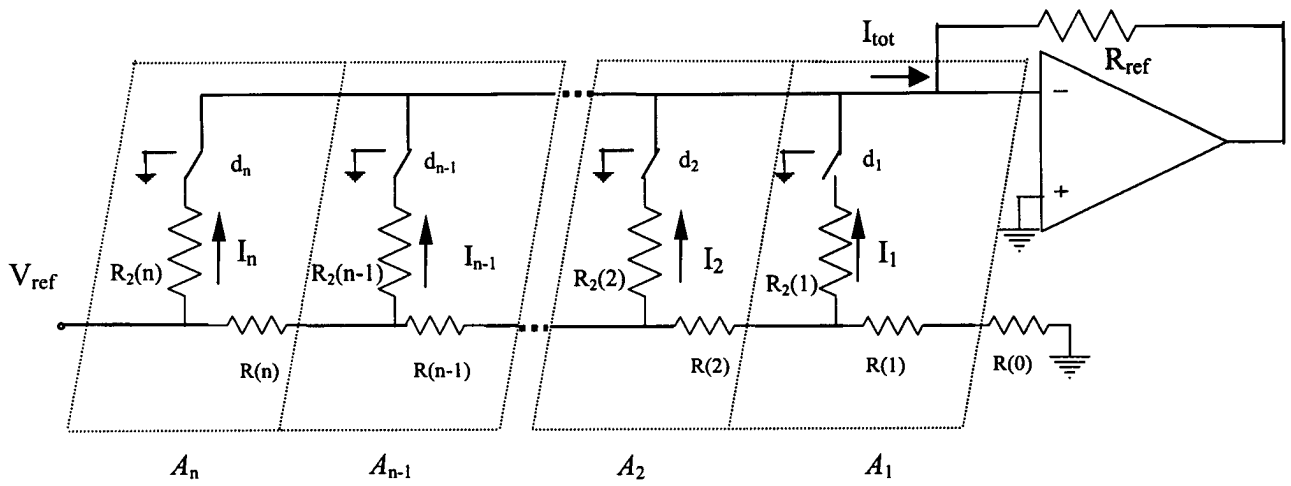

Fig.1 A basic n-bit R-2R DAC

the same standard resistor cell and the "2R" resistors are implemented with two of the same standard resistor cells in series. The second is termed the "conventional parallel" strategy, in which the "2R" resistors are all implemented with the same standard resistor cell and the "R" resistors are implemented with two standard resistor cells in parallel.

For the n-bit R-2R DAC depicted in Fig. 1, which has $N=2^n$ output levels, the endpoint INL at the k^{th} output is given as:

$$INL_k = (\sum_{i=1}^{n} d_i I_i - \frac{k}{N-1}\sum_{i=1}^{n} I_i)/\frac{1}{N} \qquad (2)$$

where the sequence $<d_i>$ is the digital input, k is the decimal equivalent of $<d_i>$ and I_i is the current flowing in the corresponding bit resistors. The INL is defined to be the maximum of the absolute values of the INL_k and is formally expressed as:

$$INL = \underset{0\le k\le N-1}{Max}\{|INL_k|\} \qquad (3)$$

The standard deviation of the INL is denoted by σ_{INL}. A comparison obtained by simulation of the standard deviation of the conventional series configuration and the conventional parallel configuration for the R-2R DAC for varying number of bits is shown in Fig.2. In this comparison, the total area for the resistor array was fixed for all R-2R ladders with the standard deviation of a resistor of this total area assumed to be 1% of nominal . From this plot, it is apparent that the conventional series layout will give an improvement in yield when compared with the conventional parallel layout. Intuitively, it is better to allocate more area to the "2R" resistors than to the "R" resistors. Thus it is apparent that area allocation plays a role in yield. Two questions naturally arise: What is the optimal area allocation between the "R" and "2R" resistors and how should the area be allocated between more significant and less significant bit cells for a given total area?

In order to better understand the contributions of each resistor, a statistical model of the R-2R DAC is needed. The INL is a random variable that represents the N^{th} order statistic of the N random variables $<INL_k>$ and the probability density function of such variables is analytically unwieldy. In what follows, we will attempt to develop insight into what resistors play the most important role in the overall INL.

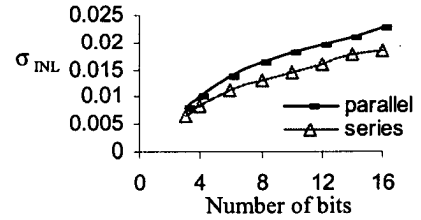

Fig.2 σ_{INL} vs. number of bits

With reference to Fig. 1, it can be shown analytically that the stand deviation of the INL_k, σ_{INLk} is a maximum at $k=2^{n-1}$ and at $k=2^{n-1}-1$. This can be expressed as:

$$Max(\sigma_{INLk}) = \sigma_{INL(2^{n-1})} = \sigma_{INL(2^{n-1}-1)} \qquad (4)$$

It is instructive to identify the major contributors to $Max(\sigma_{INLk})$. Although a formal expression for any n is possible, the expression for the case where n=3 does provide the desired insight. If we assume each resistor can be expressed as the sum of a nominal value and a random component, $R = R_{NOM} + R_r$, it follows from a tedious but straightforward derivation for a 3-bit R-2R DAC that

$$\text{Max}(\sigma_{INLk}) = \sigma\{\frac{4}{7}(\frac{3}{16}\frac{R(1)_r}{R_{NOM}} + \frac{3}{16}\frac{R(0)_r}{R_{NOM}} - \frac{5}{16}\frac{R_2(1)_r}{R_{NOM}} - \frac{1}{4}\frac{R(2)_r}{R_{NOM}} - \frac{3}{4}\frac{R_2(2)_r}{R_{NOM}} - \frac{R(3)_r}{R_{NOM}} + \frac{3}{2}\frac{R_2(3)_r}{R_{NOM}})\} \quad (5)$$

From this expression, it is apparent that the MSB resistors R(3) and $R_2(3)$ provide the largest contributions to the standard deviation. This can be generalized to show that the higher bit resistors make a larger contribution to the standard deviation of the Max(σ_{INLk})than the lower bit resistors. Although Max(σ_{INLk}) is not the standard deviation of the INL, this expression gives insight into the roles that different resistors play in determining the overall INL. Intuitively, the overall INL should be reduced if the standard deviation of those resistors that make the individual INL_ks large can be reduced. This can be achieved if more area is allocated to the MSB resistors and less area is allocated to the LSB resistors while keeping the total area constant. Of course, if too much area were removed from the LSB resistors, the contributions of these resistors to the overall INL would dominate thus again deteriorating the INL.

It is our goal in this study to determine a good area allocation strategy for minimizing the INL in R-2R DACs. Our ultimate goal is to obtain an optimal area allocation strategy. In what follows, we will focus on an 8-bit DAC but the results extend to DACs of any order. Referring again to Fig. 1, there is an "R" resistor and a "2R" resistor allocated to each bit. We will refer to the area allocated to these two resistors as the area associated with that bit. Let the area allocated to the p^{th} bit be denoted as A_p. Therefore, the first bit area is A_1, the second is A_2 and the MSB bit area is A_n for the n-bit DAC. For convenience, we allocated the extra termination resistor to the LSB bit cell. In each bit, the allocation of area between the "R" resistor and the "2R" resistor must also be determined. Denote the ratio of the area allocated to the "2R" resistor and the "R" resistor in the p^{th} bit as θ_p. An optimal area assignment strategy will thus determine the optimal values of A_1, ... A_n and θ_1, ... θ_n. With 2n variables and only one constraint, the total area, an analytical formulation of the optimal area allocation algorithm appears unwieldy. In what follows, we will consider a strategy that will give a good area assignment.

We will assume that the area ratio of the neighboring bits is m, i.e. A_2=mA_1, A_3=mA_2, ... A_n=mA_{n-1} and the area ratio of the 2R and R resistor inside each bit is θ. We have thus reduced a 2n-1 variable optimization problem to the 2-variable optimization problem of finding optimal values for m and θ. The standard deviation of the DAC is a function of θ, m and A_{total}. We will assume A_{total} is a fixed value. For relative comparisons, the values of A_{total} is arbitrary. For an 8-bit DAC, we first assumed θ =2 (this corresponds to the "conventional series" strategy discussed earlier) and then varied m by computer simulations to find a minimum in the standard deviation of the INL. We found that around m=1.8, the local minimum standard deviation in INL is achieved. Then m was fixed at 1.8 and θ was varied to obtain an optimal value of θ and the optimal value of θ is around θ =2. The corresponding simulation results are shown in Fig.3 and Fig.4.

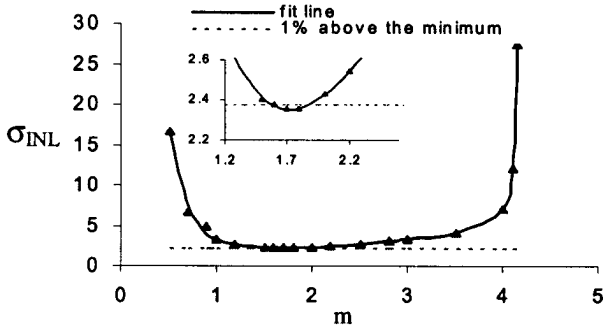

Fig.3 σ_{INL} vs. m curve of 8-bit R-2R DAC with θ =2

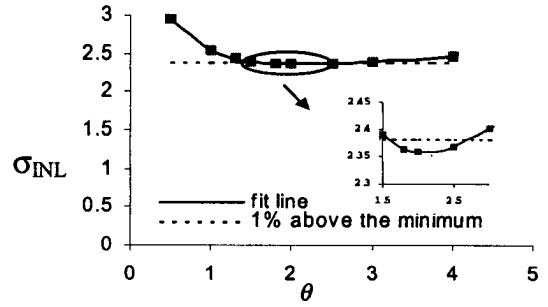

Fig.4 σ_{INL} vs. θ curve of 8-bit R-2R DAC with m=1.8

From these simulations, it is apparent that the standard deviation is much more sensitive to m than to θ for n= 8. The optimal m and θ are 1.8 and 2 respectively.

COMPARISON WITH EXISTING STRATEGIES

Optimal values of m and θ to minimize the INL for different values of n were obtained by a similar procedure. The optimal values for θ and m did not differ much from those obtained for n=8 for DACs with more

than a few bits. The optimal deviation is compared with the conventional series and the conventional parallel approaches in Fig.5. From this plot, it is apparent that the standard deviation is reduced more with higher DAC resolution. For a 3-bit DAC, the decrease is 8.1% and for a 16-bit DAC it is about 48% relative to what is attainable with the conventional series layout that allocated equal area to each bit.

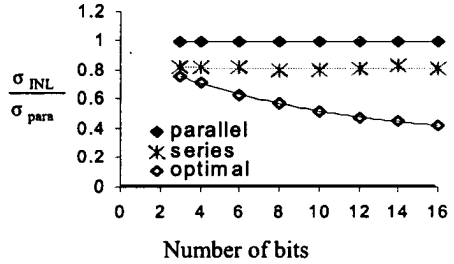

Fig. 5 The normalized σ_{INL} of R-2R DAC vs. the number of bits

ASSESSMENT OF YIELD

The soft yield [6] of a device that has a single stochastic error mechanism that is normally distributed can be expressed as:

$$Y = \mathrm{erf}\left(\frac{\varepsilon}{\sigma\sqrt{2}}\right) \qquad (6)$$

where, ε is the tolerable error and σ is the standard deviation of the relevant parameter. The actual yield can be expressed in terms of optimal yield Y_{opt}, by the expression

$$Y = \mathrm{erf}\left(\frac{\sigma_{min}}{\sigma}\mathrm{erf}^{-1}(Y_{opt})\right) \qquad (7)$$

It is apparent that the closer σ is to σ_{min}, the higher the yield is. If the area is fixed and parameters are set so that the optimal yield of a 16-bit DAC is 99%, then if follows from above that the conventional series area allocation approach would have a yield of 82%. Stated alternately, if a conventional series area allocation had a soft yield due to random variations in the sheet resistance of 82%, then the new area allocation strategy would provide a yield of 99% with the same total area allocated to the R-2R network. The concepts presented here can be extended to the allocation of area in capacitors and transistors in related applications.

In the formulation presented in this paper, the issues of contact resistance and edge definition were ignored. By allocating proportionally larger areas to the higher bits than to the lower bits, the question naturally arises about how the resistors should be geometrically formed. Even with the proposed area allocation strategies, the concept of using a reference resistor with segmentation still applies. The topic of how these reference resistors need to be combined to at least approximate the optimal area allocation strategy warrants further investigation.

CONCLUSIONS

The random variations of the sheet resistance degrade the accuracy of the R-2R DAC. A new method for distributing area between the resistors of different bits has been introduced that offers significant yield enhancement in R-2R DACs when compared to that achievable when equal area is allocated to each bit. The improvements in yield become more significant as the number of bits of resolution is increased.

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