A 0.6V ULTRA LOW VOLTAGE OPERATIONAL AMPLIFIER*

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ABSTRACT

A technique for low-voltage CMOS analog circuit design is presented in this paper. In this technique, voltage sources are added in series with the gates of the MOS transistors to lower the effective threshold voltages of the transistors. With the lowered effective threshold voltage, it is possible to build a host of analog circuit that operates with a decreased supply voltage. A 0.6V ultra-low voltage two-stage operational amplifier (Op Amp) was designed in a standard 3.3V 0.35u CMOS process to validate the technique. Compared to its counterpart operating with a 3.3V power supply at a much higher power level, the low-voltage Op Amp maintained the same gain-bandwidth product and most other key performance parameters.

I. INTRODUCTION

Low-voltage circuit design has been of a topic of considerable interest in recent years. This interest is oriented primarily by the inherent reduction in supply voltages available in fine feature processes and the potential for a reduction in power dissipation. This work focuses on a technique for operating at supply voltages around threshold voltage level in a standard process without requiring modifications that include special low threshold transistors.

In our approach, we build a "virtual" transistor by adding a voltage source to the gate of the "real" transistor so that the effective threshold voltage of the "virtual" transistor can be lowered and adjusted dynamically to compensate for process and temperature variations. With this technique, it is possible to build ultra-low voltage circuits that operate with supply voltages that approach the threshold voltages of the devices.

Several approaches have been reported to achieve low voltage strong inversion operation in standard processes. These include of the use of bulk-driven transistors [1], floating-gate transistors [2] [3] and dynamically biased stages [4]. These techniques have drawbacks. Floating-gate transistors have a smaller g_m and a larger output conductance than conventional transistors and may require special process to make this technique practically viable. Bulk-driven transistors experience a reduction in gain bandwidth product and a worse frequency response because of the substantially smaller g_m. Dynamically biased transistors have not been reported at very low supply voltages. The Op Amp in [4] worked at 1.2V power supply with 0.75V threshold voltage process.

A fundamental building block in analog signal processing is the operational amplifier. To demonstrate our technique, we designed a 0.6V operational amplifier in a 0.35u standard 3.3V CMOS process. It uses the basic two-stage configuration with an N-channel differential input stage. Our design goal was to maintain the same gain bandwidth product compared to a counterpart at the standard 3.3V power supply for the process. The core of the low-voltage Op Amp has been designed to draw the same current from the 0.6V power supply as the counterpart Op Amp draws from the 3.3V supply.

With some power consumption in the supporting circuits, the total power consumption of the low-voltage Op Amp is roughly 20% of that of the 3.3V counterpart.

The basic idea of this low voltage technique is explained in Section II together with the core circuits of the ultra-low voltage Op Amp. The overall structure of the Op Amp and the supporting circuits are discussed in Section III. In Section IV, simulation results and comparisons are given.

II. THRESHOLD VOLTAGE TUNING

Generally the minimum supply voltage is limited by the threshold voltage and the saturation voltage (V_{DSAT}) of the MOS transistor for operation in the strong inversion region. For a typical CMOS process with a threshold voltage around 0.7V, the minimum power supply voltage that researchers have reported even modest success has been around 1.5V.

If we can practically lower the threshold voltage to a much smaller value, the potential will exist for building low-voltage analog circuits. As shown in Figure 1, the basic concept of this low-voltage technique is very simple. A voltage source is added to gate of each transistor results in a "virtual" transistor with a lowered

* This work was supported, in part, by NSF, SRC and National Semiconductor Inc.

threshold voltage $V_t^{'}$ where $\left|V_t^{'}\right| = \left|V_t\right| - V_{dc}$. With this approach, the low threshold transistors will have the same g_m and g_o if biased at the same drain current level.

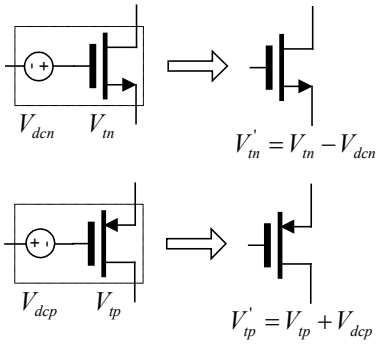

Figure 1. Threshold voltage tuning scheme

A low voltage Op Amp core using this technique is shown in Figure 2. It is a traditional two-stage architecture. Each transistor is connected with a voltage source or a shared voltage source at the gate. A total of five voltage sources are used in this design. R_c and C_c comprise the well-known miller compensation network. The resistor is used to eliminate the effect of the right-half-plane zero resulting from feedforward through the compensation capacitor C_c.

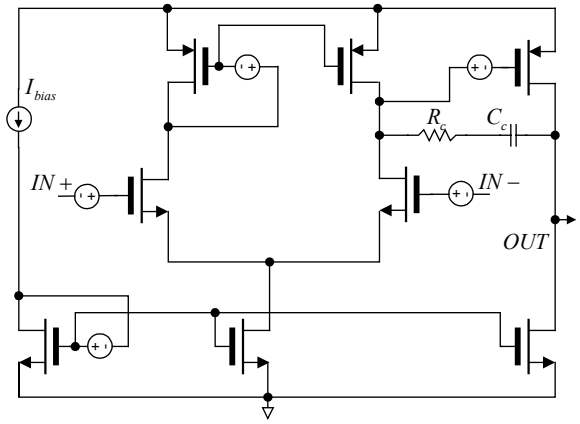

Figure 2. Ultra-low voltage Op Amp Core

III. DESIGN OF THE LOW-VOLTAGE OP AMP AND ITS SUPPORTING CIRCUITS

In order to implement this low-voltage technique, several supporting circuits are needed to realize the voltage sources. Figure 3 shows a block diagram of the low-voltage Op Amp. Although the supporting circuitry shown inside the dotted box may appear to dominate that of the Op Amp core itself, the power dissipation in the supporting circuitry is small compared to that in the core circuit and the same supporting circuitry can be used to condition a large number of transistors.

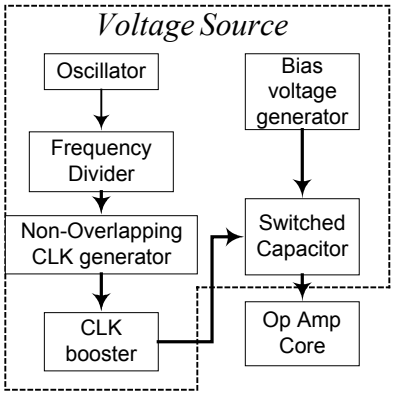

Figure 3. Block diagram of the ultra-low voltage op amp

The series voltage source design for an n-channel transistor is shown in Figure 4. The bias voltage V_{dc} periodically charges the capacitor C_1 to keep the voltage between "IN" and "OUT" constant. ϕ_1 and ϕ_2 are non-overlapping clocks. During ϕ_1, C_1 is connected to the signal path and shares its charge with C_2. During ϕ_2, C_1 is disconnected from the signal path and is charged by V_{dc}. For p-channel devices, the polarity of the bias voltage V_{dc} is inverted.

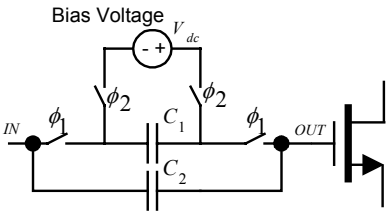

Figure 4. Voltage source design

Since the input impedance of the MOS transistor is high and the switch leakage current is very small, the frequency of ϕ_1 and ϕ_2 can be low to reduce noise injection.

3.1 Switch clock generator

The left half of Figure 3 shows the circuits that generate the non-overlapping clocks ϕ_1 and ϕ_2. The oscillator was implemented as a 7-stage ring oscillator shown in Figure 5(a) worked at the 0.6V supply. All transistors in the oscillator operate in either the weak saturation or the

sub-threshold region. Although the oscillation frequency varies substantially with process and temperature, the switched capacitor voltage source is tolerant of a very wide range of switching frequencies.

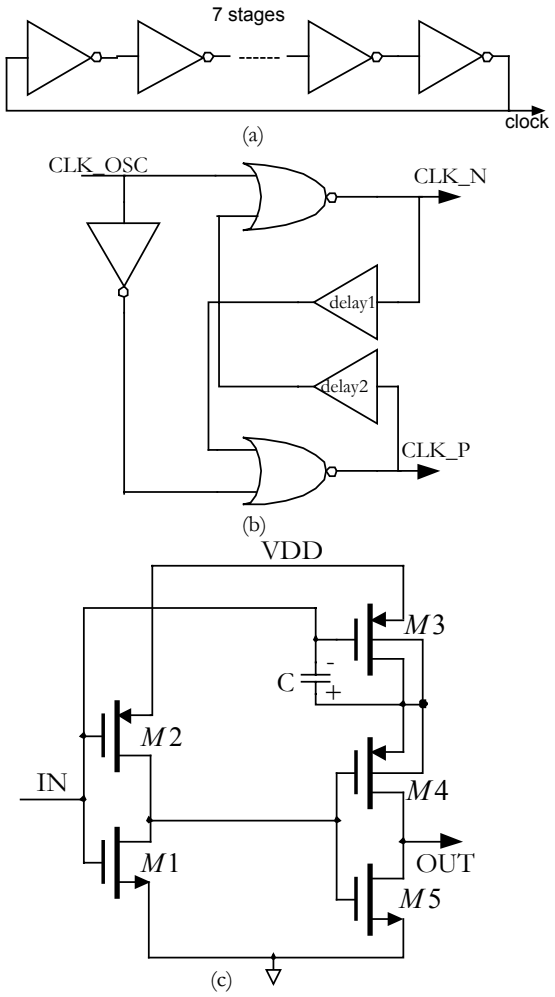

Figure 5. (a) Oscillator; (b) Non-overlapping clock Generator; (c) Clock booster (One stage)

3.2 Frequency divider

The frequency of the ring oscillator is in the 0.5MHz range. A 64:1 frequency divider was used to reduce the clock frequency. The frequency divider used a conventional D flip-flop based architecture. Like the case in oscillator, all transistors in the divider are working in either weak saturation or sub-threshold region.

3.3 Non-overlapping clock generator

The clock signals ϕ_1 and ϕ_2 must be non-overlapping. The circuits in Figure 5(b) were used to generate the non-overlapping clock signals.

3.4 Clock booster Circuit

The switches in the voltage source circuits are implemented by NMOS transistors. In order to turn them fully ON or OFF, the control clock swing of 0.6V is not adequate. So a clock booster was used to boost the clock signal swing from 0.6V to about 2.5V level. The clock booster circuit is shown in Figure 5(c). When the input is low, M3 and M5 are ON and M4 is OFF. Capacitor C is charged to VDD and the output is zero (ground). When the input becomes high, M3, M5 are OFF, M4 is ON, the voltage level at C- becomes VDD and the voltage level at C+ becomes 2VDD and it is transferred through M4 to the output. Theoretically, this booster circuit can double the clock swing. But we can see that when the voltage at C+ becomes higher than VDD, the charge will start leak through M3 because the drain voltage of M3 starts to become higher than source voltage. So in simulation, depends on the value of VDD compared to threshold voltage V_{tp}, the swing of the clock can be boosted to about 1.2VDD – 1.8VDD in one stage. In our design, 3 stages of booster are used to boost the swing of the clock from 0.6V to about the 2.5V level which is sufficient to fully turn the switches ON and OFF.

3.5 Bias voltage generator.

There are two objectives for designing the bias voltage generator. First, it should provide a voltage that is roughly 0.2V below the threshold voltage. Second, it must provide enough current so that during the charging of C_1, the capacitors can be sufficiently charged. The circuit that we used was a simple self-biased circuit working under 0.6V.

There is an issue associated with the switches in the voltage sources that we should be aware of. We used a standard N-well CMOS process. All the switches used in the voltage sources are implemented with NMOS transistors and their bodies are all tied to the ground. For the voltage sources that are connected to the gates of the PMOS transistors, negative voltages may be transferred through them. This forms a forward-biased PN junction in the NMOS transistors. We tried to use PMOS transistors as switches in those cases. But it requires another set of clock generator to get negative level clocks. Furthermore, the forward-bias voltages of the junctions in our cases are around 0.2V-0.3V which are

way below the conducting voltage for diode. Total leakage current from the simulations was below 1uA. So we still use the NMOS transistors for all the switches.

IV. SIMULATION RESULTS AND COMPARISON

The low-voltage op amp was designed in a standard 3.3V 0.35u CMOS process. The nominal threshold voltages are $V_{tn} \approx 0.55V$ and $V_{tp} \approx 0.6V$.

In order to compare the performance of the low-voltage Op Amp, a normal two-stage Op Amp was designed with 3.3V power supply. The 0.6V counterpart was designed without changing the transistor sizes or bias currents.

Simulation results of the low-voltage Op Amp based on BSIM level 49 models and extracted layout parasitics are summarized in Table 1.

Process	Single poly, 4 metal 0.35u CMOS
Power supply range	0.6V-0.75V
Temperature range	0°C - 100°C
Power consumption (all circuits)	42uW@0.6V (typical) 100uW@0.75V (typical)
Gain Bandwidth Product	8MHz@0.6V (typical) 22MHz@0.75V (typical)

Table 1. Key parameters of the low-voltage Op Amp

At power on and with zero initial charge on the capacitors, the low-voltage Op Amp took about 20 clock cycles to settle to within 5% of the final bias points. The Op Amp works reliably over temperature and process variations and at up to 0.75V power supply voltages.

The comparison of the low-voltage Op Amp to its counterpart at 3.3V is shown in Table 2. (typical case)

Power Supply	Gain-Bandwidth Product	Phase Margin	DC gain	Power consumption (Total)
0.6V	8MHz	58 deg	79dB	42uW
3.3V	8.4MHz	57 deg	86dB	220uW

Table 2. Comparison of the low-voltage Op Amp with a counterpart 3.3V Op Amp

V. CONCLUSION

A new approach to low-voltage CMOS design was introduced. In this approach, voltage source is added in series with the gate of the transistor so that the effective threshold voltage can be lowered. An ultra-low voltage Op Amp was designed to demonstrate this technique. Simulation results show it maintains the key small signal parameters when compared to its counterpart operating with a normal supply voltage, but the low voltage circuit exhibits a major decrease in power dissipation.

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