A HIGH GAIN AMPLIFIER USING A CASCADING ARCHITECTURE

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ABSTRACT

High gain amplifiers with fast settling times are needed for high-speed data converter applications. Cascading amplifiers is generally a good way to achieve the desired open loop gain however; stability and settling speed become a concern. A cascading architecture that is inherently stable and maintains good settling performance was previously discussed. In this paper, a transistor level three stage implementation is presented that achieves over 100dB of gain while maintaining good settling performance.

1. INTRODUCTION

Data converter circuits require fast settling and high gain amplifiers. The high gain is needed for the output of the amplifier to settle accurately to the desired final value. Cascode amplifiers are widely used because they satisfy both requirements. The problem with using the cascode amplifiers is the limitation that occurs due to the need of a high supply voltage to provide an acceptable output signal swing. This becomes a problem especially with the technology pushing towards smaller device sizes and lower supply voltages. An alternative that does not require large supplies is to cascade amplifiers to achieve the desired gain. Various cascade feed forward schemes already exist [1][3][4][5]. However, they introduce pole-zero pairs that exhibit imperfect cancellation. This causes the appearance of slow settling components in the transient response. Unless the magnitude of the effects are sufficiently small, long settling time constants can not be tolerated in many applications.

A method for cascading amplifier stages to achieve the desired gain and at the same time maintain comparable settling time to that of a basic amplifier was previously presented. In this paper a transistor level implementation of the cascaded architecture is discussed. It is shown that a stable high gain amplifier (100+ dB) can be obtained from cascading simple amplifier stages and the compensation is inherent in the system.

2. ARCHITECTURE BACKGROUND

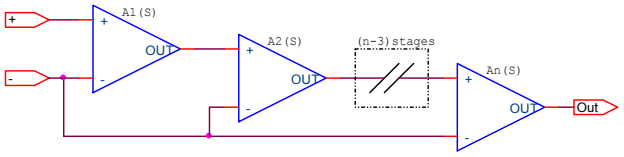

Figure 1, Cascaded amplifier architecture

A previous paper [6] introduced a new cascading structure that is inherently stable. The architecture is composed of (n-1) identical amplifiers cascaded together and the output is again cascaded into an amplifier that has a gain-bandwidth product modestly higher than the rest of the amplifiers to keep the overall structure stable in the presence of negative feedback. The amplifiers are cascaded in the manner shown in figure 1.

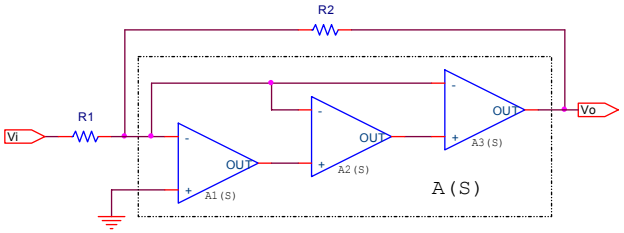

Figure 2, Three stage cascaded amplifier in inverting configuration

Considering a three stage cascade in closed loop as shown in figure 2 and writing the closed loop transfer function, we get the following equation:

$$\frac{V_o}{V_{in}} = \frac{-(R_2/R_1)(1+\tau_1 s+\tau_1\tau_2 s^2)}{1+\tau_1 s+\tau_1\tau_2 s^2+\left(1+\frac{R_2}{R_1}\right)\tau_1\tau_2\tau_3 s^3} \quad \text{..... (1)}$$

where,

$$\tau_i = \frac{1}{GB_i} \quad \text{..... (2)}$$

When in closed loop, the two zeros will cancel two of the poles leaving only one dominant pole in the system and no extra compensation is required. However the condition for stability for the closed loop transfer function is $\tau > 2.7\tau_3$ where $\tau = \tau_1 = \tau_2$ (since the first two stages are identical.) Figure 3 below shows the root locus of the structure's transfer function.

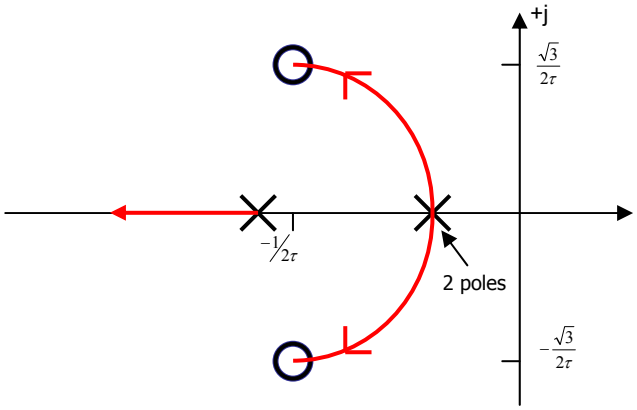

Figure 3, Closed loop pole/zero plot

The open and closed loop zeroes are located at half the gain-bandwidth of the first and second stage amplifiers. The dominant pole location is a variable that can be changed by increasing or decreasing the third stage pole location. As will be shown, the location of the dominant pole relative to the zeroes is a very critical design parameter for the structure.

High DC gains can be achieved by this structure but there is a cap on the maximum closed loop gain. Since the zeros stay constant whether in open loop or closed loop, if the thirst stage pole happens to be at a much lower frequency than the frequency of the zeroes, the possible stable closed loop gain will drop to a very low value if not less than 0dB making the amplifier useless in closed loop. So it is important to carefully design the pole frequency of the third stage.

It is also worthwhile to mention that this amplifier is not open loop stable but this is not a concert because it is closed loop stable and phase margins of 90 deg are achievable.

3. CASCADE AMPLIFIER DESIGN

The architecture used makes it easy to design the transistor level implementation since no special features are required in the individual amplifiers. The only architectural requirement is that the last stage must have a higher gain-bandwidth product that the previous identical stages. How much higher, depends on how much closed loop gain is required from the overall amplifier and how fast is the amplifier required to settle.

If the gain-bandwidth of the third stage (GB_3) is much higher than the gain-bandwidth of the first two stages ($GB_{1,2}$), we will maximize the possible closed loop gain but at the same time we will be jeopardizing the settling performance of the amplifier. This is because the closed loop dominant pole will no longer be close to the zeroes and any mismatch in the pole-zero cancellation shown in figure 3 will add a considerable slow settling component to the step function. See figure 4 below.

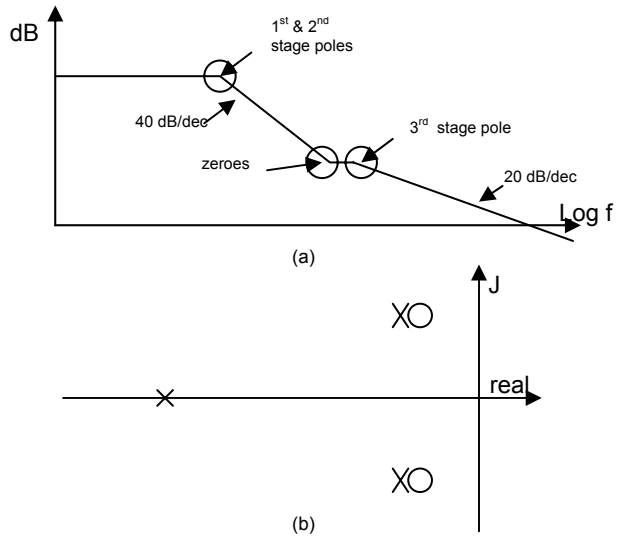

Figure 4, Open loop gain plot (a) & pole-zero plot (b) for $GB_3 >> GB_{1,2}$

On the other hand, if the gain-bandwidth of the third stage (GB_3) is close to the gain-bandwidth of the first two stages ($GB_{1,2}$), the step response will have a large overshoot and to get the amplifier to settle fast, we will need to design all three stages to have high gain-bandwidths and this will require a considerable amount of power. See figure 5 below.

The solution in to find the medium point where we can balance the settling time, DC gain, overall bandwidth of the amplifier, possible closed loop gain and power dissipation. To do so, a spreadsheet was generated to look at how these variables are affected with varying all the input parameters. The design presented in this paper was optimized for all the above mentioned parameters, in particular to achieve 135dB of gain and 100MHz unity gain frequency. We could have just as well optimized the design for only one, two or three of the parameters. For example if a faster settling response is desired, it could be done but it will cost more power.

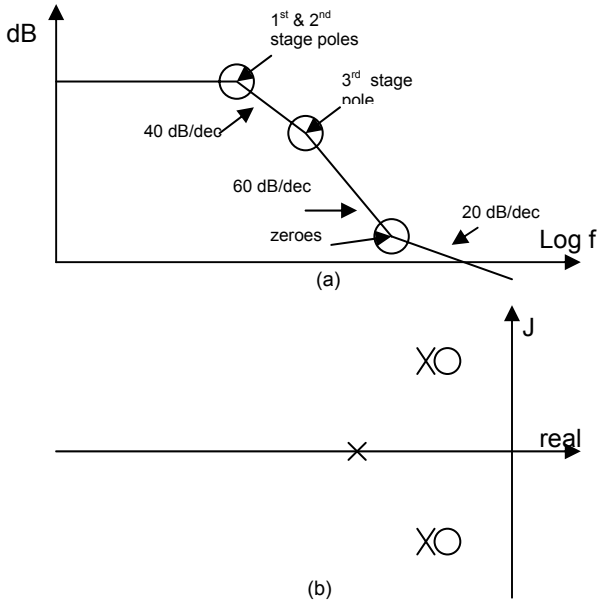

Figure5, Open loop gain plot (a) & pole-zero plot (b) for $GB_3 > GB_{1,2}$

The circuit was designed in a 0.5µ process. A simple five transistor Transconductance Amplifier was used for each stage of the amplifier. Figure 6 shows the over all schematic and figure 7, shows the schematic for each of the first and second stages.

A small load capacitor was added to each of the first two stages to control their pole location. The transistors of the first two stages are not as big as those of the third stage because the first two stages have a lower gain-bandwidth and they drive much smaller capacitors than the third stage (which was designed to drive 20pF.) This combination of lower bandwidth and lower load capacitance allows for a minute amount of power to be dissipated in these stages relative to the third stage.

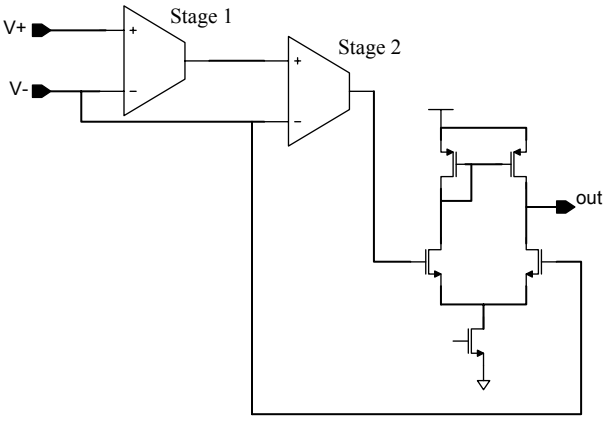

Figure 6, Implemented circuit

A simple five transistor implementation was used for the third stage so as not to add an extra pole in the system which would need to be compensated.

The first two stages were designed to have a tail current of 20µA verses 8mA needed for the third stage. In other words the power dissipated in the first two stages combined is 200µW while the power dissipated in the third stage is 40mW (V_{DD} = 5V.)

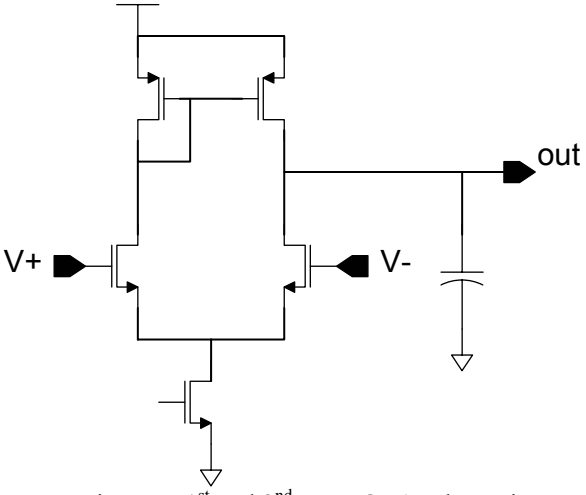

Figure 7, 1st and 2nd stage OTA schematic

In the next section we will discuss the results obtained from simulating the amplifier design.

4. SIMULATION RESULTS

All simulations were run using HSpice level 49 models. The amplifier was simulated in the inverting unity gain configuration.

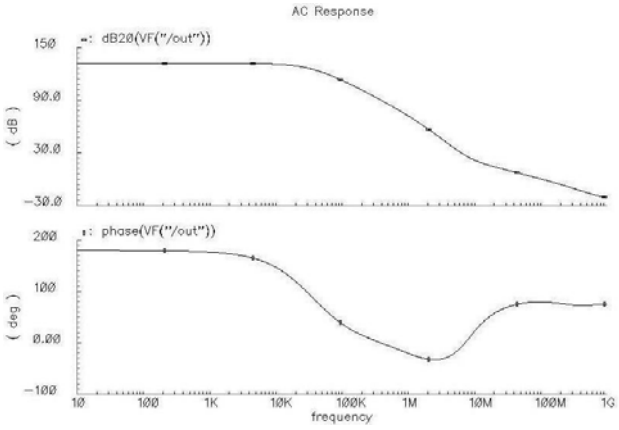

Figure 8, Open loop characteristic

A DC gain of 131 dB was achieved with a unity gain frequency of 102 MHz. Figure 8 above shows the open

loop bode plot of the amplifier while figure 9 below shows the step response (1V step.)

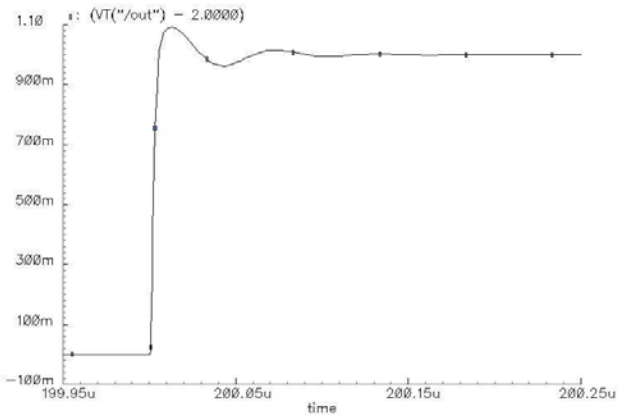

Figure 9, Inverting unity gain step response

Table 1 below summarizes the results obtained from simulating the amplifier while table 2 shows the settling performance of the amplifier.

Table 1, Table of amplifier characteristics

Process	0.5 µ
VDD (V)	5
Cload (pF)	20
DC Gain (dB)	131
Unity gain freq. (MHz)	102
Power Dissipation (mW)	40.2
Output Signal Swing (V)	0.22 - 4.76
Slew rate (V/µs)	400

Table 2, Amplifier settling performance

% settled	Time to settle (ns)
10	6
1	87
0.1	141

It is important to point out that the amplifier settling performance could be improved if the power budget is increased.

5. CONCLUSIONS

In this paper a cascaded amplifier circuit that achieves over 120dB of gain and a unity gain bandwidth in excess of 100MHz was presented. The design was optimized for one set of conditions but it can easily be modified to enhance any desired characteristic. The circuit was comprised of basic amplifiers that are not necessarily high gain but an overall high gain is achieved by cascading these amplifiers. No complicated compensation schemes were required for stabilizing the circuit.

6. REFERENCES

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