A DYNAMIC ELEMENT MATCHING APPROACH TO ADC TESTING

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ABSTRACT

A dynamic element matching approach to ADC testing is presented. With this technique a highly nonideal DAC is used to generate an excitation for the DUT. Dynamic element matching is used to create a statically precise excitation from imprecise components. Simulation results show this approach can be used to accurately measure the performance of an ADC. This technique offers potential for use in both production test and BIST environments.

1. INTRODUCTION

Testing analog-to-digital converters (ADC) is a non-trivial task since an accurate input is needed. This input is typically generated by a digital-to-analog converter (DAC) with higher resolution than the device under test (DUT). In other words, the real challenge is designing the circuit to test the part, since it needs to have higher resolution and linearity than the DUT. This approach is not suitable for BIST applications since the DAC needs more silicon area than the ADC to be tested.

It is known that dynamic element matching (DEM) can be used to generate analog signals with high SFDR using a moderately low resolution digital-to-analog converters (DAC)[1]. This becomes possible due to this technique's decoupling of the DAC noise from the DAC input. In [1], it was shown that in a DAC with static errors, performance can be improved using randomization DEM. This characteristic of the dynamic element matching technique makes it a suitable candidate for generating the input of a DUT using a not-so-accurate DAC. The focus of this work is to use a low accuracy DAC with DEM to characterize an ADC with higher accuracy.

In the proposed scheme, the DAC will have more bits than the ADC but is not ideal and has some static errors caused by mismatches. Static mismatch errors can be caused by process variations and result in a nonlinear transformation in the DAC, called integral nonlinearity (INL), which degrades the DAC performance. Similar mismatches in an ADC contribute towards its INL. Although any number of ADC performance parameters may be characterized, INL will be used to test the proposed scheme.

This paper is organized as follow. Section 2 explains how the ADC is implemented and how the INL is calculated. Dynamic element matching method is explained in Section 3. Section 4 gives details about the random DAC, while in Section 5 some simulation results are shown and discussed. The summary is in Section 6.

2. ADC MODEL AND INL CALCULATION

To test our idea, a flash ADC is going to be characterized through the INL measurement. A simple implementation of a flash ADC is shown in Figure 1.

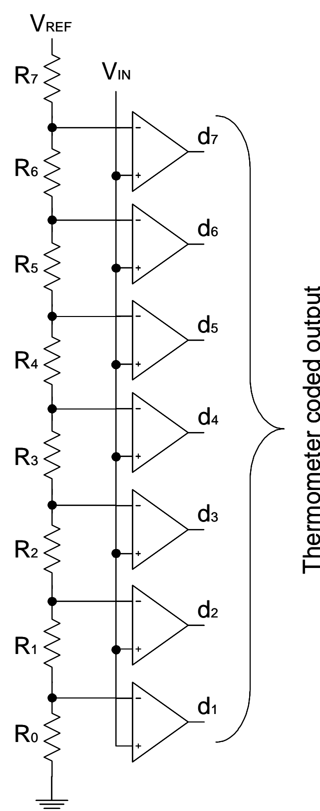

Figure 1: A 3-bit flash ADC.

The input signal in to a flash converter is fed to the comparators in parallel. Each comparator is also connected to a resistor string, as shown in Figure 1. The output of the comparator is set to one if the input value is bigger than the voltage of the resistor string. The output code obtained is called thermometer code. Resistor mismatch and comparator errors are the two primary sources of static errors contributing towards the INL of the ADC. For the purposes of this work, comparator mismatches are ignored and only the static error caused by resistor mismatches is modeled.

There are several alternative but similar definitions of INL of an ADC. The endpoint fit line method was picked for this work. In this definition, the INL, as given in (1), is defined to be the maximum deviation of the ADC's transfer curve from the endpoint fit line. With this definition, the INL of an ideal ADC is 0.5 LSB.

$$INL = \max\left(\left|\frac{V_o - V_{FITLINE}}{V_{LSB}}\right|\right) \quad (1)$$

An example with a non-ideal ADC transfer curve and its corresponding fit line is shown in Figure 2. It is a 3-bit flash ADC with a voltage reference equal to 2V.

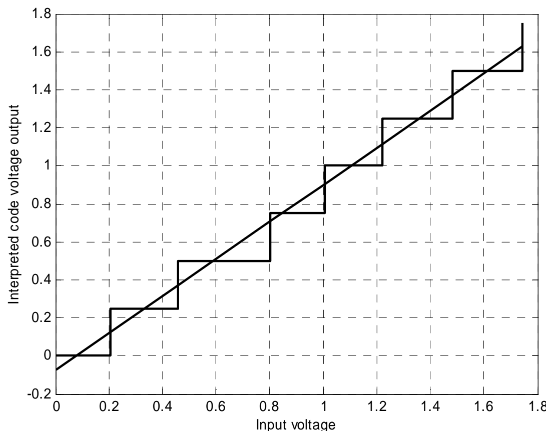

Figure 2: A nonideal ADC transfer curve and its endpoint fit line.

As can be seen in Figure 2, the INL has maximum values in the transition points when the output changes from one code to the next one. These are the points that need to be measured for characterizing the ADC under test.

3. DYNAMIC ELEMENT MATCHING

Element matching errors are inevitable due to inherent process variations. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The dynamic element matching technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average the element values are nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated.

Existing DEM structures are used in real-time circuits, making difficult to fully exploit DEM potential. Our approach is different since the DEM is not in the DUT but in the signal generator, eliminating the real-time concern when using DEM.

4. A DAC WITH DYNAMIC ELEMENT MATCHING

In order to construct a DAC with dynamic element matching two different approaches can be found in the literature [1- 2]. One is the partial randomization DEM. The other is the so called full randomization DEM. This latter technique is used in this work and will be explained next along with some modifications.

The full randomization DEM will be explained using a 3-bit current mode thermometer-coded DAC as an example as shown in Figure 3.

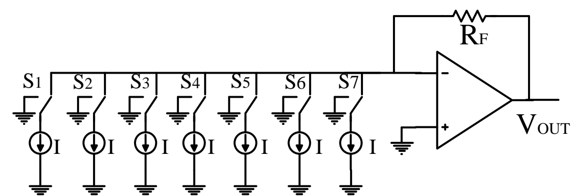

Figure 3: A 3-bit current mode thermometer-code DAC.

In this case when all the switches are connected to ground the output corresponds to the digital word zero. To have the output voltage for a digital one, one switch needs to be connected to the negative input of the Operational Amplifier (opamp). The idea is to pick the switch randomly so that output error behaves as white noise uncorrelated with the input digital word [3]. The same idea is used for the other input digital words, where the switches to be closed are selected randomly.

Our approach uses this technique but also take advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static view point. Since the output of the DAC is used as the input of the ADC, the same digital word using different randomly chosen current sources is going to be input to the ADC more than once. The ADC's output for each one of them is then stored for calculating the INL later. In this way the real-time limitations are

eliminated and an arbitrarily accurate input signal can be generated.

The INL is calculated using the average value obtained for that particular transition point of the DAC that is input to the ADC. Since each individual value was generated using different combination of current sources, the average will be more accurate and will compensate part of the mismatching.

5. SIMULATION RESULTS

To verify our approach we simulated two flash ADCs with resistor mismatches. These ADCs are tested using simulated current mode thermometer-coded DAC with static error mismatch in the current sources. The mismatch in all cases has a Gaussian distribution with a standard deviation of 0.2 and a mean value of 1.

The results shown in Table 1 and Table 2 were calculated using two different sets of 100 different DACs. Each set is used to characterize one of the ADC. As is stated in the tables, 100 different 6-bit DACs were used to characterize a 3-bit ADC, while 10-bit DACs were used to characterize a 7-bit ADC. In both cases the DACs used to estimate the INL have high nonlinearities as we wanted.

Each DAC has different current sources, although all of them have mismatches. For each DAC the current sources are picked randomly following the DEM approach and each digital word is input to the ADC (with different current sources configurations) P times. Also the INL is calculated and then compared to the actual INL of the ADC. This actual ADC INL is known since we know the ADC. For every DAC, an INL error is calculated using the difference between the actual ADC INL and the one estimated using our approach. The average of the INL error for 100 different DACs and the worst error en the INL estimation are the values shown in Table 1 and Table 2.

Table 1: Results for a 3-bit ADC and 6-bit DACs.

3-bit ADC		
6-bit DAC		
Average DACs INL: 1.229023 LSB		
Worst DAC INL: 2.592191 LSB		
ADC actual INL: 0.832937 LSB		
P	Average error in ADC INL estimation [LSB]	Worst error in ADC INL estimation [LSB]
1	0.078160	0.292063
4	0.051692	0.183192
16	0.019900	0.081034
32	0.018850	0.074748

In Table 1 the results for a 3-bit ADC being characterized by a 6-bit DAC are listed. As was explained before, different DACs were used; all of them with mismatches resulting in INL up to 2.6 least significant bits (LSB). When only one combination is used for each input of the ADC (P = 1) the error in the INL estimation of the ADC can be as bad as 0.3 LSB. This means that the INL estimated is in the worst case equal to 0.83 LSB $\pm$ 0.3 LSB, where 0.83 LSB is the real ADC INL. However, when P is equal to 32, the error in the INL estimation is at most equal to 0.07 LSB.

Table 2: Results for a 7-bit ADC and 10-bit DACs.

7-bit ADC		
10-bit DAC		
Average DACs INL: 5.812044 LSB		
Worst DAC INL: 12.846913 LSB		
ADC actual INL: 2.503805 LSB		
P	Average error in ADC INL estimation [LSB]	Worst error in ADC INL estimation [LSB]
1	0.147856	0.45451
32	0.08904	0.264553
128	0.083385	0.142052
512	0.083089	0.115538
1000	0.084044	0.107552

Same behavior is observed in the results shown in Table 2. INL estimate improves when the same DAC input digital word with different sources connected randomly is input to the ADC. There is always an error present since the input is generated by a DAC and is not continuous.

From these results we can observe that minimal performance requirements are needed in the DEM DAC use to generate the input signal to the ADC. This make the approach practical for the use in a BIST environment since the area requirements for a no accurate ADC are not high.

6. SUMMARY

In this paper we state and validate through simulations a technique to estimate the INL of an ADC using a DAC less accurate than the ADC. This technique uses DEM and also redundancy of samples, obtaining an arbitrary precision since DEM is not use in real-time single path. We believe that this technique can be used for testing ADCs with low quality DACs and can ease design of the testing circuits. Then the technique is well suited for BIST applications and production test environments.

7. REFERENCES

[1] Jensen H. T. and Galton I., "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis." *IEEE Transactions on Circuits and Systems,* Vol. 45, pp. 13-27, January 1998.

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