

# Optimal Loop Parameter Design of Charge Pump PLLs For Jitter Transfer Characteristic Optimization\*

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## Abstract

An optimal loop parameter design method of charge pump PLLs for jitter transfer characteristic optimization is proposed. Based on the linear model of charge pump PLLs, the relationship between PLLs' loop parameters and jitter transfer characteristic is illustrated. Using the proposed optimal design method, a design example is done and the expected simulation result is obtained.

**Index Terms**— charge pump PLL, jitter transfer characteristic, optimal design

## 1. Introduction

In optical communication systems such as SONET or SDH, receivers with good jitter characteristics are essential to achieve good system performance. The ITU-T G.783 recommendation for SDH specifies 3 issues about jitter characteristics of receivers: 1) jitter transfer, 2) jitter generation 3) jitter tolerance. Jitter characteristics of receivers should meet these specifications.

The Clock and Data Recovery (CDR) circuit is the most important part of a receiver, in which usually a Phase Locked Loop (PLL) is integrated [1], [2]. The PLL in a CDR circuit is used to regenerate the clock signal from the received data and then to recover the data. Hence, the design of a PLL in a CDR circuit turns out to be a key consideration for the design of high-speed communication systems. The jitter characteristics of PLLs are quite dependent on the loop parameters. The PLL parameters should be chosen properly so that the jitter characteristics of PLLs meet the specifications of the ITU-T G.783 recommendation [3]. Therefore, to provide CDR circuits with good jitter characteristics, one basic issue to be considered is to optimize the loop parameters of the PLL [4].

The charge pump PLL is one of the most popular PLL structures since 1980s. Charge pump PLLs are widely used in state of the art CDR circuit designs, because this type of PLLs has outstanding performance. However, proper design of charge pump PLLs for good jitter transfer characteristics remains to be a problem in the existing literature, and the jitter transfer characteristics of some existing designs could not meet the specifications. Although loop parameter optimization of PLLs for jitter transfer consideration was discussed in [4], however, the method proposed in [4] cannot be used for charge pump PLLs, since charge pump PLLs exhibit different characteristics from the lag-lead type PLLs discussed in [4]. In this paper, we will propose the optimal loop parameter design method of charge pump PLLs for jitter transfer characteristic optimization. Since

the most commonly used charge pump PLLs are third order PLLs with a second order low-pass filter in the loop, we will discuss this kind of third order charge pump PLLs in this paper. In Section 2, the linear model of charge pump PLLs is described. In Section 3, the jitter transfer characteristic of charge pump PLLs is discussed. The method of optimal loop parameter design of charge pump PLLs is given in Section 4. Section 5 gives the conclusion.

## 2. Linear model of charge pump PLLs

A charge pump PLL in CDR circuits is normally composed of a phase detector (PD), a charge pump (CP), a low pass filter (LPF) and a voltage controlled oscillator (VCO). Figure 1 shows the block diagram of a charge pump PLL. The PLL performs as a low pass filter to the phase of input signal. By focusing on the phase variables, the PLL can be modeled as a linear system. In this model the PD and CP are modeled as gain stages of  $1/2\pi$  and  $I_p$  respectively, and the VCO is modeled as an integrator.

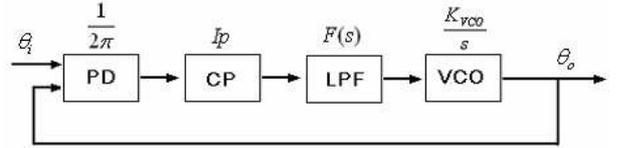


Figure 1. block diagram of charge pump PLL

The most commonly used loop filters for charge pump PLLs are second-order low-pass filters, such as the filters in [1] and [2]. Figure 2 shows the low pass filter used in the PLL loop. The whole PLL loop is a third order loop.

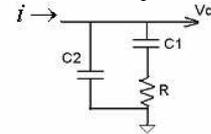


Figure 2. low-pass filter in PLL loop

The open loop phase transfer function and closed loop phase transfer function of the PLL can be written as (1) and (2) respectively,

$$G_o(s) = \frac{I_p K_{VCO}}{2\pi} \frac{(sRC_1 + 1)}{s^3 RC_1 C_2 + s^2 (C_1 + C_2)} = \frac{I_p K_{VCO} R + I_p K_{VCO}}{2\pi} \frac{1}{s^3 mRC_1 + s^2 (m+1)} \quad (1)$$

$$G_c(s) = \frac{I_p K_{VCO} R + I_p K_{VCO}}{2\pi} \frac{1}{s^3 mRC_1 + s^2 (m+1) + s \frac{I_p K_{VCO} R + I_p K_{VCO}}{2\pi}} \quad (2)$$

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where  $I_p$  is the current of charge pump,  $K_{VCO}$  is the VCO gain constant and  $m=C_2/C_1$  is the capacitance ratio. Usually,  $C_2$  is much smaller than  $C_1$  ( $m \ll 1$ ). If we let

$$\omega_n^2 = \frac{I_p K_{VCO}}{2\pi C_1} \quad (3)$$

$$2\xi\omega_n = \frac{I_p R K_{VCO}}{2\pi} \quad (4)$$

then (1) and (2) can be re-written as (5) and (6),

$$G_o(s) = \frac{2\xi\omega_n s + \omega_n^2}{m \frac{2\xi}{\omega_n} s^3 + (m+1)s^2} \quad (5)$$

$$G_c(s) = \frac{2\xi\omega_n s + \omega_n^2}{m \frac{2\xi}{\omega_n} s^3 + (m+1)s^2 + 2\xi\omega_n s + \omega_n^2} \quad (6)$$

Thus, the PLL has three loop parameters,

- 1) natural frequency  $\omega_n$  (sometimes  $f_n = \omega_n/2\pi$  is used for convenience);
- 2) damping ratio  $\xi$ ;
- 3) capacitance ratio  $m$ .

Note that for second order PLLs, natural frequency and damping ratio are well defined and can be used to characterize second order system definitely. Here, these two terms are used only for convenience and do not carry the same information as they do for second order loops.

### 3. Jitter transfer characteristic of charge pump PLL

The jitter transfer characteristic of the PLL is the same as the phase transfer characteristic. So the open loop and closed loop jitter transfer function of the PLL, which relates the input jitter and output jitter, can also be described as (1)~(6). The magnitude-frequency response of the closed loop transfer function  $G_c(s)$  is that of a low-pass filter. The DC gain of  $G_c(s)$  is 0 dB, and the cutoff frequency  $f_c$  (-3dB frequency) is about several times of the natural frequency  $f_n$ . The maximum value of  $|G_c(j\omega)|$  is called jitter peaking.

The ITU-T G.783 recommendation specifies that the jitter peaking of the jitter transfer function should be no more than 0.1dB. The following figure 3 shows the specification.

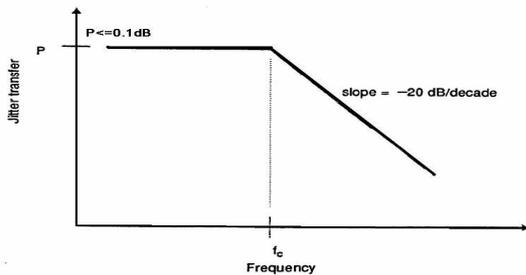


Figure 3. Jitter transfer characteristic specification

The shape of the magnitude-frequency response of  $G_c(s)$  is only dependent on the damping ratio  $\xi$  and the capacitance ratio  $m$ , and is independent of the natural frequency  $\omega_n$  except for a lateral shift. However, the magnitude-frequency response of  $G_c(s)$ , or so called jitter gain, inherently has jitter peaking larger than 0.1dB if  $m$  is not small enough. Figure 4 shows the magnitude-frequency

responses of  $G_c(s)$  when  $m=0.05$  and  $\omega_n=1000\text{rad/sec}$ , and for  $\xi=2$  and 0.707 respectively. The jitter peaking (maximum value of the jitter gain curve) is 1.11dB when  $\xi=2$  and 2.42dB when  $\xi=0.707$ . Both are much higher than the specified 0.1 dB.

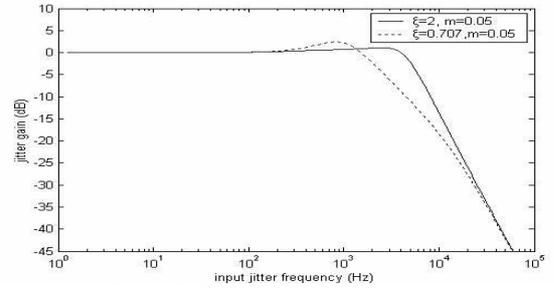


Figure 4. Jitter transfer characteristics

For second order zero-less transfer functions, jitter peaking can be reduced by simply increasing the damping ratio, and it can be eliminated when damping ratio  $>1$ . Because of this, less experienced design engineers tend to increase the damping ratio of a third order PLL loop when they need to reduce jitter peaking. Unfortunately, this straight-forward method rarely works. This is because the peaking and damping ratio relation becomes much more complex in the presence of additional poles or zeros. In fact, increasing damping ratio can cause even worse jitter peaking under some conditions for third-order PLLs. Specially, when damping ratio is quite small, increasing damping ratio will decrease the jitter peaking; however, when damping ratio is larger than a threshold value  $\xi_m$ , increasing damping ratio will increase jitter peaking. Figure 5 shows the relationship between jitter peaking and damping ratio  $\xi$  and capacitance ratio  $m$ . From the figure we can see that for a given capacitance ratio  $m$ , there exists a lower bound for jitter peaking when the damping ratio  $\xi$  varies. For the given capacitance ratio  $m$ , this lower bound is achieved only by using the specific damping ratio  $\xi_m$ .

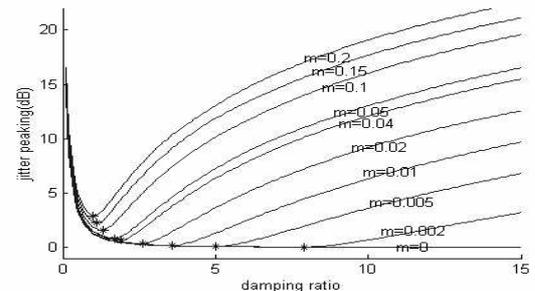


Figure 5. Minimum jitter peaking versus damping ratio and capacitance ratio

From Figure 5, we can see that the minimum jitter peaking (the lower bound of each curve) can be viewed as a function only with respect to  $m$ . Figure 6(a) depicts the function  $JP(m)$  that gives the relation between the minimum jitter peaking and capacitance ratio  $m$ . Although it's not easy work to get the function using accurate mathematic description, we can use a table that illustrates this relationship for practical design. Such a table is included in Table 1 (a). It's necessary to find the condition under which the minimum jitter peaking is achieved. As presented previously, for a given  $m$ , the minimum jitter peaking is achieved only by using a specific damping ratio value  $\xi_m$ . This specific

damping ratio  $\xi_m$  should also be a function of  $m$ :  $\xi_m(m)$ . Figure 6(b) shows the function  $\xi_m(m)$ . From the figure we can see that it's also a continuous function, and we can also have a table for practical design (included in Table 1 (b)). In practical design, instead of merely increasing the damping ratio to get small jitter peaking, we should choose the capacitance ratio  $m$  and the damping ratio  $\xi$  properly to achieve the jitter transfer characteristic that meets the specifications.

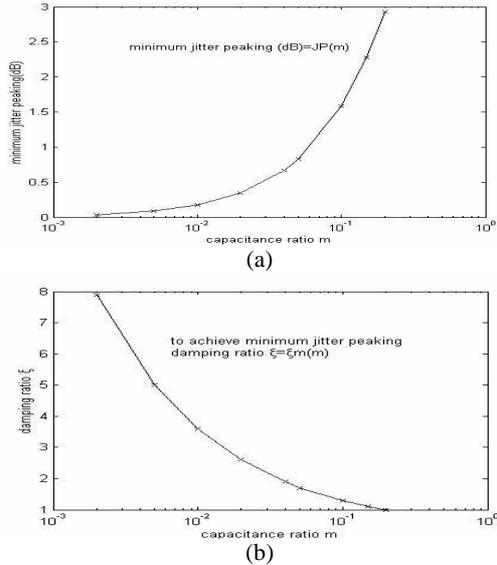


Figure 6. (a)  $JP(m)$ ; (b)  $\xi_m(m)$

### Sampling effect of phase detector

The phase detector is modeled as only a gain of  $1/2\pi$  in Section 2. Actually, most phase detectors used in charge pump PLLs work in the digital mode. The phase detectors inherently have sampling effect, i.e., the input of the phase detector is sampled at a rate at which the phase detector is operated. Design engineers don't expect such sampling effect and ignore this effect in practical design since considering sampling effect will make the design much more complicated. However, the sampling effect will affect the characteristics of PLLs significantly if the operation rate of the phase detectors is not much higher than the loop cut-off frequency. It is necessary to take account in such an effect in PLL design.

Although inherently nonlinear, the phase detector can be approximately modified as a linear transfer function of the form:

$$H_{PD}(s) = \frac{1 - e^{-sT_p}}{sT_p} \cdot \frac{1}{2\pi} \quad (7)$$

where  $1/T_p$  is the operation rate of the phase detector. The sampling effect will cause the jitter peaking of the PLL jitter transfer characteristic to become worse. This effect becomes worse significantly when the operation rate  $1/T_p$  becomes not much higher than the loop bandwidth. When including the sampling effect in the linear model, simulation results show that when the phase detector operation rate is lower than hundreds of times of the natural frequency, the relationship between jitter peaking and damping ratio has different shape from that without the sampling effect. Figure 7 illustrates the difference. Taking the

case that  $1/T_p = 100 * f_n$  as an example, the curve can be divided into 3 segments:

- i) when the damping ratio is very small, jitter peaking decreases when damping ratio increases;
- ii) when the damping ratio becomes larger than  $\xi_m$ , the jitter peaking increases with damping ratio;
- iii) when the damping ratio is larger than  $\xi_{m2}$ , the jitter peaking decreases when the damping ratio is increased further;

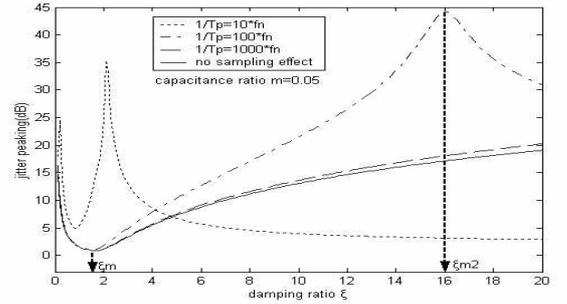
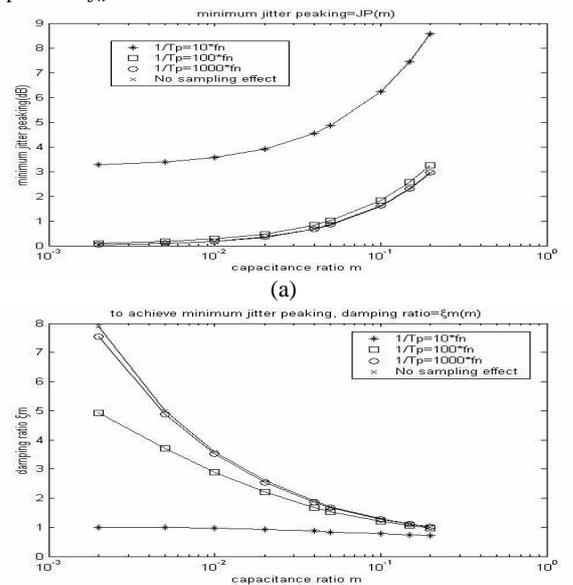


Figure 7. jitter peaking versus damping ratio with sampling effect

Although in the third segment, increasing the damping ratio can reduce the jitter peaking, we cannot make use of the third segment in practical design, since that makes damping ratio too high, which will lead to a very sluggish PLL. If we only consider the condition that the damping ratio is not much high, then we can similarly have the two functions  $JP(m)$  and  $\xi_m(m)$  for the case taking account in sampling effect. Figure 8 (a) and (b) show the modified  $JP(m)$  and  $\xi_m(m)$  with different sampling effect respectively. In each figure, 4 curves are shown corresponding to 4 cases respectively: 1)  $1/T_p = 10 * f_n$ ; 2)  $1/T_p = 100 * f_n$ ; 3)  $1/T_p = 1000 * f_n$  and 4) no sampling effect (for comparison). From the figure, we can see that the sampling effect plays an important role for the jitter transfer characteristic when  $1/T_p$  is not high compared to  $f_n$ .



(b) Figure 8. (a) modified  $JP(m)$ , (b) modified  $\xi_m(m)$  with sampling effect

From simulation, we can obtain the following tables of  $JP(m)$  and  $\xi_m(m)$  for practical PLL design.

**Table 1.** (a) Minimal jitter peaking (dB), (b) optimal damping ratio to achieve minimal jitter peaking under different cases for different capacitance ratio  $m$

(a)									
m	0.002	0.005	0.01	0.02	0.04	0.05	0.1	0.15	0.2
Case1	0.035	0.087	0.17	0.34	0.67	0.83	1.6	2.3	2.9
Case2	0.039	0.092	0.18	0.35	0.69	0.85	1.6	2.3	3.0
Case3	0.091	0.16	0.27	0.47	0.84	1.0	1.8	2.6	3.3
Case4	3.3	3.4	3.6	3.9	4.5	4.8	6.2	7.4	8.6

(b)									
m	0.002	0.005	0.01	0.02	0.04	0.05	0.1	0.15	0.2
Case1	7.9	5.0	3.6	2.6	1.9	1.7	1.3	1.1	1.0
Case2	7.5	4.9	3.5	2.5	1.9	1.7	1.3	1.1	1.0
Case3	4.9	3.7	2.9	2.2	1.7	1.5	1.2	1.1	1.0
Case4	1.00	0.99	0.96	0.92	0.87	0.84	0.78	0.73	0.72

(Case 1: no sampling effect; Case 2:  $1/T_p=1000*f_n$ ; Case 3:  $1/T_p=100*f_n$ ; Case 4:  $1/T_p=10*f_n$ )

## 4. Optimal loop parameter design

### for jitter transfer characteristic optimization

From the previous discussion, to minimize the jitter peaking of PLLs' jitter transfer characteristic, the loop parameters  $m$  and  $\xi_m$  should be chosen properly. We can define the following procedure of optimal loop parameter design of charge pump PLLs for jitter transfer characteristic optimization:

- 1) Decide the range for the ratio of phase detector operation rate over natural frequency (note that in most specifications only the cut-off frequency is defined and we can use the cut-off frequency here as approximation), decide the maximum tolerated jitter peaking and find capacitance ratio  $m$  using Table 1(a).
- 2) Use Table 1(b) to find the optimal damping ratio value  $\xi_m$  to achieve minimum jitter peaking;
- 3) Decide the accurate natural frequency  $\omega_n$  according to the application (try different  $\omega_n$  in the transfer function and find  $\omega_n$  that gives the cut-off frequency nearest to the specified value), choose reasonable value of VCO gain constant  $K_{VCO}$ , and then use (3) and (4) to calculate  $I_p$ ,  $R$ , and  $C_j$ .  $C_2=m*C_j$ ;
- 4) Use time domain simulation with non-linear model to verify that the expected jitter transfer performance can be achieved by using the parameters selected. Charge pump PLL is actually a non-linear system, so it is not accurate to use linear model to predict the system performance, and it is necessary to use a non-linear model to verify the design result.

The following is a design example. The target is to design a PLL for OC-48 receiver, and the PLL should work at 2.5 GHz. According to the specification, the cut-off frequency  $f_c$  should be 2 MHz. So the natural frequency of the PLL should also be around 2 MHz. Assume a full-rate phase detector is used.  $1/T_p=2.5GHz$ ,  $1/T_p$  is about 1250 times of the natural frequency, so we can refer to case 2 in table 1. To meet the jitter specification of the ITU-T G.783 recommendation, the maximum

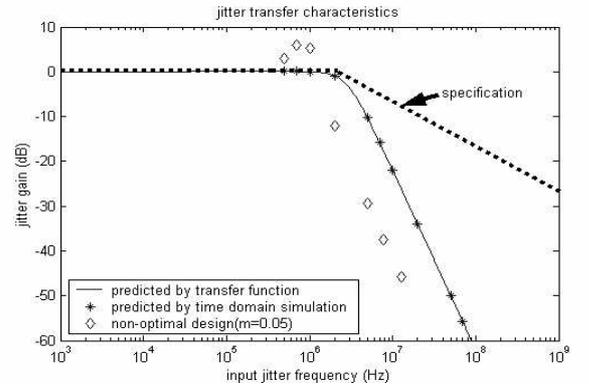
tolerated jitter peaking should be lower than 0.1 dB. From Table 1, we can choose  $m=0.005$  and  $\xi=5.0$ . The final parameters are:

$$m=0.005, \xi=5.0, f_n=200kHz, f_c=2000kHz$$

$$I_p=50\mu A, K_{VCO}=2\pi \times 5 \times 10^8 \text{ rad/sec/V}$$

$$R=503\Omega, C_j=15.83nF, C_2=79.16pF$$

Results from time domain simulation with non-linear model show that the maximum jitter peaking is only 0.078dB with these selected parameters. Figure 9 shows the simulated jitter transfer curves. The jitter transfer curves predicted both by transfer function and by time domain simulation with non-linear model match well, and meet the requirement of the specification. For comparison, the jitter transfer curve of a non-optimal design ( $m=0.05$  and all other parameters remain the same) is also shown in this figure, in which case the jitter peaking is up to 5.9dB.



**Figure 9.** Jitter transfer characteristic of the designed PLL

## 5. Conclusion

Jitter transfer characteristics for third order charge pump PLLs' are discussed in this work. Simulation results shows that to achieve jitter transfer characteristic with minimized jitter peaking, loop parameters of PLLs such as the natural frequency  $\omega_n$  and the capacitance ratio  $m$  should be chosen properly. Two functions  $JP(m)$  and  $\xi_m(m)$  are defined to illustrate the minimum jitter peaking for the given  $m$  and the damping ratio  $\xi_m$  that should be used to achieve such minimum jitter peaking. Also it is shown that the sampling effect should be considered when the operation rate of the phase detector is not much higher compared to  $\omega_n$ . An optimal loop parameter design method is given. The simulation results of a design example show that this method is effective.

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