*A HISTOGRAM BASED AM-BIST ALGORITHM FOR ADC CHARACTERIZATION USING IMPRECISE STIMULUS

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ABSTRACT

A new method enabling the use of stationary non-linear signals has been proposed for testing the linearity of high resolution ADCs. With this method, linearity requirement of the source can be dramatically relaxed and faster sources can be utilized to reduce the test time and increase test coverage for the ADC. Preliminary simulation results show that with a 5-bit linear input signal, the trip points of a 11-bit Flash ADC can be identified to better than 0.5LSB and by incorporating a built-in calibration circuit, the trip point error can be decreased from an uncalibrated 15 LSB level (7-bit performance) to less than 0.5 LSB (11-bit performance) or better.

1. INTRODUCTION

The rapid growth in the application of increasingly complex mixed-signal circuits in the communication and signal processing arenas coupled with industry-wide improvements in semiconductor processing has created a large market for low-cost mixed signal integrated circuits. Paralleling this downward cost pressure are increased demands on the number, accuracy and complexity of testing steps in the production test environment. As a result, production-testing costs are becoming a rapidly growing and increasingly significant portion of the overall manufacturing costs [1].

ADC testing has also become very challenging and costly. For high resolution ADCs (16bits and above), test cost for the ADC is determined by the number of codes in the ADC, and not by the ADC sampling rate. This non-intuitive result can be explained by the following observation. As the number of codes increase, the linearity requirements of the source driving the ADC (linearly) increases. This performance requirement enforces slow, high-precision signal generator architectures that require long settling times. This results in increased testing time and testing costs, which is totally prohibitive for manufacturing.

This has caused the emergence of mixed-signal integrated Built-In-Self-Test (BIST) strategies as attractive solutions. Apart from reduction or elimination of costs associated with using production testers, BIST solutions are attractive from alternate viewpoints. One advantage is the ability to test deeply embedded analog functionality in SoC that cannot be practically presented to an external tester. The second potential advantage is associated with the ability to extend some BIST approaches to provide self-calibration as a part of the design process. By jointly considering the issues of Analog and Mixed-Signal BIST (AM-BIST) and built-in calibration, value can be added with an AM-BIST capability by salvaging devices that would be scrapped due to soft-faults with a commercial production tester. However the main bottleneck with the existing BIST solutions is associated with the generation of highly linear stimuli on-chip. A new approach to BIST for analog and mixed-signal circuits is presented in this paper. Unlike the traditional approaches that require precise input stimuli [2][3][4], the new approach is based upon using easily generated but inherently imprecise stimuli to generate a circuit response that can be used to validate the performance of the Device-Under-Test (DUT) through post-processing of output data with standard Digital Signal Processing (DSP) algorithms and hardware.

2. A HISTOGRAM-BASED IDENTIFICATION STRATEGY

In this section, a new histogram-based algorithm suitable for characterizing a Flash ADC is discussed. Two highly nonlinear signals are used as inputs and the outputs obtained from the ADC are then analyzed to characterize the device. Initial approaches to solving this problem are discussed in [5, 6]. However the method proposed in [6] is sensitive to the relationship between the two input signals. Also the various approximations that were made limited the overall accuracy of the final result. In this paper a more elegant and modified solution has been proposed that results in better characterization. Also the exact relationship between the two inputs need not be known a priori and is estimated as part of the algorithm.

Figure.1. gives a plot of the transfer-characteristics of the input excitation signals. Overlaid on top are the ideal and non-ideal trip points of the flash converter. The various symbols that are used in the figure are described below:

I_i : i^{th} transition level (trip point) of Ideal ADC

T_i : i^{th} transition level of actual (non-ideal) ADC

Ψ_i : Deviation of Ti from Ii

F1 : 'ramp-like' input signal

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F2 : F1 shifted by α

$C_i^{'}$: Number of samples in i^{th} bin for actual ADC with F1 as input signal (i.e. Histogram of F1)

$C_i^{''}$: Number of samples in i^{th} bin for actual ADC with F2 as input signal (i.e. Histogram of F2)

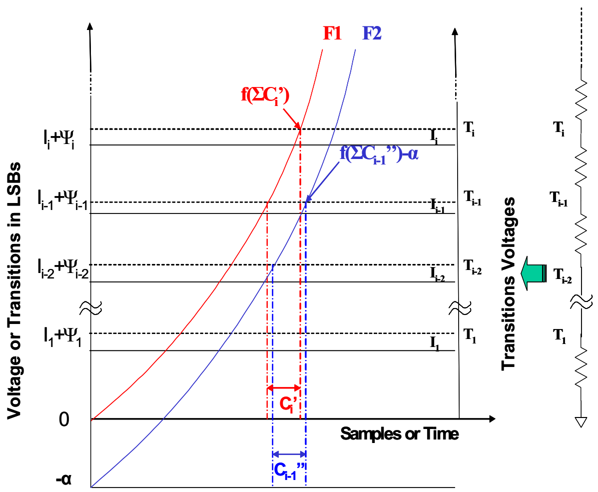

Figure.1 Transfer Characteristics of the Input Excitation Signal

It is assumed that F2 is shifted with respect to F1 by a fixed but unknown amount α. The trip points of the non-ideal ADC can be written in terms of the trip points of the Ideal ADC by the following equations:

$$T_i = I_i + \Psi_i , i = 1,2,...,2^N \tag{1}$$

where N refers to the resolution of the ADC.

Our goal in identifying the system is to determine the actual deviations of the ADC under test from that of an ideal ADC. In terms of the notations used, the goal is to determine the sequence $<\Psi_1, \Psi_2, \ldots, \Psi_{2^N}>$.

Let the input signal F1 be defined by some function 'f'. The exact nature of the function is not important as long as it is continuously differentiable and its first derivative is locally constant. This requirement is not difficult to achieve, because the function is only defined at finite points and we can always find a polynomial that satisfies this property. If the input signal is sampled uniformly in time, then the function 'f' maps the histogram values to the ADC transition points by the following equation:

$$f(\sum_{j=1}^{i} C_j^{'}) = T_i = I_i + \Psi_i , i = 1,2,...,2^N \tag{2}$$

Also since the second signal, F2, is obtained by shifting the first signal, F1, by a constant value (α), we get:

$$f(\sum_{j=1}^{i} C_j^{''}) = I_i + \Psi_i + \alpha, i = 1,2,...,2^N \tag{3}$$

If the function 'f' is linear, it is trivial to obtain the values of Ψ_i from either equation (2) or (3). However, due to the nonlinear nature of the input signal, this task is complicated and some linearization method needs to be used to make the solution practical. Subtracting the $(i-1)^{th}$ equation in (3) from the i^{th} equation in (2), we get:

$$f(\sum_{j=1}^{i} C_j^{'}) - f(\sum_{j=1}^{i-1} C_j^{''}) = 1 + \Psi_i - \Psi_{i-1} - \alpha \tag{4}$$

for $i=2,3,\ldots\ldots 2^N$, where $I_i - I_{i-1} = 1$ LSB. In the above equation, all the terms are expressed in LSBs. Using the mean value theorem, the left hand side part of the equation can be rewritten as

$$f(\sum_{j=1}^{i} C_j^{'}) - f(\sum_{j=1}^{i-1} C_j^{''}) = f'(\xi_i)(\sum_{j=1}^{i} C_j^{'} - \sum_{j=1}^{i-1} C_j^{''})$$
$$\xi_i \in [\min\{\sum_{j=1}^{i} C_j^{'}, \sum_{j=1}^{i-1} C_j^{''}\}, \max\{\sum_{j=1}^{i} C_j^{'}, \sum_{j=1}^{i-1} C_j^{''}\}] \tag{5}$$

where, $f'(\xi_i)$ is the derivative of the input signal evaluated at ξ_i. We approximate $f'(\xi_i)$ by the following equation:

$$f'(\xi_i) = \frac{1}{2}\left(\frac{1+\Psi_i - \Psi_{i-1}}{C_i^{'}} + \frac{1+\Psi_i - \Psi_{i-1}}{C_i^{''}}\right) \tag{6}$$

This is a simple average of the two slopes of $f(x_{in})$ at $x_{in} \approx I_i + \Psi_i$ and $x_{in} \approx I_i + \Psi_i + \alpha$ respectively, but this approximation is good enough for most of the normal non-linear input signals. Using the above linearization method we can simplify equation (4) as follows:

$$1 = \frac{1}{1-\gamma_i}\alpha + \Psi_{i-1} - \Psi_i , i = 2,3,...,2^N \tag{7}$$

$$\text{where, } \gamma_i = \frac{1}{2}\left(\frac{1}{C_i^{'}} + \frac{1}{C_i^{''}}\right)\left(\sum_{j=1}^{i} C_j^{'} - \sum_{j=1}^{i-1} C_j^{''}\right) \tag{8}$$

All the γ_i's can be computed from the two sets of histogram values. It can be safely assumed that Ψ_{2^N} is 0, since the top node of the flash ADC is tied to the supply and hence is fixed. The total numbers of variables that then need to be identified are 2^N, which comprises the sequence $< \Psi_1, \Psi_2, \ldots, \Psi_{2^N-1}, \alpha >$. Thus, in addition to (7), we still need one more equation to uniquely solve for all of the 2^N variables. It can be seen that the case of i=1 in (2) has not been used in the set of equations derived in (4). This equation in conjunction with the case when i=3 in (3) results in the following condition:

$$f(C_2^{''}) - f(C_1^{'}) = 1 + \Psi_2 - \Psi_1 + \alpha \tag{9}$$

(9) can also be reduced to a linear equation using the same linearization method as explained earlier. These sets of 2^N equations can then be simultaneously solved for all of the unknowns. Simulation results using the above method to characterize the ADC were found to be very good. The transitions of the ADC were identified to a much higher accuracy than the resolution of the device-under-test. Section 3 gives more detail on the simulation setup and the results obtained.

The solution of the set of linear equations described above, however, requires a 'matrix inversion' step that increases the computational complexity for ADC resolution in excess of 9~10 bits. On closer look into (7), it can be seen that if the value of α can be identified independently, then a much simpler set of equations given in (10) is obtained.

$$\Psi_i = 2^N - i - \sum_{j=i}^{2^N-1} \frac{1}{1-\gamma_{i+1}} \alpha, i = 1,2,\ldots,2^N - 1 \qquad (10)$$

The computational complexity of equation (10) is proportional to the number of equations (2^N), as compared to the complexity for matrix inversion method that is of the order of 2^{3N}. The latter solution is more attractive from complexity viewpoint, provided α can be determined by some alternate method with sufficient accuracy. One proposed method is to use all C_i' and C_i'' to estimate α, and then replace its value into equation (10). The equation used to determine α is given by:

$$\alpha = \left(\frac{\sum_{i=1}^{2^N-1} C'_{i+1}}{\sum_{i=1}^{2^N-1} \frac{1}{1-\gamma_i}} \right) \left(\frac{N}{\sum_{i=1}^{2^N} C'_i} \right) \qquad (11)$$

Results using this 'non-matrix inversion' method are also presented in Section 3 and are compared with that obtained using 'matrix-inversion' approach.

3. MODELING OF THE TEST SETUP AND SIMULATION RESULTS

To validate the algorithm, the system involving the input signal generator and the A/D converter was modeled in MATLAB. For convenience in this work we limited the non-idealities of the converter to the resistor variations but the concept can be extended to include the comparator offsets as well. To each of the resistors in the ADC (with nominal value of R_o), an uncorrelated error value based on a uniform distribution between +/-50% R_o was added. The two signals that were used as input are:

$$x_1(t) = t + a(t - t^2) \text{ and}$$

$$x_2(t) = t + a(t - t^2) - \alpha \qquad (12)$$

The magnitude of the coefficient 'a' determines the accuracy of the input signal. Simulation results with the earlier version of the histogram algorithm and with small amounts of shifts are given in [5,6]. The newly proposed approach described in this paper was then used to characterize the data converter. An 11bit flash converter was considered. An input signal of 5 bit linearity was given to the DUT. The second signal was obtained by shifting the first signal by 300LSBs. This value of shift is just used to generate the input signal and is not used in the algorithm. The amount of shift (i.e. α) is calculated independently in the algorithm as described in section 2. The shift estimated by the histogram algorithm for this sample run was 300.0259LSB, which is very close to the actual value. Figure.2. shows the plot of the trip point errors introduced (Ψ_i's), and that estimated and the error in prediction.

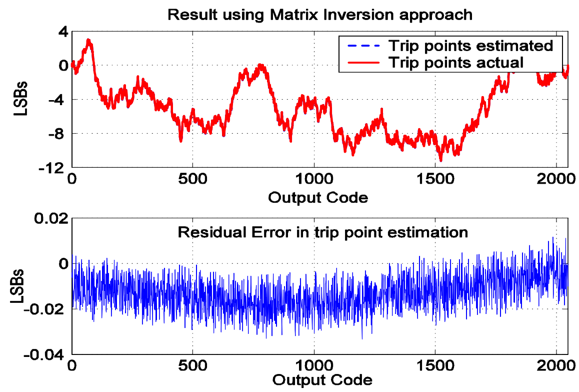

Figure.2. Introduced and Estimated trip point errors

From the figure it can be observed that the trip point error of the device ranges from -12~3 LSBs approximately and the estimated value closely matches the actual value. What is more important is the fact that the residual error is less than 0.02LSB, which means that with the information that is obtained from the algorithm, after calibration the trip points can be adjusted to approximately 14 bit accuracy. As compared to the results provided in [6] where the residual error is nearly 0.2LSB, the method proposed here gives significant improvement in performance. This is primarily due to the precise estimation of the relationship between the two signals within the algorithm. Figure.3. shows the plot of the DNL introduced and DNL estimated. The error in DNL estimation is also plotted. The magnitude of the error in DNL prediction is less than 0.02LSBs. This is actually limited by the number of samples taken in each bin.

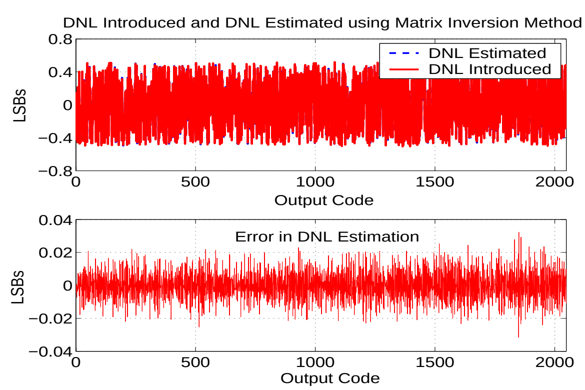

Figure.3. Plot of DNL introduced and DNL estimated

Next a set of 50 runs of 11 bit ADCs was performed. A different random resistor combination was used each time to model different trip point error patterns. Figure.4. gives the plot of maximum trip point error introduced in each run and the residual error in prediction.

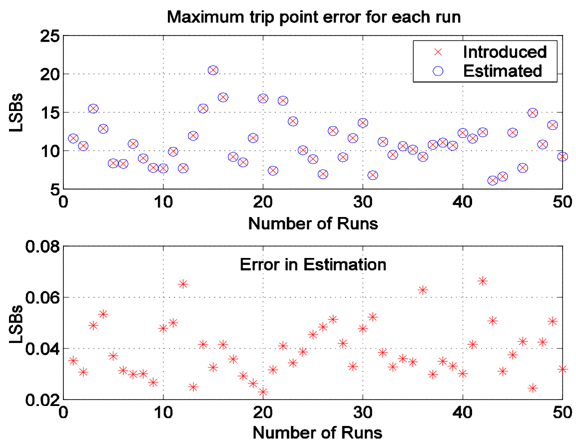

Figure.4. Result of 50 runs – Matrix Inversion Method

It can be seen that using the predicted value, after correction the trip points of the converter can be identified to approximately 0.02LSB~0.07LSB (i.e. 14 bits accuracy).

The Non-matrix inversion method was then tried on the same converter. Again a set of 50 runs of 11 bit ADCs was performed. Figure.5. gives the plot of maximum trip point error introduced in each run and the residual error in prediction.

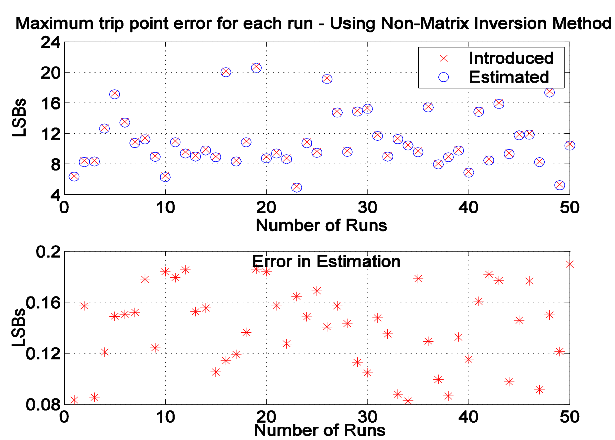

Figure.5. Result using Non-matrix Inversion method

It can be seen that the residual error is now approximately 0.08LSB~0.12LSB, which implies that we can still identify the trip points to nearly 13 bit level, only 1 bit less accurate than that obtained by using matrix inversion method. The number of floating point operations (in MATLAB) reduces from 5.1e10 for Matrix Inversion method to 3.6e4 for Non-Matrix Inversion method, corresponding to a significant reduction in complexity. This makes it viable for this scheme to be implemented as a BIST solution.

The simplified 11-bit Flash ADC example is for illustration purposes only. In reality, Flash ADC performance is dominated by dramatic comparator offset mismatches and AC kick-back effects. Also, 11-bit flash architectures are also very expensive and uncommon due to the high number of comparators required. Moreover, testing of an 11-bit ADC is considered to be known art and can be done well within 2 second of test time and does not constitute a problem (mostly because 12bit linear sources are widely available and are significantly fast).

4. CONCLUSION

Two histogram based approaches for characterizing a flash A/D has been proposed. Results indicate that for smaller resolution, the matrix inversion method can be used to get very high accuracy identification (being limited by the number of sampler per bin); while for higher resolution the non-matrix inversion method can be easily implemented resulting in modest improvement in performance after calibration. Simulation results show that a Flash ADC can be characterized/tested to the 13-bit level from initial 7-bit accuracy or worse while using a stimulus that is only 5-bit accurate.

5. REFERENCES

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