An Alternative Method for Characterizing Capacitor Matching

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Abstract **– An alternative method for characterizing capacitor matching is presented. The basic idea of this method is to sense the mismatch among the capacitors by amplifying the error voltage using an iterative switched-capacitor scheme. Through simulation, this method has shown attractive property for sensing capacitor mismatches down to 1% and smaller.**

INTRODUCTION

Switched-capacitor is one of the most popular approaches in data converters design. However, high-resolution data converters require accurate capacitor matching. In order to improve circuit performance, both digital and analog calibration techniques were proposed and discussed in the literature [1-5]. Among the many calibration methods, the under-range/ over-range method had been greatly discussed in the literature [1,5]. This method utilizes a capacitor array to correct mismatches by monitoring the under-range or over-range occurrence of the signal. However, it is difficult to detect under-range or over-range of the signal if the mismatch is considerably small. Therefore, it is the interest of this paper to discuss a method of picking up small signal that corresponds to small mismatch. By doing so, it is possible to achieve highly accurate capacitor matching. Figure 1 depicts a gain-of-two circuit that is widely used in pipelined and cyclic A/D converters. Note that the circuit only requires a ratio of one capacitor matching.

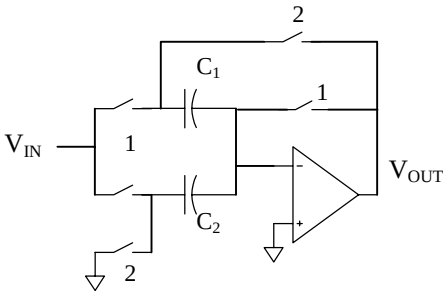

Figure 1: Gain-of-two circuit

The output, V_{OUT}, of the circuit is given by the following expression:

$$V_{OUT} = V_{IN}(1+\frac{C_2}{C_1}) \qquad (1)$$

If $C_2=(1+\varepsilon)C_1$ where ε is 0 nominally, then (1) can be rewritten as

$$V_{OUT} = V_{IN}(2+\varepsilon) \qquad (2)$$

From (2), one can see that the error due to capacitor mismatch has an expression of εV_{IN}. If ε is small, the calibrating circuit required to pick up the small mismatch error needs to be highly sensitive. To ease the requirement on the calibrating circuit, this paper is proposing a simple switched-capacitor scheme that is able to pick up small mismatch error.

BASIC IDEA

The same switched-capacitor circuit in Figure 1 is reconfigured as depicted in Figure 2(a). This is the reset phase of the calibration, during which C_1 is charged to V_{IN} while C_2 is discharged. In the next phase (phase 1) as in Figure 2(b), C_1 is hold and C_2 is charged to V_{IN}. If C_1 and C_2 are perfectly matched and everything else is ideal, then the charge transfer from C_2 should completely cancel the charge held in C_1. This will result in a zero voltage change at V_{OUT}. Nevertheless, if there is a capacitor mismatch of θ between C_1 and C_2 ($C_2=\theta C_1$ where θ is 1 nominally), a non-zero voltage change, ΔV_{OUT}, given by the following expression will result at V_{OUT}.

$$\Delta V_{OUT} = (1-\theta)V_{IN} \qquad (3)$$

The error voltage or ΔV_{OUT} obtained at the output of A_1 is sampled by C_3 and the voltage is then held by A_2 in the next phase (phase 2) to charge up C_2, as depicted in Figure 2(c). With the error voltage $(1-\theta)V_{IN}$ stored in C_2, the switched-capacitor will go through phase 1 again as in Figure 2(b), and followed by phase 2 as in Figure 2(c) for *k*-cycle. At the end of the k^{th} cycle, the error voltage ΔV_{OUT} has the following expression:

$$\Delta V_{OUT}\,|_{k-th} = (1-\theta^k)V_{IN} \qquad (4)$$

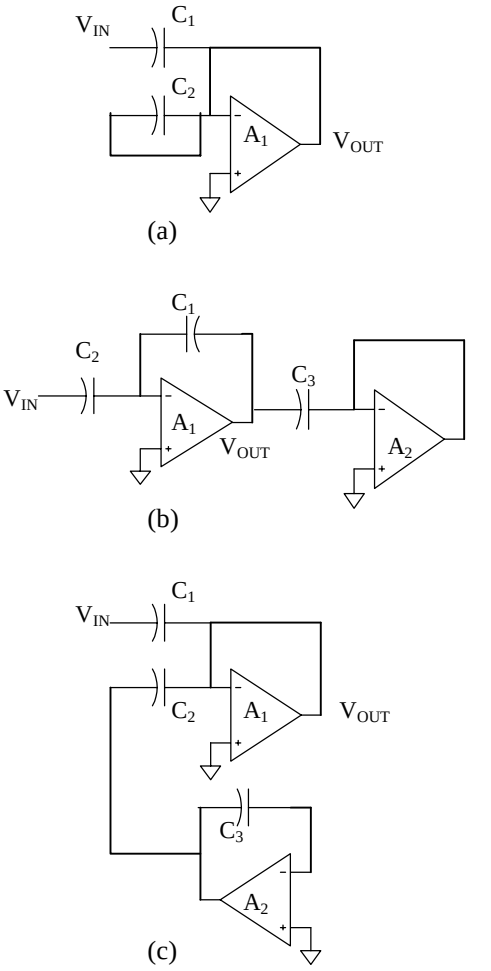

Figure 2 (a) Reset phase. C_1 is charged to V_{IN}; C_2 is discharged. (b) Phase 1. Any mismatch between C_1 and C_2 will result in an error voltage ΔV_{OUT}; C_3 is charged to ΔV_{OUT}. (c) Phase 2. This phase is similar to the reset phase except C_2 is charged to ΔV_{OUT} instead of being discharged.

In Table 1, one can see that ΔV_{OUT} due to a mismatch of ±0.5% (θ=0.995 or 1.005) is amplified by approximately 10 at the 10^{th} iteration (k=10). The error voltage ΔV_{OUT} due to 0.5% mismatch is 5mV in contrast to 50mV at the end of the 10^{th} cycle; hence it is almost trivial to build the comparator needed to pick up the much bigger error signal despite of the small mismatch.

k \ θ	0.995	0.99	1.005	1.01
1	0.0050	0.0100	-0.0050	-0.0100
2	0.0100	0.0199	-0.0100	-0.0201
3	0.0149	0.0297	-0.0151	-0.0303
4	0.0199	0.0394	-0.0202	-0.0406
5	0.0248	0.0490	-0.0253	-0.0510
6	0.0296	0.0585	-0.0304	-0.0615
7	0.0345	0.0679	-0.0355	-0.0721
8	0.0393	0.0773	-0.0407	-0.0829
9	0.0441	0.0865	-0.0459	-0.0937
10	0.0489	0.0956	-0.0511	-0.1046

Table 1: Calculated ΔV_{OUT} due to ±0.5% and ±1% mismatches for 10 cycles.

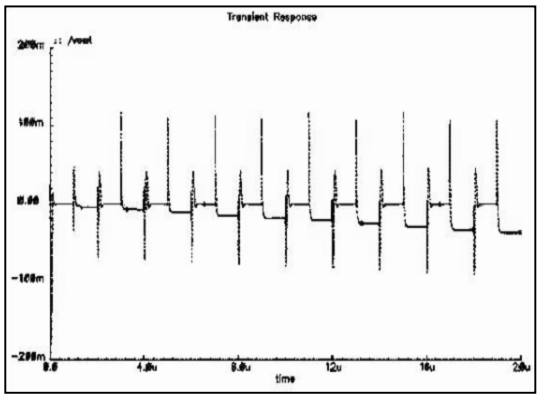

Figure 3: V_{OUT} transient waveform for +0.5% mismatch.

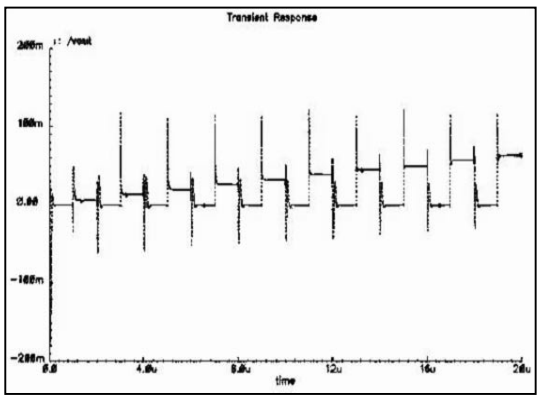

Figure 4: V_{OUT} transient waveform for -0.5% mismatch.

SIMULATION RESULT

Transistors level simulation using HPSICE was performed to verify the discussion. The circuit implementation is depicted in Figure 5. Minimum sized transmission gates were used to realize the switches while the op-amp has a DC gain of 82 dB and GB of 10MHz. Figure 3 and 4 depict the V_{OUT} transient waveforms for 10 cycles with θ=0.995 and 1.005. Note that ΔV_{OUT} is amplified in every clock cycle. The simulated data for ΔV_{OUT} can be found in Table 2. It can be seen that the simulated result is in close agreement with the calculated result. The error introduced by the op-amp and the switches sets an upper limit on the attainable accuracy of this calibration scheme.

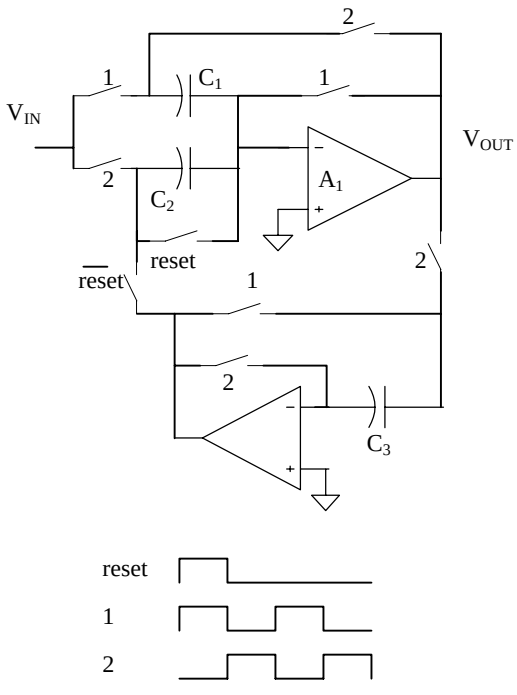

Figure 5: Circuit implementation and timing diagram.

k \ θ	0.995	0.99	1.005	1.01
1	0.0061	0.0112	-0.0040	-0.0088
2	0.0127	0.0225	-0.0070	-0.0162
3	0.0193	0.0341	-0.0099	-0.0243
4	0.0258	0.0452	-0.0135	-0.0340
5	0.0330	0.0559	-0.0164	-0.0416
6	0.0397	0.0673	-0.0191	-0.0506
7	0.0461	0.0783	-0.0221	-0.0591
8	0.0532	0.0895	-0.0263	-0.0678
9	0.0593	0.1007	-0.0300	-0.0773
10	0.0662	0.1114	-0.0330	-0.0857

Table 1: Simulated ΔV_{OUT} due to ±0.5% and ±1% mismatches for 10 cycles.

CONCLUSION

A switched-capacitor scheme that can be used to characterize capacitor matching has been discussed. The major feature of this scheme is its ability to amplify the small error signal due to small capacitor mismatch. This scheme can be adopted in on-chip calibration and built-in self-test systems [6-8] while relieving the performance requirement of other circuits in the system.

REFERENCES

[1] H. Ohara, H. X. Ngo, M. J. Armstrong, C. F. Rahim, and P. R. Gray, " A CMOS programmable self-calibrating 13-bit eight-channel data acquisition peripheral," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 930-938, Dec. 1987.

[2] H. T. Yung, K. S. Chao," An error-compensation A/D conversion technique," IEEE Trans. Circuits Syst, vol. 38, No. 2, pp. 187-195, Feb. 1991.

[3] A. M. A. Ali, K. Nagaraj," Correction of operational amplifier gain error in pipelined A/D converters," *ISCAS 2001 IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 568 –571, 2001.

[4] T. L. Sculley, M. A. Brooke," Nonlinearity correction techniques for high speed, high resolution A/D conversion," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Processing*, vol. 42-3, pp. 154 –163, Mar. 1995.

[5] K. Nagaraj," Efficient circuit configurations for algorithmic analog to digital converters," *IEEE Trans. Circuits Syst. II: Analog and Digital Signal Processing*, vol. 40-12, pp. 777 –785, Dec. 1993.

[6] E. J. Peralias, G. Huertas, A. Rueda, J. L. Huertas," Self-testable pipelined ADC with low hardware overhead," *19th. VTS 2001 IEEE Proc. VLSI Test Symp.*, pp. 272 –277, 2001.

[7] E. K. F. Lee," Reconfigurable data converter as a building block for mixed-signal test," *1997 Proc. European Design and Test Conference*, pp. 359 –363, 1997.

[8] E. Teraoka, T. Kengaku, I. Yasui, K. Ishikawa, T. Matsuo, H. Wakada, N. Sakashita, Y. Shimazu, T. Tokuda," A built-in self-test for ADC and DAC in a single-chip speech CODEC," *1993 Int. Proc. Test Conference*, pp. 791 –796, 1993.