

# Enhancing Performance in Interpolating Resistor String DACs

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## ABSTRACT

Several techniques for enhancing the performance of interpolating resistor string digital-to-analog converters (DAC) are discussed. These techniques will enhance both static and dynamic performance. The resulting circuit structures compensate for the inaccuracies inherent in the coupling of the interpolator to the coarse resistor string by isolating or eliminating the voltage drop across the coarse tap selection switch.

## 1. INTRODUCTION

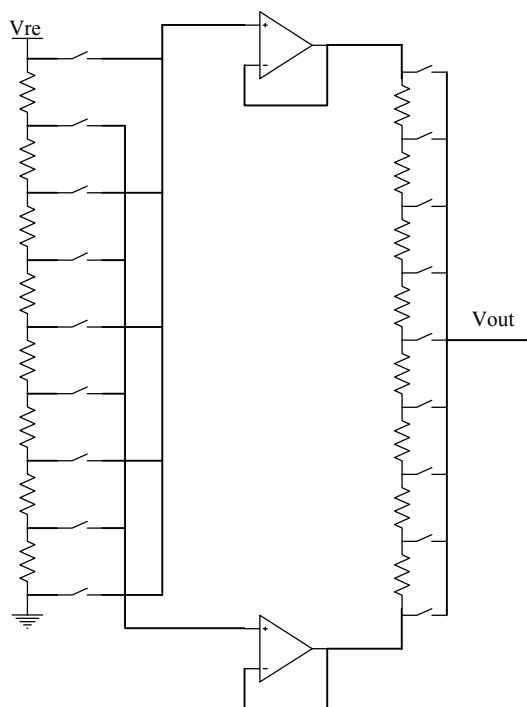


Figure 1: Dual Resistor String DAC

One of the most basic DAC architectures is the resistor string DAC. This structure has many advantages in mid-resolution, moderate to high-speed data converter applications including its inherent monotonicity, high speed, and versatility. This architecture can be improved through the use of an additional interpolating resistor string. The basic implementation of this architecture is illustrated in figure 1 [1]. Here an additional 3 bits of accuracy is achieved by linearly interpolating the voltage

between sub-taps on the main coarse resistor string. An important issue in this architecture is the isolation of the interpolating resistor string from the coarse resistor string. In figure 1, this is accomplished through the use of buffers at the top and bottom of the interpolator.

In addition to the advantage of also being monotonic, this architecture has a reduced matching requirement on the interpolating resistor string, allowing for a more area efficient layout. However, due to the bandwidth limitation of the buffer, the speed is a major disadvantage in this scheme for isolating the interpolating resistor string from the coarse resistor string. Another potential issue is the level dependent offset of the buffer. This is due to the changing DC operating point of the buffer as it moves up or down the coarse resistor string. A wide common mode range is another requirement of the buffer in this architecture. These issues could potentially sacrifice the monotonicity of the structure.

Two distinct problems emerge when the buffer amplifier is removed from the circuit. First, the load of the interpolator affects the integral non-linearity of the converter. The other is the effect of the ohmic resistance of the switch on the differential non-linearity at the extreme tap points of the interpolator. This paper will discuss potential solutions to these problems that have appeared in the literature, as well as solutions that the authors have developed. The paper is divided into 5 sections. Some techniques, which have appeared in the literature, will be discussed in Section 2. In section 3, we will discuss the proposed techniques; specifically offset switching techniques to compensate for the ohmic drop across the switch and techniques for the elimination of the loading effects of the interpolator. There will be a brief discussion of potential ping-pong techniques that can be used in resistor string converters in Section 4. And finally, we will conclude our discussion with a brief summary.

## 2. CURRENT LITERATURE

There are several techniques to compensate for the loading of the interpolator on the coarse resistor string that are currently proposed in the literature and patents. The major advantage of these methods is the elimination of the buffer amplifier, which contributes to an immediate improvement in speed. However, the circuit must now be modified to eliminate the error current inherently drawn by the interpolating resistor string.

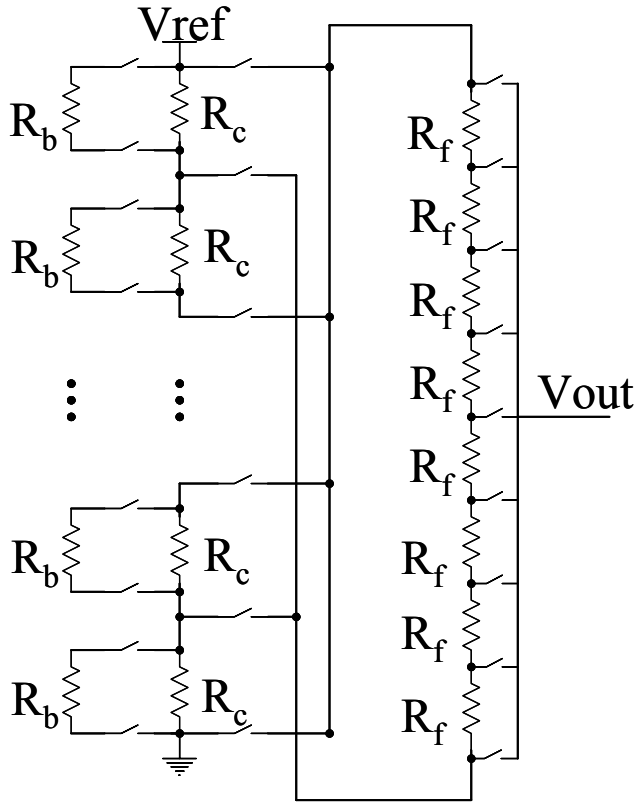


Figure 2: Dual Resistor String DAC with Buffer Resistors

In figure 2, buffer resistors, which compensate for the loading of the interpolator, are added in parallel to each coarse string resistor with a resistance equal to the total resistance of the interpolator. While this effectively reduces the size of the coarse resistor string it also increases the current draw of the DAC. This actually improves the performance of this architecture because the buffers require additional switches, which increase the capacitive loading on the main resistor string that slows down the dynamic performance of the DAC. While the advantage of this technique is the effective elimination of the interpolator loading, there is one major weakness in that it does not eliminate the voltage drop across the coarse tap selection switch. Two other major disadvantages are the added loading of the buffer control switches and the additional logic required to control the buffer resistors [2].

Another technique that is a natural expansion on this patent was discussed by Pelgrom [3]. The method uses interpolation resistors placed in parallel with all of the coarse resistors. This eliminates the cartwheel or sliding effect of the interpolator but does require added resistors. It also eliminates the need for switching in and out the buffer resistors to eliminate the loading of the interpolator. However, this technique adds complexity to the decode logic and  $2^n$  switches to the output.

Rivoir et al. in US patent no. 5,703,588 implement a current biasing scheme to eliminate the buffer amplifier (figure 3). In this method, the inventors apply an appropriate bias current

through the interpolator thus eliminating its loading. The bias current is applied at the top of the interpolator and an equal current is sourced from the bottom of the interpolator. Additional transistors are used to allow the interpolating resistor string to go nearly rail-to-rail in the case where  $V_{refn}$  or  $V_{refp}$  are at or near the rail voltages [4]. The major limitation of this structure is the matching requirements of the mirrors that convey the currents. Any errors in the matching of the transistors sinking and sourcing current will result in an error current applied to the coarse resistor string. These errors will directly impact the linearity of the data converter. Additionally, the use of the transistors to pull the interpolator completely to the rail voltages, in the case where  $V_{refn}$  and  $V_{refp}$  are near the rail voltages, also creates the possibility of errors due to the ohmic drop across these transistors.

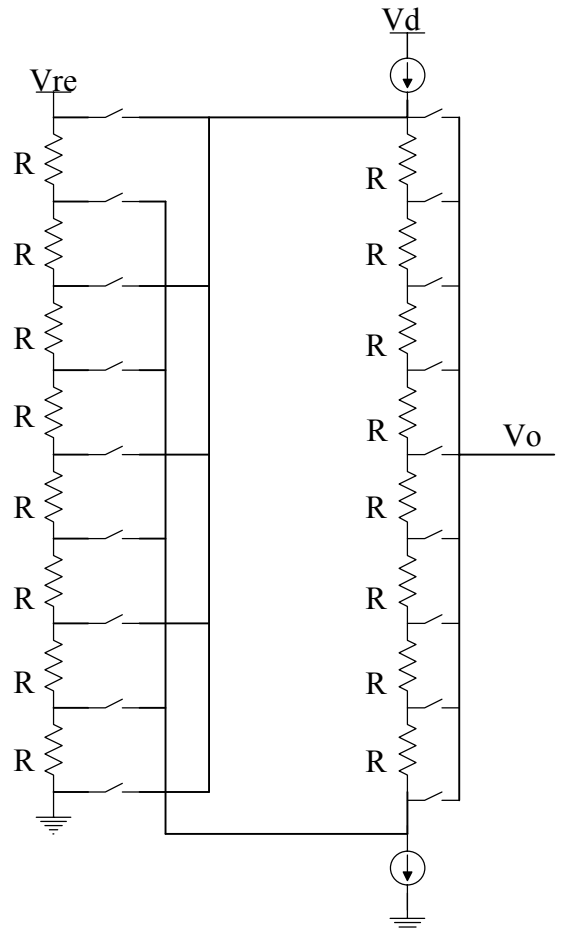


Figure 3: Dual String DAC with Current Source Isolation

### 3. TECHNIQUES FOR ISOLATING INTERPOLATORS

In addition to the above techniques, we have identified additional methods for isolating the interpolator from the main coarse resistor string in R string DACs or compensating for the ohmic drop across the interpolator switch.

The first techniques identified are best described as offset switching techniques. In these methods, the interpolator itself compensates for the resistance of the switch. In addition, these techniques allow for direct polling of the MSB voltages of the interpolator without directly connecting the output to the coarse resistor string. This potentially simplifies the logic design and reduces the capacitive loading on the coarse resistor string.

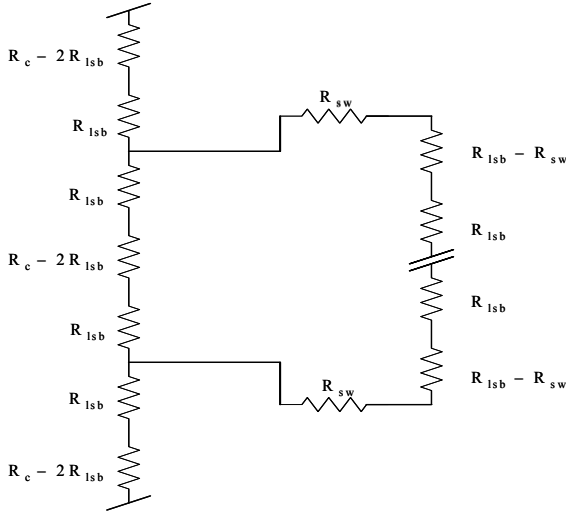


Figure 4: Offset Switching with Sub-Tap

In the first technique, sub-taps are added to the coarse string resistors at one least significant bit (LSB) drop above and one LSB drop below the coarse taps. In addition, the coarse resistors are reduced by 2 LSBs. The switches connecting the interpolator to the coarse resistor string are connected to these resistor tap points. The interpolator in this design has one extra resistor added minus the on resistance of the coarse selection switch. This is illustrated in figure 4. This allows for the compensation of the switch resistance while not directly tapping the coarse resistor string. This simplifies the logic design of the converter and reduces the capacitive loading on the coarse resistor string.

The next method, illustrated in figure 5, uses an approach similar to Rivoir. An extra LSB resistor is added to the interpolator and a current equal to the current flowing in the interpolator is applied to the extra resistor. This again allows for the selection of the output value of the coarse selection while compensating for the resistance of the coarse selection switch. Additionally, the end resistors are reduced by the value of the on resistance of the coarse selection switch.

While these methods compensate for the ohmic drop across the coarse selection switch they have a major drawback in not isolating the coarse resistor string from the loading of the interpolator. These techniques could then use a method such as the buffer resistors as described above to isolate the coarse resistor string from the loading of the interpolator.

Other alternative methods will now be discussed to potentially eliminate the loading effect of the interpolator. The primary

method to achieve this is to capacitively couple the interpolator to the main coarse resistor string. One technique for doing this is to use a cascade of level shifters. In this configuration, two level

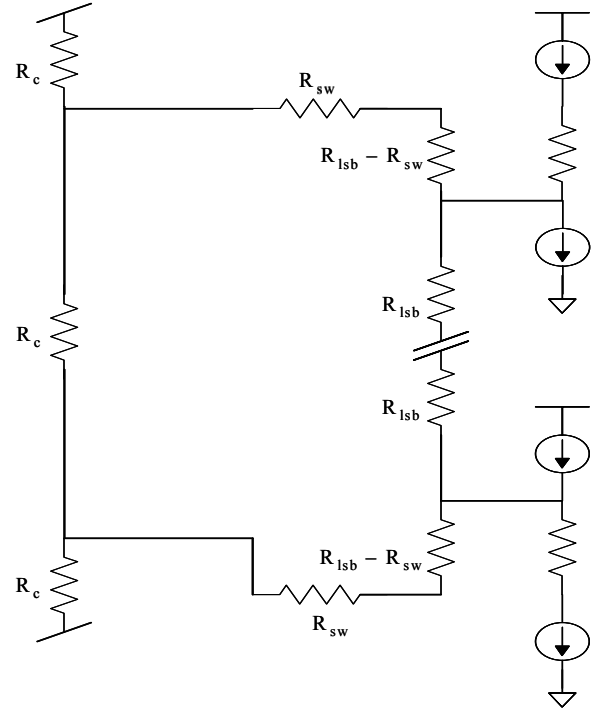


Figure 5: Compensation for Switch Resistance

shifters are used to step down and then step back up the voltage level selected from the main coarse resistor string, as illustrated in figure 6. The advantage in this circuit is the ability to capacitively isolate the interpolator with minimal loss of speed.

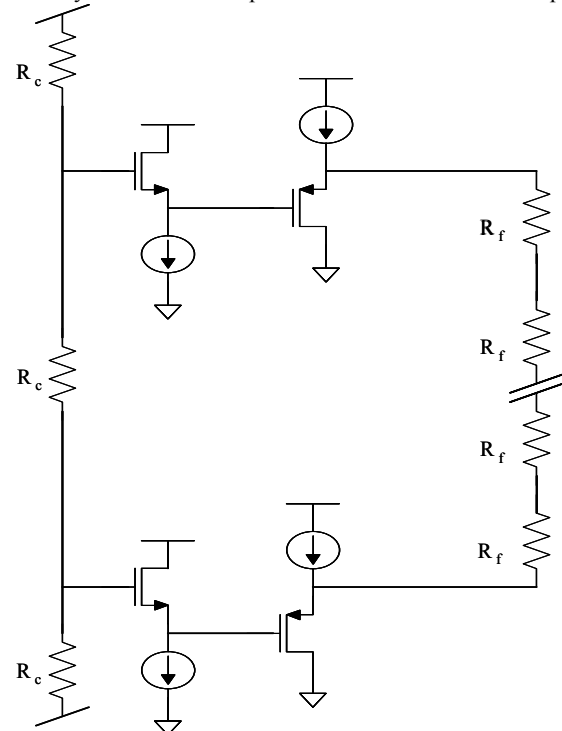


Figure 6: Isolation of Interpolator with Level Shifters

In addition, the ohmic resistance of the selection switches, as well as the loading of the coarse resistor string, is completely compensated by the interpolator. The major drawback of this circuit is the matching of the  $V_{ds}$  drops across the NMOS and PMOS devices. This can be improved through the use of the control loop illustrated in figure 7. However, the major disadvantage of this circuit becomes the offset of the amplifier.

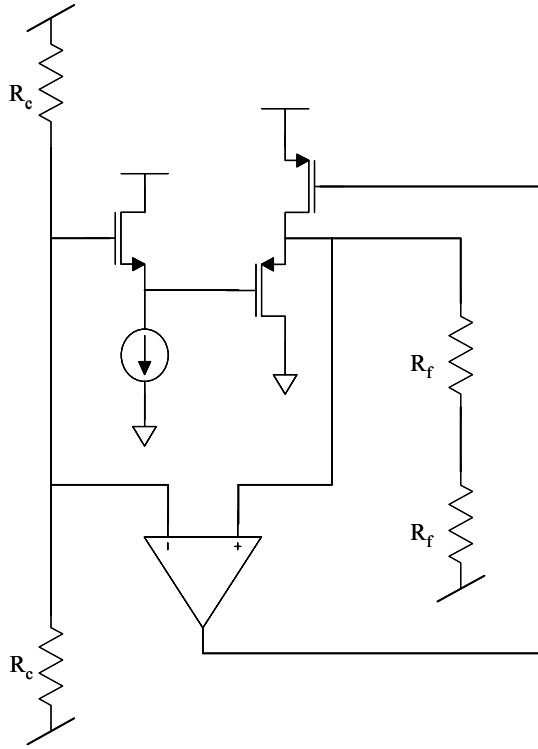


Figure 7: Improved Isolation of Interpolator with Level Shifters

Another potential solution is the use of alternative interpolators. Yilmaz discusses one such alternative in patent number 6,246,351. Here, a current steering approach is used for the interpolator as illustrated in figure 8. In this approach, Yilmaz uses independent source coupled pairs tied to a common load. The non-diode connected input to the load acts as a current summing node. As the thermometer coded least significant bits increase, the output voltage increases to equilibrate the current in the load [5]. This circuit has several weaknesses. First is the matching requirement on the sourced coupled pairs. Next is the settling of the feedback amplifier, which will band limit the output of the DAC. Finally, there is a significant increase in capacitive loading, due to the  $2^{N-1}$  source coupled pairs of the coarse resistor string. This final problem can be significantly alleviated through the use of binary weighted current sources.

#### 4. SUMMARY

In this paper we discussed several techniques to enhance interpolating resistor string digital to analog converters. The

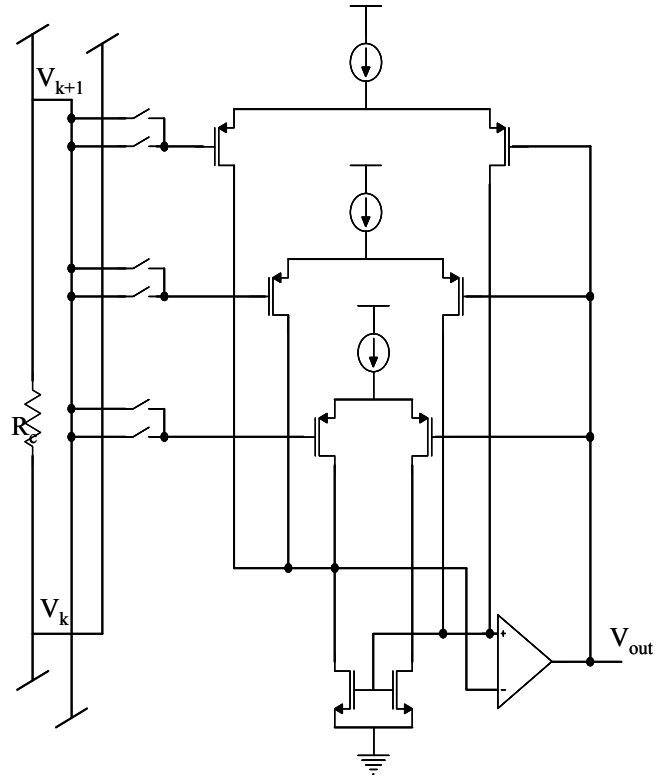


Figure 8: Current Steering Interpolator

most common problems relating to this architecture are the ohmic drop across the selection switch and the loading of the coarse resistor string. There are two ways to eliminate these errors. One is a combination of compensating for each independently and the second is to capacitively couple the coarse resistor string to the interpolator.

#### 5. REFERENCES

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- [2] T. Yuasa, O. Kobayashi, and K. Gotoh, "Digital-to-analog converter having resistor networks," *U.S. Patent*, No. 5,252,975, Oct. 12, 1993.
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- [5] Yilmaz, "LSB Interpolation circuit and method for segmented digital to analog converter," *U.S. Patent*, No. 6,246,351, Jun. 12, 2001.