*A BLIND IDENTIFICATION ALGORITHM FOR DIGITAL CALIBRATION OF PIPELINED ADC

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ABSTRACT

A blind identification based algorithm for calibration of pipelined ADC is discussed in this paper. In contrast to traditional approaches that use one highly precise input stimulus to characterize the device, the approach adopted here is based on providing multiple inputs with nonlinearities of separated spectrum to the device-under-test (DUT). A correction code for each output of ADC is determined, which is then used to calibrate the device. Simulation results show that using the algorithm, trip point error of a 16-bit pipelined ADC with original INL of hundreds of LSBs can be decreased to less than 1 LSB, while input signals of 6-bit linearity are identified to more than 12-bit accuracy. The relaxed requirement of the input signal makes it practical to be generated on-chip and hence is a promising solution for Analog and Mixed-signal Built-In-Self-Test (AMBIST).

1. INTRODUCTION

Testing of Analog and Mixed-signal circuits is becoming an important issue that not only affects the overall production cost but also the time-to-market for most products [1]. With rapid increase in the level of integration, more and more circuitry is added in a small area, which in turn results in longer testing time and increased testing costs. The use of commercial testers in a production testing environment not only requires initial investment on the high-cost testers, but also the cost associated with test time. The need to limit or reduce such costs necessitates the development of a new approach for designing Mixed-signal circuits with integrated Built-In Self-Test solutions.

The obvious apparent advantage of a BIST solution and the end-goal in most proposed BIST approaches is the reduction or elimination of the costs associated with using production testers. However, BIST solutions are also suitable to test deeply embedded modules that might be difficult to access otherwise through an external tester. Another advantage associated with an AM-BIST approach coupled with the built-in calibration capability is the ability to actually enhance performance specifications while still maintaining yield targets. Also, by combining AM-BIST strategies with the built-in calibration capability, certain inherent matching requirements at design can be relaxed for some class of circuits.

One main obstruction towards realizing a complete BIST solution is the unavailability of sufficient data about the input signal. Although considerable research efforts [2][3][4][5] has been done towards generating precise input stimuli on-chip, the task of precise signal generation is becoming more challenging as we move towards higher resolution products. However with the vast amount of information available about data converter operation and about the various standard methods of signal generation on-chip, certain practical assumptions can be made about the system and the signal that can enable identification of the system without having access to the signal source. An approach towards identification of the stimuli and characterization of flash ADCs was discussed in authors' previous work [6]. This paper focuses mainly on simultaneous identification of nonlinear input signals and calibration of pipelined ADCs.

2. ALGORITHM DESCRIPTION

In the approach described here, multiple input signals with definite non-linearities will be used to calibrate the device. To understand the general approach, let us consider a non-ideal input 'x' that is given to the DUT. The non-ideal input can be represented as:

$$x=t+f(t)+n_i \quad (1)$$

where t represents the intended ideal input, f(t) denotes the various nonlinear terms that are part of the input signal, and n_i is any additional noise term present. For the purpose of identification, f(t) is parameterized by a set of basis functions $\{f_i(t), i=1, 2, \ldots\}$ as shown below:

$$f(t)=a_1h_1(t)+ a_2h_2(t)+\ldots \quad (2)$$

The parameters $\{a_i, i=1, 2, \ldots\}$ are the coefficients of the various basis functions. Let the actual output digital code of the pipelined ADC corresponding to input 'x' be represented as 'y(x)'. 'y(x)' can then be split into various terms as shown in (3),

$$y(x)=x+E(x)+q_n \quad (3)$$

where E(x) denotes any error in the ADC performance, and q_n the inherent quantization noise. Depending on the nature of the ADC nonlinearity, the output code y(x) may be quite different from the actual intended output. To digitally calibrate the ADC is

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to provide an error correction code e(y) for each output code 'y' so that the calibrated ADC will have output code

$$y_c=y-e(y) \tag{4}$$

The goal of the proposed algorithm is to determine an optimal code e(y) such that the mean square output error after correction is minimized:

$$\text{Min } E\{(y_c(x)-x)^2\} \tag{5}$$

Theorem: Suppose the original ADC has differential nonlinearity DNL, the best achievable integral nonlinearity INL, for the calibrated ADC is given by:

$$INLc = (1+DNL)/2 \tag{6}$$

Note: If the input signal 'x' to the ADC is known precisely and its levels can be varied with arbitrary resolution, then the calibrated ADC can achieve the performance bound given by (6). If the input signal 'x' is not known precisely or if it is generated by a finite resolution DAC, the achievable INL for the calibrated ADC will be larger than the bound.

With this general approach in mind, the following describes a way to obtain the required correction codes. Two non-ideal input signals, whose nonlinearities have different spatial spectral distribution, are used for this purpose. Let the 1st input signal be expressed as:

$$X1=t+f(t)= t+ a_1f_1(t)+a_2f_2(t)+\ldots \tag{7}$$

where the nonlinearity f(t) in (1) is parameterized by basis functions $\{f_i(t), i=1, 2, \ldots\}$ and coefficients $\{a_i, i=1, 2, \ldots\}$. With this signal as input, the output of the pipeline ADC at sampling instances corresponding to intended input $t_1, t_2, \ldots, t_n$, is then given by:

$$\begin{aligned} y_1&=t_1+ a_1f_1(t_1)+ \ldots+a_mf_m(t_1)+e(y_1)+n_1 \\ &\ldots \\ y_n&=t_n+ a_1f_1(t_n)+ \ldots+a_mf_m(t_n)+e(y_n)+n_n \end{aligned} \tag{8}$$

Only the first 'm' basis functions are used in the algorithm. The choice of 'm' is decided based on a trade-off between the computational complexity and the accuracy of the final calibrated result. The quantization noise, higher order terms of $e(y_i)$ and any input nonlinearity that is not modeled by the 'm' basis functions are combined as a single noise term n_i.

If the input signal is sampled at a high rate, then multiple input samples may correspond to the same output code of the ADC. By re-grouping the equations in (8) according to the output code and averaging among each group, the set of equations in (8) is reduced to

$$\begin{aligned} 1&=t^{(1)}+a_1f_1(t^{(1)})+ \ldots+a_mf_m(t^{(1)})+e(1)+n^{(1)} \\ 2&=t^{(2)}+a_1f_1(t^{(2)})+ \ldots+a_mf_m(t^{(2)})+e(2)+n^{(2)} \\ &\ldots \\ N&=t^{(N)}+a_1f_1(t^{(N)})+ \ldots+a_mf_m(t^{(N)})+e(N)+n^{(N)} \end{aligned} \tag{9}$$

where, N is the total number of different codes present at the output of the pipelined ADC. The superscript 'i' in $t^{(i)}$ denotes the output code i. By grouping the terms and averaging them the noise term gets averaged and hence can be much less than n_i if the number of samples per bin is much greater than 1.

Writing equation (9) in matrix form, we get

$$\mathbf{Y}=\mathbf{T_1}+\mathbf{F}*\mathbf{A}+e(\mathbf{Y}) \quad +\mathbf{N_1} \tag{10}$$

where

$$\mathbf{A}=[a_1, a_2,\ldots, a_m]^T$$

$$\mathbf{Y}=[1, 2, \ldots, N]^T$$

$$e(\mathbf{Y})=[e(1), e(2), \ldots, e(N)]^T$$

$\mathbf{T_1}$ is the vector of averaged ideal inputs for 1st input, while $\mathbf{F}$ is associated the basis function matrix.

Next a 2nd input signal with a different nonlinearity as represented by (11) is given as input to the ADC.

$$X2=t+g(t)= t+ b_1g_1(t)+b_2g_2(t)+\ldots \tag{11}$$

where the nonlinearity g(t) is parameterized by basis functions $\{g_i(t), i=1, 2, \ldots\}$ and coefficients $\{b_i, i=1, 2, \ldots\}$. Using the same approach as described earlier for input X1, we get the matrix equation for 2nd input

$$\mathbf{Y}=\mathbf{T_2}+\mathbf{G}*\mathbf{B}+e(\mathbf{Y}) \quad +\mathbf{N_2} \tag{12}$$

$\mathbf{Y}$ and $e(\mathbf{Y})$ are the same as those in (10), $\mathbf{T_2}$ is the vector of averaged ideal inputs for 2nd input, $\mathbf{G}$ is the associated basis function matrix and

$$\mathbf{B}=[b_1, b_2,\ldots, b_m]^T$$

Subtracting equation (12) from (10), the terms $\mathbf{Y}$ and $e(\mathbf{Y})$ get cancelled and we get:

$$0= \mathbf{T_1}-\mathbf{T_2}+ \mathbf{F}*\mathbf{A}-\mathbf{G}*\mathbf{B}+\mathbf{N_1}-\mathbf{N_2} \tag{13}$$

The parameter vectors A and B are then obtained by using least squares estimation, and is given by (14)

$$[\mathbf{A_{est}}^T \mathbf{B_{est}}^T]^T=(\mathbf{C}^T \mathbf{C})^{-1} \mathbf{C}^T (\mathbf{T_2}-\mathbf{T_1}) \tag{14}$$

where $\mathbf{C}=[\mathbf{F} \ -\mathbf{G}]$. The noise term $\mathbf{N_1}-\mathbf{N_2}$ drops in the least square solution if it is uncorrelated with the basis functions in $\mathbf{C}$. This is a fairly good assumption since $\mathbf{N_1}-\mathbf{N_2}$ contains averaged values of residual modeling errors in 'f' and quantization errors. With the parameter vectors available, the error correction code is given by either

$$e(\mathbf{Y})=\mathbf{Y}-\mathbf{T_1}-\mathbf{F}*\mathbf{A_{est}} \tag{15}$$

or

$$e(\mathbf{Y})=\mathbf{Y}-\mathbf{T_2}-\mathbf{G}*\mathbf{B_{est}} \tag{16}$$

or suitable weighted average of the two.

Although we will not be able to provide analytical performance analysis of the proposed algorithm due to page limitation, the efficiency of the approach will be verified through simulation in section 4. Specifically, the simulation results will show that the proposed algorithm can lead to a calibrated INL that is only slightly larger than the bound given by (6). We will also show that by a little bit more calculation, we can use the estimated $e(\mathbf{Y})$ vector to characterization the trip points of the pipelined ADC,

and the accuracy for trip point identification is not limited by the DNL.

3. PIPELINED ADC MODELING

An n-bit pipeline ADC (with 1 bit/stage) is composed of n identical stages as shown in Figure.1.

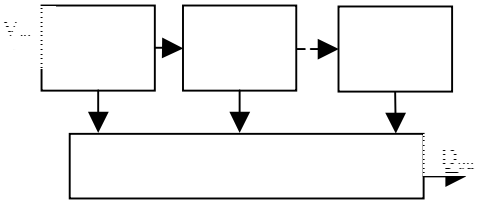

Figure.1. n-bit Pipeline ADC

Each stage of the pipeline can be modeled as shown in Figure.2.,

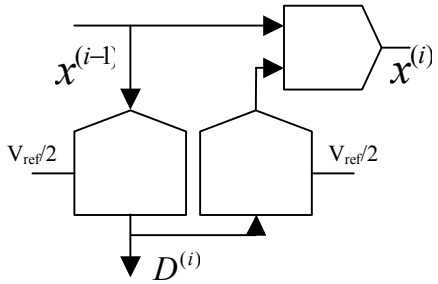

Figure.2. Individual stage of pipeline ADC

where for the i[th] stage, $x^{(i-1)}$ denotes the analog input to this stage which is also the output from the previous stage, $x^{(i)}$ the analog output to be sent to next stage, and $D^{(i)}$ the 1-bit digital output, respectively. Assuming that the sources of non-idealities in the pipelined ADC are only due to gain error of the "multiply-by-2" stage, offset of the 'multiply-by-2' amplifier and the offset voltage of the 1-bit ADC, the mathematical model of one stage can be written as follows.

$$\begin{aligned} D^{(i)} &= \tilde{\text{sgn}}(x^{(i-1)} - (V_{ref}/2 + \delta_i)) \\ x^{(i)} &= g_i(x^{(i-1)} - D^{(i)}V_{ref}/2 - \theta_i) \end{aligned} \tag{17}$$

where δ_i, θ_i, g_i are the offset voltage of the 1-bit comparator, offset of the "multiply-by-2" stage and gain of the "multiply-by-2" stage respectively, and

$$\tilde{\text{sgn}}(x) = \begin{cases} 0, & x < 0 \\ 1, & x > 0 \end{cases} \tag{18}$$

The digital code < $D^{(1)}$, $D^{(2)}$,.... $D^{(n)}$ > then corresponds to the output of the ADC for any given input.

4. SIMULATION RESULTS

A non-ideal 16-bit pipeline ADC was modeled as described in section 3. The offset voltages of the comparator and "multiply-by-2" stage were randomly generated and were limited to 0.5% of Vref. The gain error of the "multiply-by-2" stage was bounded between +/- 0.5% of the ideal value. The INL and DNL pattern of the modeled ADC is shown in Figure.3. and Figure.4.

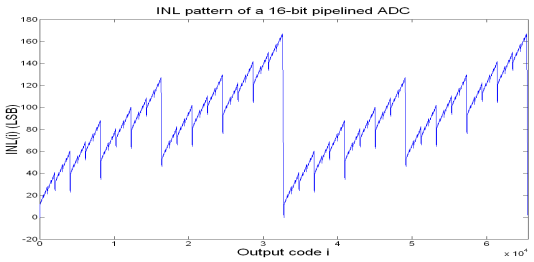

Figure.3. INL pattern of a 16-bit ADC

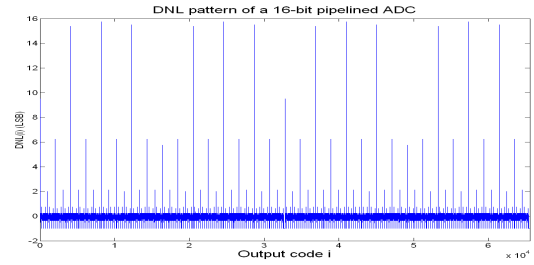

Figure.4. DNL pattern of a 16-bit ADC

The two nonlinear inputs to the ADC were modeled as follows:

$$X1 = t+0.03*\sin(pi*t)+0.01*\sin(2*pi*t) \tag{19}$$

$$X2 = t-0.01*\sin(5*pi*t)-0.001*\sin(6*pi*t) \tag{20}$$

Even though only two basis functions were considered in simulations, more terms could be included to get better accuracy of the final result.

Using the two inputs, the algorithm was simulated to identify the correction codes for the modeled ADC. Figure.5. gives the plot of the INL of the ADC after calibration with e(**Y**). It can be seen that INL of several hundred LSBs can be calibrated to less than 8 LSB, which corresponds to half the DNL value before calibration. This indicates that with the proposed algorithm, the ADC can be calibrated to the accuracy set by DNL. It's in agreement with the theorem explained in Section 2.

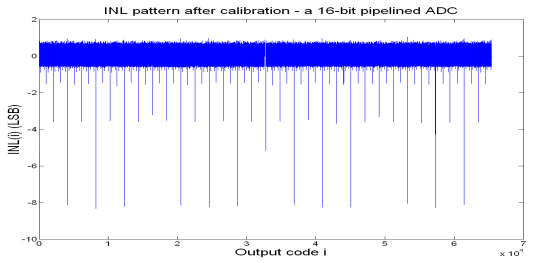

Figure.5. INL of the ADC after calibration

Also using the algorithm, the actual trip points of the pipelined ADC can be accurately identified. As shown in Figure.6, the residue error in trip point after identification is less than half LSB. This means that by using the information provided by the algorithm, with some structural modifications, we can calibrate the ADC to have INL less than 1 LSB, i.e. 16-bit accuracy. This will dramatically increase the yield of the product.

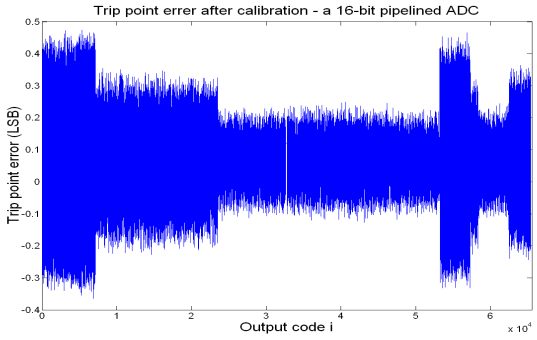

Figure.6. Difference between introduced and identified trip point

Next a set of 30 runs of 14 bit pipeline ADCs were simulated. Different random combination of offset errors and gain error was chosen for each run. The algorithm was then implemented to identify and calibrate the trip points of each of the ADC. Figure.7. gives a plot of maximum trip point error in each run before and after calibration. The results indicate that 14 bit ADCs with initial maximum trip point error in the range of 39LSB~43LSB (corresponding to 8 bit accuracy), can be calibrated to within 0.5LSB (corresponding to 14 bit accuracy).

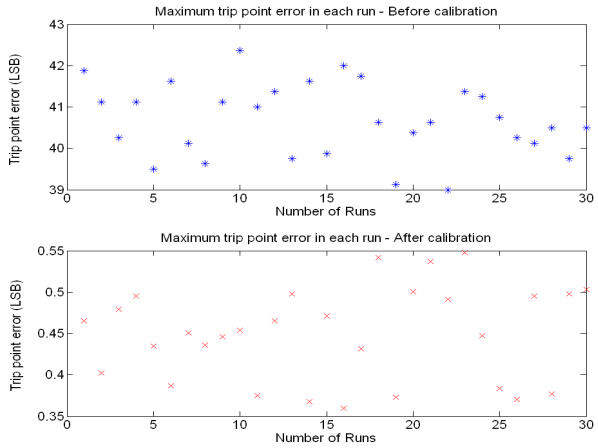

Figure.7. Simulation results for 30 runs of 14-bit ADC

Further simulations with more number of basis functions were performed and the results were in agreement to the theoretical estimation.

5. CONCLUSION

A blind identification approach to digital calibration of pipelined ADCs has been introduced. The algorithm is based upon using multiple input signals that are given to the DUT. The outputs of the DUT are then analyzed to characterize/calibrate the device. Simulation results for 16-bit pipelined ADCs are presented. Results indicate that with input signal of around 6 bit linearity, the device can be calibrated from an initial 8-bit accuracy to nearly 16-bit accuracy. Results of multiple 14 bit ADCs are also presented that confirm the robustness of the algorithm.

6. REFERENCES

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