A HIGHLY LINEAR CMOS AMPLIFIER FOR VARIABLE GAIN AMPLIFIER APPLICATIONS*

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ABSTRACT

This paper reports the design of a highly-linear CMOS amplifier for Variable Gain Amplifier (VGA) applications. A better than –60dB 3rd harmonic distortion at differential output level of 1V peak-to-peak is obtained by utilizing a linearization scheme that does not rely on the active devices. The amplifier maintains 3dB bandwidth over 300MHz. A noise figure at 8.6dB is obtained with source impedance of 200 ohms. It is implemented in standard CMOS 0.25u process and consumes 40mA current under 3.3V power supply.

I. INTRODUCTION

Variable gain amplifier finds a very wide range of applications where Automatic Gain Control (AGC) is needed, such as hearing aids, imaging and wireless communications. In such applications, the signal strength varies over a large range. VGA is used for either controlling the transmission signal power or adjusting the received signal amplitude. In order to let system work under such situations, a feedback loop is usually required to implement AGC. VGA plays a key part in this loop. Usually a highly linear VGA is needed to maintain good system linearity. The linearity of the VGA is almost entirely determined by its amplifier section. A highly-linear amplifier design is crucial for the linearity of the VGA.

Sophisticated analog design usually realized using expensive BiCMOS, SiGe processes. Large-scale integration of a mixed-signal system or SoC in deep sub-micron process can only be achieved when analog circuits are also implemented with ultra-short channel devices in CMOS. This project is trying to implement a highly linear CMOS amplifier with the performance that was only achievable in more expensive processes before.

This design is a part of a CMOS digitally-controlled variable gain amplifier project. Its function is to provide a fixed gain at around 36dB with very low distortion level. Some design challenges and specifications in this design are:

(1) Maintains enough bandwidth (>250MHz)
(2) The third harmonic distortion for input signal at f=160MHz should be no worse than –55dB@Vopp=1V
(3) Less than $2.5nV/\sqrt{Hz}$ input-referred thermal noise
(4) Fixed differential output impedance of 600 ohms

In section II, an overview of the linearized amplifier design will be given. Our highly-linear CMOS amplifier will be discussed in section III. And finally, its performance will be evaluated with some simulation results in section IV.

II. DESIGN CONSIDERATIONS AND CANDIDATES

To achieve high linearity, the first natural choice would be the negative feedback configuration. But the limited speed in CMOS compared to BiCMOS or BJT technologies may make this approach not viable. Several investigations were conducted to see if there is enough bandwidth for this approach. Unfortunately, the projected CMOS process doesn't have the luxury of extra bandwidth to play with negative feedback.

Our focus shifted to open loop configuration. Compared to the feedback amplifier, several issues need to be solved in the open loop situation. First, the gain of the amplifier needs to be stabilized within a certain range (±3dB). Though the gain requirements for the amplifier is not very tight, it should not vary too much over process variations and temperatures, which is usually the case if the gain of the amplifier relies on the transconductance of the devices. Secondly, the amplifier needs to be linearized because the MOS transistors are inherently not quite linear especially in modern small-feature size process that is prone to short-channel effect and deviates from the classic square-law equation.

We chose to use a two-stage open loop configuration for this amplifier design. The first stage is a transconductance stage that converts the input small signal voltage to current. The second stage is a simple current mirror which drives a

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resistive load of 300 ohms. This approach can also meet the requirement of 600 ohms differential output impedance easily.

At first, we investigated the linearity performance of the traditional differential pair shown in Figure 1(a) (only transconductance stage is shown here). The best distortion performance that we can get is –51dB@Vopp=1V for f=160MHz. The bandwidth for this structure is about 400MHz which is good though.

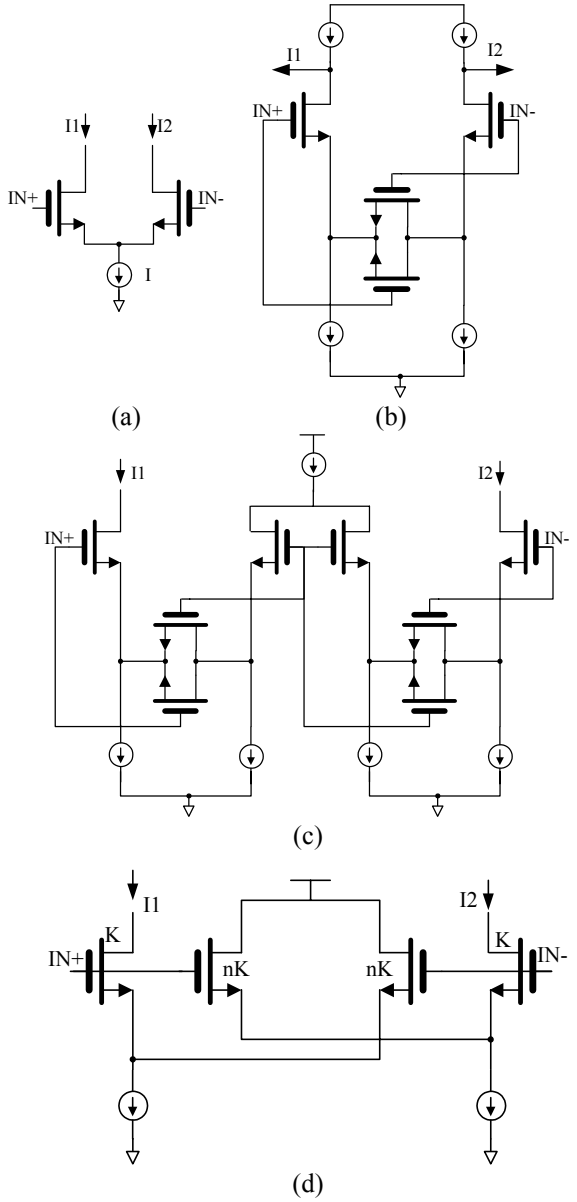

Figure 1. Candidates for linearized transconductance stage

In order to achieve better linearity, several linearization schemes for the transconductors were compared [2] [3] [4]. The topology proposed by Krummenacher and Joehl [2] is shown in Figure 1(b). It is basically a source degeneration structure. The gates of the triode region transistor are connected to the input signal to improve the transconductance at large signals. The best distortion performance that we can get for this structure is –58dB. Another structure proposed by Silva-Martinez et al. is shown in Figure 1(c). It is the extension for the previous approach. The input signal is further split over two input stages to further improve the linearity. Unfortunately, in our simulation, there is almost no improvement over the previous approach. The best distortion performance that we can get is –58dB. The linearization scheme proposed by Nedungadi [4] is shown in Figure 1(d). The transistors labeled nK are n times larger than other transistors. The idea was to use those big transistors as source followers to realize the floating voltages sources in order to maintain a constant sum of gate-source voltages so that a linear relationship of differential input voltage and differential output current can be obtained. The best distortion performance that we can get is –57dB. Furthermore, those two big transistors drain a lot of current compared to other structures.

These linearization schemes can bring us moderate improvements. The ideas behind them were all based on the square-law model of the MOS devices. Compared to long-channel processes at the time when they were published, the improvements that can be obtained from those schemes in short-channel processes are limited. This is due to the large deviation from the classic square-law model for the short-channel devices. Because of the short-channel effects, it's not a good choice to use active devices to linearize the transconductor in order to achieve high linearity. Discussed in next section is a linearization scheme that doesn't depend on the MOS devices.

III. CIRCUITS IMPLEMENTATION

A. Transconductor strucrure

A transconductor structure similar to the structure used in [1] is shown in Figure 2. In [1], they used a "floating linear resistor" formed by triode region transistors to linearize the transconductor. Because the resistance value in our design is small, we replaced the floating linear resistor with a real resistor in order to get better linearity.

The transconductance stage includes M1, M2, R and the current sources I1 and I2, while the current mirror stage is consist of M3-M6 to drive resistive loads.

Current I1 is forced flew through M1 and M2 at any time that keeps the constant Vgs' for both M1 and M2. Thus the p-channel devices will serve as voltage followers buffering the input small signal across the resistor R. The small-signal

current will then flow through M3 and M4 and be mirrored to the output to drive the loads R1. Theoretically, the transconductor stage is very linear and it doesn't rely on the square law of the transistors.

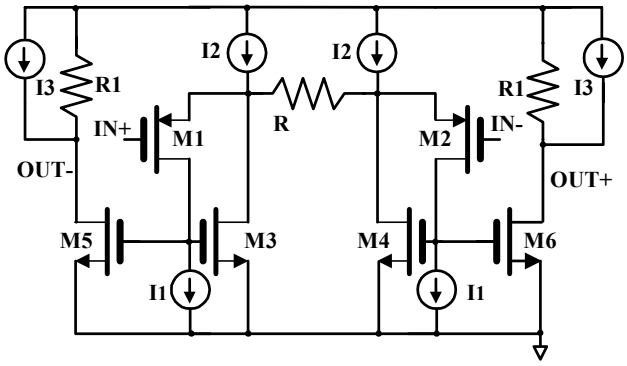

Figure 2. Structure of the open-loop amplifier

This structure also takes care of the gain stability problem for the open loop amplifiers. The transconductance of the first stage is simply $Gm = 1/R$. The gain of the amplifier is given by:

$$A = \frac{R1 // Rx}{R} M$$

where M is the mirror gain, Rx is the external load.

The gain of the amplifier is determined by the mirror gain and the ratio of the two resistances. This property greatly enhances the gain stability. Actually, the gain of the amplifier will change because the sheet resistance of the integrated resistors varies while the external resistive load keeps constant. Simulation results considering this effect will be given later in this paper which shows an acceptable performance.

Because the output impedance of the amplifier is fixed in order to interface with the loads, the only two design variables that we can control are R and M. A combination of them must be carefully chosen to ensure the low distortion and ease the realization of the resistors.

To get the best linearity out of the current mirror, the output common mode voltage was chosen to be around 1.1V. Because the output impedance of our design is fixed, the quiescent current level in the output transistor would be limited in a small range. This limited quiescent current in the output stage can't sustain large current swing while still maintain the required linearity. Two current sources were added to the output devices to increase the quiescent current in M5 and M6. These additional currents give an additional 4dB better linearity.

The input transistors were chosen to use PMOS devices. This is based on several considerations. First, its body can be connected to the source in the projected N-WELL CMOS process. It eliminates the body effect and improves the linearity. Secondly, PMOS devices are less noisy than NMOS devices. Finally, to complement the design, NMOS current mirrors can be used that have better frequency response than PMOS current mirrors with NMOS input stage.

B. Linearity discussion

Current mirrors contribute part of the overall nonlinearity. The intuitive thoughts to improve the linearity of the current mirrors were to use cascode current mirrors. Hope the additional cascoded devices can shield the drains of M5 and M6 from large voltage swings. But several investigations revealed that this approach has little to do with the linearity of the amplifier. We have two observations about the linearity performance that apply for both simple and cascode current mirror configurations under small-feature size processes and BSIM3 models:

(1). Couplings from the output (drains of M5 and M6) back to the gm stage (through gates of M3 and M4) have a major impact on the linearity of the gm stage at high frequencies. At low frequencies, the linearity of the signal current of the gm stage is keeping constant and very high. It starts to get worse when the input frequencies are higher than 100MHz.

(2). Small drain voltage swings at the output devices (M5 and M6) do not necessary give a better linearity compared to larger swings. The linearity is more depend on the harmonies between two drain voltages, i.e. it would be more linear to have a constant large difference between two drain voltages than a variable small difference between them.

IV. SIMULATION RESULTS

This project was designed in a standard CMOS 0.25u process. It was simulated using HSPICE simulator and BSIM3, level 49 models with package and power supply models at all-transistor level. The accurate simulation option was switched ON in order to get good approximation for the expected measurement results.

A. Gain Characteristics

The AC response of the amplifier at room temperature and normal device models is shown in Figure 3. The 3dB bandwidth of the amplifier is larger than 350MHz. A 100MHz margin on bandwidth in our design would bring more confidence in the future testing.

B. Linearity

The simulation results for the linearity of the amplifier under different process corners are shown in Table 1. This measurement was done at the input signal frequency f=160MHz.

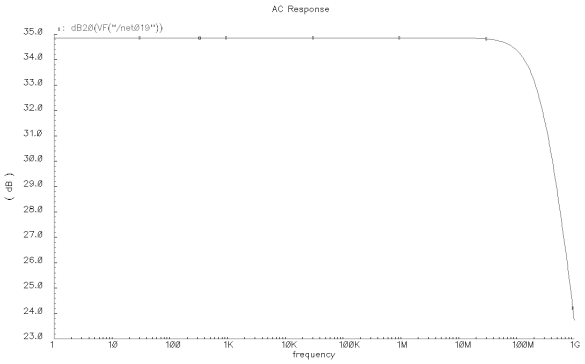

Figure 3. Gain response of the amplifier

Table 1. Linearity@Vo_pp=1V (HD3)

	Normal	Fast	Slow
Linearity	-62.8dB	-62.6dB	-61.8dB

Some margin was left to meet the requirements for the linearity because the transistor mismatch was not taken into account. It's not surprising to see the worse real measurement results.

C. Effects of sheet resistance variation

According to the data sheet of the projected process, its sheet resistance for poly resistor varies about ±20%. Shown in Figure 4 and Table 2 are the gain response and the linearity performance considering the resistance variation, i.e. all the integrated resistors vary their resistance while the external load keeps constant. The gain variation is controlled within ±1dB and the linearity also meets the requirements.

Table 2. Effects of the sheet resistance variation

	Linearity	Gain
Rmax	-62.3dB	35dB
Rmin	-61.6dB	34.4dB

D. Thermal noise and Noise Figure

The simulated input equivalent noise for the amplifier is $1.44nV/\sqrt{Hz}$. It is the average value over the frequency range of 100MHz to 500MHz which covers the entire frequency range of our interest.

Noise figure for the amplifier is 8.6dB assuming 200 ohms source impedance.

E. Temperature variation effects

The temperature effect was also simulated and is shown in Table 3. The amplifier design keeps the acceptable performance on linearity and AC characteristics.

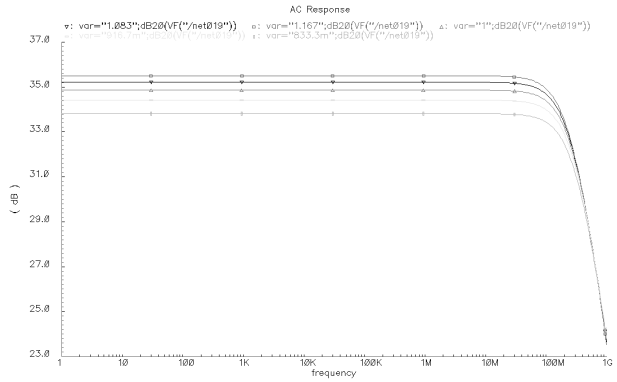

Figure 4. Gain response considering resistance variations

Table 3. Temperature effects on amplifier design

	Linearity	Gain	BW
-40C	-64dB	35.9dB	303MHz
85C	-60.8dB	33.7dB	297MHz

V. SUMMARY

Dedicated analog function can also be realized in deep sub-micron CMOS process. It not only provides acceptable performance, but also cost effective. In this work, we demonstrated the design of a CMOS amplifier with a highly linear transconductance stage. It can also be used as a low distortion building block for very wide applications.

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