An MSB-First Monotonic Switched Capacitor Serial DAC

Mezyad M. Amourah, Saqib Q. Malik, and Randall L. Geiger
Iowa State University
Department of Electrical and Computer Engineering
Ames, IA 50011

Abstract – A monotonic DAC using switched capacitor integrator is presented. For an N-bit digital input sequence, the proposed DAC starts conversion with the MSB and takes N cycles to finish conversion. The DAC samples the reference voltage only once and transfers appropriate charge to an output capacitor. Some issues relevant to the design and their possible solutions are presented.

I. Introduction

Digital-to-Analog converters (DACs) help bridge the digital domain with the everyday analog world. A DAC occupying small area capable of high resolution is of use in many applications. A monotonic DAC always has an increasing analog output with increasing digital input. This behavior is essential in many applications. These applications can tolerate non-linearities but cannot tolerate non-monotonicity. In this paper, a simple switched capacitor DAC is presented that exhibits monotonicity while occupying a small area. The proposed DAC starts its conversion from the MSB instead of the traditional approach of starting from LSB [1].making it suitable for use in cyclic or successive approximation analog-to-digital converters (ADCs).

II. Background

Digital to analog converters operating at moderate speeds and moderate resolutions are used in many applications. These DACs often have a small footprint and consume low power. The classical DAC using two capacitors was proposed in [1] and is shown in Figure 1. The operation of DAC is as follows. The capacitors are designed to be of equal value. The conversion starts with the LSB. The capacitor C_1 is charged to V_{ref} or connected to ground, depending on the value of the bit to be converted. At the same time, capacitor C_2 is discharged by turning on the switch s_4. In the second phase, switches s_1, s_2, and s_4 are turned off and the switch s_3 is turned on. This puts the capacitors C_1 and C_2 in a parallel configuration forcing the charge on C_1 to be shared equally across C_2. The procedure is repeated for all the bits except that the switch s_4 is kept open resulting in the voltage across C_2 converge towards the analog equivalent of the input digital word. Notice that the capacitor C_1 has to be charged to V_{ref} or discharged to ground during each iteration. The conversion starts from the LSB. As a consequence of this latter observation, if this DAC is used as a sub-DAC in an ADC, the ADC will need to convert the input completely before the LSB becomes available for processing by the DAC. This can slow down the operation of the ADC considerably.

Section III describes the concept and operation of the proposed scheme that does not suffer from these drawbacks. Section IV shows an example circuit level implementation. Section V presents simulation results followed conclusion.

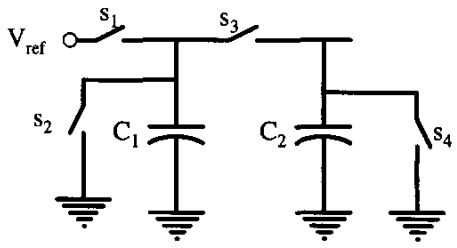

Figure 1. Conventional DAC implementation

III. Circuit Operation

The structure of the proposed DAC is shown in Figure 2. C_1 and C_2 are the same size nominally. ϕ_1 and ϕ_2 are non-overlapping clocks enabled only when ϕ_{start} is low. The conversion process starts with ϕ_{start} going high. This charges the capacitor C_1 to the reference voltage, V_{ref}. Once ϕ_{start} goes low, ϕ_1 and ϕ_2 are enabled. ϕ_1 turns on first resulting in charge sharing between C_1 and C_2 resulting in C_2 getting charged to $V_{ref}/2$. The data stream is fed to the DAC starting with the MSB. If the current bit, b, is a 1, the charge held by C_2 is transferred to the integrator. If the bit is a 0, the capacitor C_2 is discharged to ground. The process continues until the LSB is reached. In each cycle, charge is transferred in quantities corresponding to the bit under conversion from the "master" capacitor C_1 to C_2 and either integrated with output or discarded to ground.

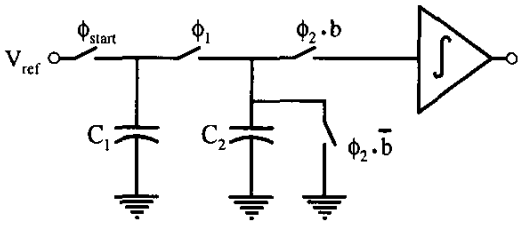

Figure 2: Concept of the proposed DAC

There are two benefits of this approach: First, the intermediate output of the DAC either increases (for an input of 1) or stays the same (for an input of 0). Therefore, the output will always be monotonic. Second, the conversion of the digital input starts with the MSB. The benefit of this becomes clear when this DAC is used as part of an ADC. The sub DAC can start its conversion as soon as the MSB from the ADC becomes available. If the DAC was designed to start the conversion starting from the LSB, the ADC would

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have to finish conversion first before the DAC can start processing its input. The savings in time can be significant.

IV. Circuit Implementation

We next look at a practical implementation of the DAC of Figure 2. An implementation is shown in Figure 3. The integrator capacitor C_4 is discharged at the start of conversion of each word using ϕ_{start} (reset switches not shown for simplicity). As can be seen from the Figure 3, C_1 and C_2

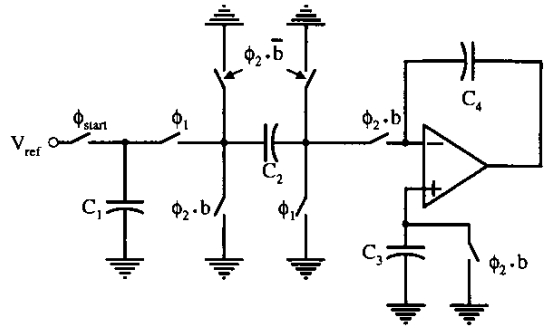

Figure 3: An implementation of the proposed DAC

form a capacitive divider network when ϕ_1 is on. The charge sampled on C_1 earlier during ϕ_{start} is equally divided between the two capacitors. During ϕ_2, depending on the value of input digital bit b, the charge on C_2 is either transferred to C_4 or discarded. For an N-bit DAC, it takes N clock cycles to finish the conversion. At the end of N-cycles, the output is available at the output of the opamp. The output converging to its final value for an input of all 1's is shown in Figure 4.

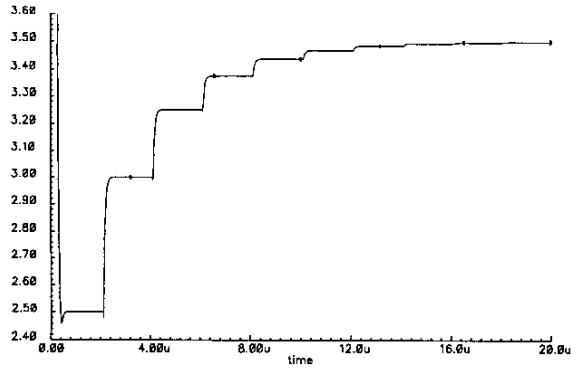

Figure 4: Output for all 1's

V. Design Issues

Several factors can degrade the performance of the proposed design considerably. Some of these design issues will be discussed next.

A. *Charge Injection*

Charge injection from the switches limit the achievable accuracy from this architecture. To alleviate the problems associated with charge injection, the extra capacitor C_3 can be added to the circuit. C_3 can be made the same size as C_2. With the addition of this capacitor, charge injection effects are presented as common mode to the opamp and are reduced by the common mode rejection ratio (CMRR) of the opamp. Additionally, using fully differential architecture and dummy switches can also reduce the nonlinearities caused by charge injection.

B. *Capacitor Sizing and Mismatch*

The capacitor sizes will affect the total power consumption of the DAC. To minimize the power, it is desirable to minimize the size of the capacitors C_1-C_4. However, the *k*T/C noise due to the capacitors considered along with the target resolution will dictate the size of the capacitors. Increasing the size of the capacitors will not only help with reducing the effects of charge injection but will also improve the matching of the critical capacitors. For higher resolution, the conversion can be done at half the speed with capacitor swap algorithm to eliminate capacitor mismatch effect.

C. *Charge Leakage from the "Master" Capacitor*

As explained earlier, the reference voltage is sampled on the "master" capacitor C_1 before the start of the conversion process. This capacitor can be viewed as a "bucket" from which charge is siphoned off for processing by the rest of the circuit. Any leakage of charge from this capacitor will show up directly as error in the output. Repeated charge injection from neighboring switches can also change the charge held by this capacitor. One way to reduce these errors is to make C_1 very large. However, this will require increasing the size of C_2 and C_3 as well resulting in increased power dissipation.

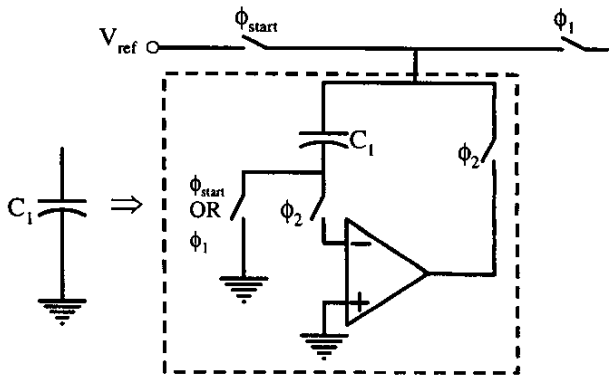

Figure 5: Scheme to hold charge accurately

An alternate approach that does not require increasing the size of C_1 is shown in Figure 5. The capacitor C_1 of Figure 3 is replaced by the network shown in Figure 5. During ϕ_{start} the reference voltage V_{ref} is sampled as before. Similarly, the circuit looks the same during ϕ_1. However, during ϕ_2 when the voltage on C_2 is being processed, the master capacitor C_1 is placed in the feedback loop of an opamp forcing the voltage across C_1 to remain constant. Any perturbations due to charge injection of charge loss from C_1 are compensated by the opamp. As a result, the charge corresponding to the reference voltage sampled across C_1 at the start of the conversion process can be held more accurately.

D. Amplifier Gain and Offset Errors

The amplifier used in the proposed DAC can become the performance bottleneck. The maximum DAC accuracy that can be reached is limited by the amplifier's open loop gain. The maximum gain error allowed should always be less than half least significant bit (LSB) value, i.e.,

$$G_{error} = \frac{1}{A_0 \cdot \beta} < \frac{1}{2} LSB \qquad (1)$$

where A_0 is the amplifier DC gain and β is the feedback factor. A more strict condition is justified if we have too many sources of errors in the switching scheme. The overall DAC offset will depend on the amplifier's offset. However, these offset issues can be resolved by the external switched capacitor circuit. In our design, the amplifier is a two-stage telescopic cascode followed by a common source amplifier with source degeneration. AC analysis in Figure 6 shows that we have a DC gain of 101dB which means that the maximum accuracy that can be reached using this amplifier is 16bit.

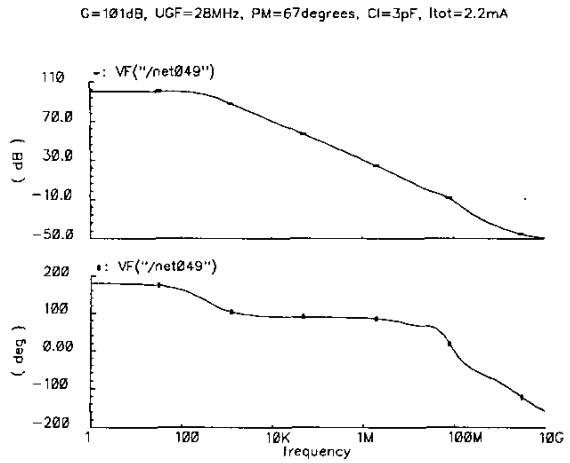

Figure 7 Frequency response of amplifier

The unity gain frequency of the amplifier limits the settling speed thus limiting the conversion speed of the DAC. Higher DC gain can be obtained by using either gain boosting technique or positive feedback technique while higher unity gain frequency can be obtained by dissipating more power in the opamp or by increasing the size of the input transistors. AC analysis shows a unity gain frequency of 27MHz when the amplifier is loaded by a 3pF capacitor drawing a current of 2.2mA.

VI. Simulation Results

The proposed structure was implemented and simulated in the AMI 0.5μ process. The output of the DAC for an eight bit input sequence is shown in Figure 7. As can be seen from the figure, the output converges to the final value without decreasing from its previous output analog value.

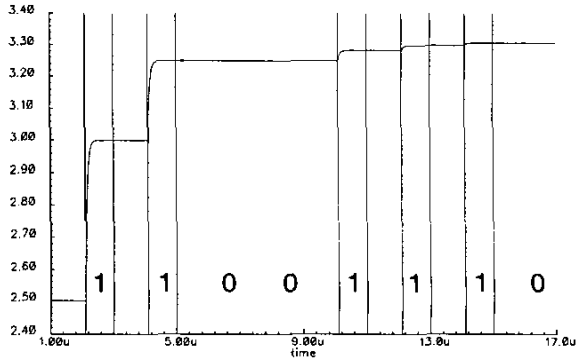

Figure 6: Simulated output for an example

Figure 8 shows the output for a string of 1's as digital input. The inset shows the output to be increasing even as the change in the output becomes small.

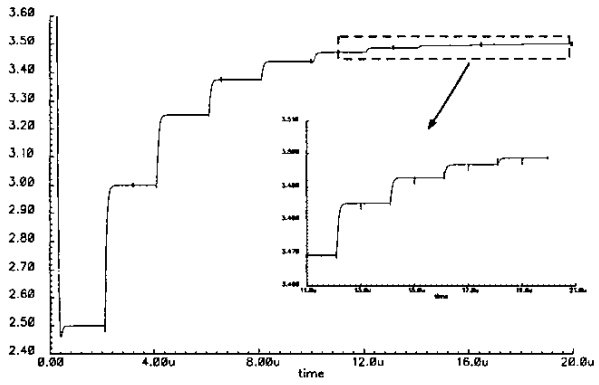

Figure 8: Output for an input of all 1's

CONCLUSIONS

A DAC suitable for applications requiring monotonic operation was presented. Instead of traditional architectures, the conversion starts from MSB and the output voltage is obtained using a switched capacitor integrator. A few of the design issues that can limit the performance of the DAC were discussed. Although the linearity of DAC was not specifically addressed, techniques such as described in [2] and [3] may be used to enhance linearity. Such enhancements as well as the design of the improved DAC incorporating the solutions proposed earlier will be discussed in a future work.

ACKNOWLEDGMENTS

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REFERENCES

[1] R. E. Suarez, P. R. Gray, and D. Hodges, "All-MOS charge redistribution analogue-to-digital conversion techniques – Part II," IEEE J. Solid-State Circuits, 1975, SC-10, pp. 379-385

[2] P. Rombouts and L. Weyten, "Linearity improvement for the switched-capacitor DAC," Electronics Letters, vol. 32, no. 4, pp.293-294, February 1996.

[3] U. K. Moon, G. C. Temes, and J. Steensgaard, "Digital Techniques for Improving the Accuracy of Data Converters," IEEE Communications Magazine, pp. 136-143, October 1999.