where C_j, V_j, F_c and M_j are the model parameters and V_g represents the voltage across the diode. The forward and reverse currents of DCVD and DCVC are chosen to be low to avoid any significant voltage drop across the network. DCW is the junction diode between the charge extraction terminal and n-well with an n-well resistance, RWC, in series. The substrate network is modelled by a diode, DSUB and a series resistance, RSUB. Inductors LPP and LWW, capacitors CPOXP, CPOXW, CPSUBP, and CPSUBW, and resistors RPSUBP and RPSUBW are parasitic elements, existing between electrodes (gate and well) and substrate, which must be considered for the accurate prediction of the high-frequency characteristics of the varactor. The temperature dependence of resistance is modelled by the equation $R(T) = R_{Tnom}[1 + \mathrm{TC1}(T - T_{nom})]$, where T_{nom} is the nominal temperature (27°C).

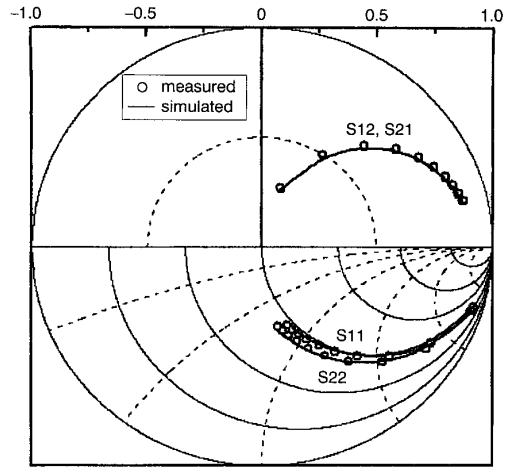

Fig. 3 *Measured and simulated S-parameters for frequency ranges 1 to 10 GHz with $V_g = 2.5$ V and $V_w = 2.5$ V*

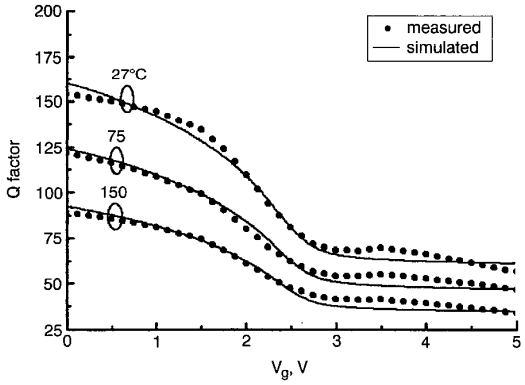

Fig. 4 *Measured and simulated quality factor of MOS varactor for different temperatures 2 GHz*

Results: The varactor model was implemented in the SPICE3 simulator. The model parameter extraction and optimisation was performed from the measured experimental data of the varactor using ICCAP [6]. To extract reliable model parameters it is important that the measurements were performed over a wide range of RF frequency and DC biasing conditions. Two-port S-parameters for the frequency range from 1 to 10 GHz were measured using an HP 8510 network analyser and GSG probes. All DC biases were applied from an HP4142B source measuring unit. During measurement RF signal was applied to the gate in addition to the varying DC voltage (V_g), along with a constant voltage (V_w) to the well. The third terminal was connected to ground by the GSG probes. The circuit parameters were extracted after open and short de-embedding of the probe-pad parasitics. Fig. 2 shows the capacitance and the quality factor extracted from S-parameters measurements at 2 GHz of the MOS varactor with three gate groups at room temperature. In general, the fit is good over the bias ranges. The novel varactor features an outstanding C_{max}/C_{min} ratio of 3.3:1. At 2 GHz the quality factor ranges from 56.2 to 153.5 with an average Q of 96.5. Fig. 3 shows the S-parameters of the MOS varactor for frequency ranges 1 to 10 GHz. The relative mean errors between simulated and measured S-parameters are $E11(\%) = 3.49$, $E21(\%) = 1.79$, $E12(\%) = 1.42$, and $E22(\%) = 2.99$, respectively. It was also found that there is no significant effect of temperature on capacitance behaviour, while the effect on quality factor is noticeable. Fig. 4 shows the quality factor for different temperatures of the MOS varactor at 2 GHz. The simulation results are in good agreement with the experimental results.

Conclusion: An empirical model for a MOS varactor has been proposed, which is valid under different bias conditions and for a frequency range up to 10 GHz. The high temperature behaviour of the MOS varactor has been also modelled. The relative mean error of the S-parameters compared to the measurement are less than 4%. The presented varactor model can be implemented in any SPICE simulator and provides sufficient accuracy for the low-risk design of RFICs.

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Phase detector for PLL-based high-speed data recovery

Yonghui Tang and R.L. Geiger

A new phase detector for high-speed data recovery is introduced. It uses combinational logic circuits along with signals inherently available in multi-stage voltage-controlled oscillators (VCO) or readily derivable from an arbitrary VCO. The resultant stateless phase detector has a very simple architecture and can operate at higher speeds than is achievable with existing state-based phase detectors.

Introduction: Phase-locked loops (PLLs) and data/clock recovery circuits find wide applications in areas such as communications, wireless systems, digital circuits, and disk drive electronics. The phase detector (PD) is a key component of the PLL, but with existing circuit implementations, the phase detector is often the bottleneck that limits the data rates that can be achieved by the PLL.

Many phase detector applications can be partitioned, by function, into two groups. One is used for clock recovery from a degraded or altered clock signal and in this group the PLL locks to a reference clock signal. Many simple phase detectors can be used for this functional group including XOR gates, RS latches etc. The second group is used for recovering a clock from a data sequence. In this functional group, the clock signal is embedded in a non-return-to-zero (NRZ) data stream and the PLL must lock to the NRZ data stream. Since the spectrum of NRZ data has little or no data-dependent energy at its data rate, the task of recovering the clock embedded in the data stream is more difficult and invariably more severe restrictions are placed on the performance of the phase detector. Traditional phase detectors for the latter group include a state machine along with a nonlinear operator at the front end of the phase detector that is used to generate energy at the data rate. The number of different phase detectors in this latter class that have been reported is small and includes those reported in [1–3]. Probably the most widely used phase detectors in this class are based on the Hogge phase detector [2]. As is typical of the state-based phase detectors in this class, the performance of the Hogge phase detector deteriorates rapidly at higher frequencies. These performance limitations are due mainly to the inadequate settling performance of the flip-flop used to form the state machine. The new phase detector introduced in this Letter can be used in PLLs designed to recover high-frequency clocks embedded in pseudo-random NRZ data streams. The simple architecture and the elimination of the state machine contribute to the improved high-frequency performance of this circuit.

Structure: In contrast to existing phase detectors that use a single-phase clock and multi-phased data signals, the new phase detector uses multi-phase clock signals and the actual data sequence to achieve simplicity and high-speed operation. A general structure of the proposed PD is shown in Fig. 1. Multi-phase clock signals ('CLK_d1' and 'CLK_d2') can be generated by delaying the clock signal 'CLK'. When the PLL acquires lock, 'CLK_d1' will phase-lock to 'data_d1'. The operating principles will be explained later.

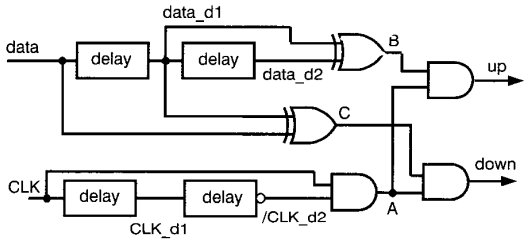

Fig. 1 *General structure of proposed phase detector*

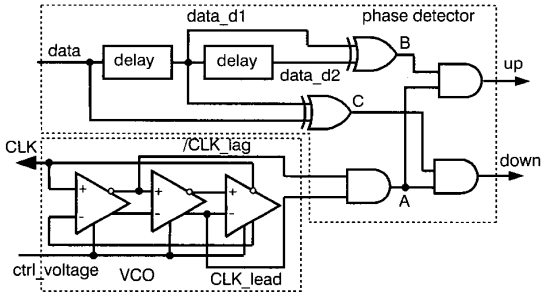

Fig. 2 *Phase detector structure used with ring oscillator with odd-number stages*

In PLLs using ring-oscillator type VCOs, the multi-phase clock signals are inherently available and two delay stages for generating the delayed clock signals are not necessary thus simplifying the structure of the PD. For example, the PD with a 3-stage ring oscillator VCO is shown in Fig. 2. The two signals extracted from the VCO labelled 'CLK_lead' and '/CLK_lag' are the leading and inverting lagging signals of the clock ('CLK') signal. Comparing Fig. 1 and 2, 'CLK_d1' is analogous to 'CLK' of Fig. 2, 'CLK' of Fig. 1 is analogous to 'CLK_lead' and '/CLK_d2' is analogous to '/CLK_lag'. For either the structure of Fig. 1 or Fig. 2, two data delay cells and the two XOR gates are used to detect the edges of transitions in the random input data.

Operation: Fig. 3 shows the timing diagram for a segment of random input data when the PLL is in lock. The circuit aligns the rising edges of 'CLK' with the middle of signal 'A' independent of the data at the input. The falling edges of 'C' and the rising edges of 'B' are aligned at the dotted line which, when the PLL is in lock, are also aligned with the middle of the signal 'A'. The 'up' and 'down' signals are generated by using 'B' and 'C' to partition the 'A' signal into equal width segments at each data transition. Therefore, the 'up' and 'down' signals have the same duty cycles when in lock and the output of the loop filter, which filters the difference in the duty cycles of the 'up' and 'down' signals, will not be driven up or down. The 'up' and 'down' signals are only generated whenever there are transitions in the incoming data stream. This property provides the ability to handle random NRZ data.

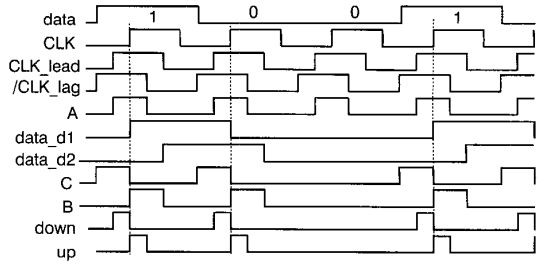

Fig. 3 *Operating principles of phase detector*

When 'data' is leading or lagging the 'CLK', the widths of the 'up' and 'down' pulse will change correspondingly in opposite directions. The changes in the duty cycles of the 'up' and 'down' signals will, in turn, decrease or increase the frequency of the 'CLK' signal through the PLL. Note that when the PLL is in lock, 'CLK' phase-locks to 'data_d1' instead of 'data'.

The accuracy requirements for the delay time of the delay cells in the PD are lax. Proper operation of the proposed PD will be achieved provided the delay cell satisfies the inequality:

$$\max\left(\frac{1}{2}T_0, \frac{1}{2}(T-T_0)\right) < T_{delay} < \min\left(T-\frac{1}{2}T_0, \frac{1}{2}(T+T_0)\right)$$

where T is the period of the signal 'CLK', 'T_0' is the pulse width of the signal 'A', and 'T_{delay}' is the delay time of the delay cell.

Extensions: For any VCO with odd number (3) of stages, the 'CLK_lead' signal can come from the non-inverting output of the stage immediately preceding the clock output stage and the '/CLK_lag' signal can come from the inverting output of the immediately following stage. Other signals can also be used for 'CLK_lead' and '/CLK_lag' when there are more than three delay stages depending on the VCO design.

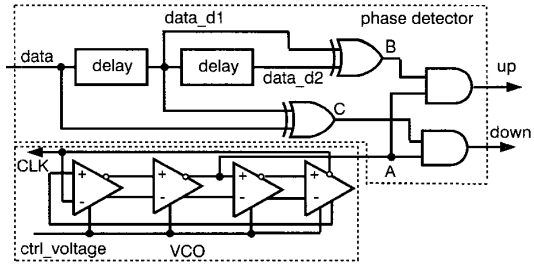

Fig. 4 *Phase detector structure used with ring oscillator with even-number stages*

When the VCO has an even number (≥ 4) of stages, the PD structure becomes even simpler. For example, Fig. 4 shows a 4 stage VCO. In

this case, we can eliminate the AND gate that is used to generate the signal 'A' since the signal 'A' can be directly extracted from the VCO. For more than four delay stages in the VCO, the number and position of the cross-overs must be considered when extracting the 'A' signal.

Implementation and simulation results: A 2.5 Gbit/s PLL [4] for data recovery using the PD/VCO of Fig. 4 along with a charge pump and loop filter was implemented in 0.25 μm CMOS process. HSPICE simulation results show that the PLL can operate at 2.5 GHz over process corners and a 0–100°C temperature range. Total power dissipation is 40 mW with a single 2.5 V power supply.

Conclusions: A simple new non-sequential phase detector structure has been introduced. It is applicable to both clock and random data recovery and offers potential for operating at higher speeds than state-based phase detectors.

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980 nm band pumped Er^{3+}-doped tellurite-based fibre amplifier with low-noise figure of less than 4.5 dB

A. Mori, H. Ono, K. Shikano and M. Shimizu

The amplification characteristics of an Er^{3+}-doped tellurite-based fibre amplifier (EDTFA) with 980 nm band pumping are described. The optimum pump wavelength and length of the newly developed EDTF are investigated in order to obtain both a low noise figure and a high gain simultaneously, and realise a low noise figure of less than 4.5 dB with a pump wavelength of 976.5 nm and a 0.4 m EDTF.

Introduction: The Er^{3+}-doped tellurite-based fibre amplifier (EDTFA) is a promising candidate with which to construct simple and high-capacity wavelength division multiplexing (WDM) networks. This is because the EDTFA provides a wide and seamless gain bandwidth that includes the C- and L-bands with a medium population inversion [1–3], or the L-band with a low population inversion [4, 5]. Successes in several terabit/s transmission experiments have confirmed that the EDTFA is effective in simplifying high-capacity WDM systems [6–8]. However, one technical problem in relation to the EDTFA has been that the noise figure in the C-band wavelength region with 1480 nm band pumping is higher than that of a 980 nm pumped Er^{3+}-doped silica fibre amplifier (EDSFA). The highest phonon energy of tellurite-based glasses is lower than that of silicate glasses and so the lifetime of the 980 nm pump level of Er^{3+} in tellurite-based glasses is longer than that in silicate glasses [9]. Therefore, a 980 nm pumped EDTFA that operates with low-noise and high-gain has not yet been realised, and EDTFA amplification characteristics have been studied by using 1480 nm pumping. Two reports on EDTFAs have shown that 980 nm level pumping cannot provide a high gain coefficient or a low noise figure [10, 11]. This is because their EDTFs did not provide a low loss when a high phonon energy glass was used as the 980 nm pumped host. Recently, by developing new tellurite-based host compositions, we successfully fabricated low loss EDTFs with a shorter lifetime of the 980 nm pumping level.

This letter describes the amplification characteristics of an EDTFA with 980 nm band pumping. By optimising the pump wavelength and the length of the newly developed EDTF to obtain both a low noise figure and a high gain simultaneously, we were able to realise a noise figure of less than 4.5 dB.

Experiment: Fig. 1 shows a schematic diagram of our EDTFA, which consists of a single stage and a single pass configuration. The EDTF was doped with Er ions at 2000 ppm, and its cutoff wavelength and refractive index difference were 1.3 μm and 0.73%, respectively. The EDTF loss was 0.9 dB/m at 1230 nm. We obtained a stable tilt splice with a loss of 0.3 dB and a reflection of −55 dB between the EDTF and a silica fibre by using the V-groove connection technique. We installed WDM hybrid-type isolators in front of and behind the EDTF. The EDTF was forward pumped by a Ti:sapphire laser to investigate the pump wavelength dependence of the EDTFA, or a 976.5 nm laser diode to study the EDTF length and the input signal power dependences of the EDTFA. The pump power was 100 mW for all the measurements. The noise figure was defined for the whole amplifier including the WDM hybrid-type isolator. We measured the absorption spectrum of the Er^{3+}-doped core glass with a UV-visible-NIR double beam spectrophotometer.

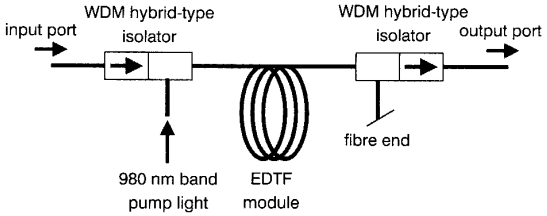

Fig. 1 *Schematic diagram of 980 nm band pumped EDTFA*

Results and discussion: Fig. 2 shows the pump wavelength dependence of the amplification characteristics and the absorption spectrum of the Er^{3+} $^4I_{11/2}$ level in the tellurite-based core glass. As regards the pump wavelength dependence, we measured the changes in the gain and noise figure for pump wavelengths of 970 to 1000 nm. The signal wavelength and the input signal power were 1534 nm and −35 dBm, respectively. The EDTF was 0.4 m long. We obtained a gain of over 25 dB and a noise figure of less than 4 dB for pump wavelengths of 970–983 nm. Taking account of the fact that the insertion losses of the WDM hybrid-type isolator and the EDTF module were about 0.5 and 0.3 dB, respectively, we achieved a low noise figure near the quantum limit of 3 dB, as obtained with a 980 nm pumped EDSFA. In comparison with the absorption spectrum, the signal gain peak corresponds to the absorption peak at 976 nm.

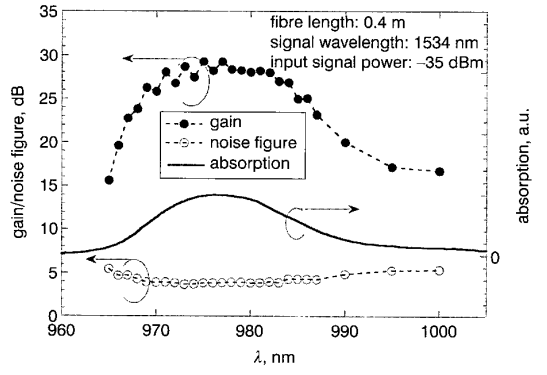

Fig. 2 *Pump wavelength dependence of amplification characteristics and absorption spectrum of Er^{3+} $^4I_{11/2}$ level in tellurite-based core glass*