7.2 A 1.5V 14b 100MS/s Self-Calibrated DAC

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Current-steering DACs used in high-speed telecommunication applications require good static and dynamic linearity. In the frequency domain, inaccurate static values and nonlinear switching transients both introduce harmonics that are the major factors limiting the SFDR. To overcome random mismatch and gradient errors, reported current source arrays are usually laid out in a large dimensional matrix with complex routing [1]. This has resulted in large parasitic capacitances and hence slows settling causing the SFDR to drop rapidly as the sampling and/or signal frequency increase.

Proper calibration can dramatically reduce the area of the current source array and hence the parasitic capacitances. A small array exhibits reduced gradient effects, relaxing requirements on layout. Calibration also reduces sensitivities to process, temperature and aging, thus providing high yields.

As processes keep shrinking in favor of digital circuits, so does the supply voltage. This introduces more challenges for high-performance DAC design. For example, the significant reduction of the effective gate-source voltages severely deteriorates the matching and noise immunity of current sources. Low supply voltages also make it impractical to use cascode current sources. In these cases, calibration becomes even more attractive. Since most conventional calibration methods are not suitable for very-low-voltage operation [2-3], a new foreground digital calibration scheme is used in this design to implement a 14-bit 100MS/s DAC in a 1.5V 0.13μm fully digital CMOS process.

The 14-bit DAC array is segmented into a 6-bit thermometer-decoded MSB array, a 4-bit thermometer decoded Upper LSB (ULSB) array and a 4-bit binary-weighted Lower LSB (LLSB) array. The MSB array will be calibrated while the 8-bit LSB (ULSB and LLSB) array needs only to maintain 9-bit accuracy.

A block diagram of the MSB array calibration is shown in Fig. 7.2.1. First, the inputs of the MSB array are all set to "0", and the inputs of the LSB array (including a dummy unit current source) are all set to "1". The differential output of the DAC is measured by a slow but accurate (16-bit) calibration ADC (CALADC). The result is denoted as D_{LSB}. Subsequently, the inputs of the LSB array are all set to "0", while the inputs of the MSB array are increased by 1 in each calibration cycle. Ideally, in the jth ($1 \le j \le 63$) calibration cycle (MSB = j), the output of the DAC, after digitized by the CALADC, is equal to $j \bullet D_{LSB}$. If not, the error is stored in word j of a SRAM, which will be addressed in the conversion mode by the MSB inputs of the DAC. The error code drives an 8-bit calibration DAC (CALDAC) whose current outputs are summed with those of the main DAC. The input swing of the CALADC is set slightly larger than the output swing of the DAC to avoid overflow. To compensate for the gain mismatch between the CALADC and the DAC, the error of the MSB code is determined by a successive approximation process utilizing the CALDAC during each calibration cycle. Since the outputs of the CALDAC are differential, tuning can be done in both directions.

This calibration algorithm is subject to "gain error accumulation". A small amount of deviation of D_{LSB} from its ideal value will be accumulated during the calibration as the MSB code increases. If uncorrected, it will require a large tuning range for the CALDAC. This problem is solved by a bias adjustment undertaken before the MSB array calibration. The goal is to tune the bias voltage of the LSB array so that D_{LSB} is equal to $1/2^6$ of the DAC full scale. The bias generator (Fig. 7.2.2) provides two bias voltages: one is fixed bias for the MSB array while the other is tunable driving the LSB array and the CALDAC. The tuning is accomplished through another successive approximation process employing a 6-bit DAC embedded in the bias generator.

The segmentation and matching accuracy of the current source arrays as well as the resolution and accuracy of the CALADC, the CALDAC, and the bias generator were optimized through careful statistical analysis and Monte-Carlo simulations. As a result, the total gate area of the current sources is reduced by over a factor of 500 compared to a DAC designed for the same static performance and yield without calibration.

Each current cell contains a single-transistor current source and a pair of switches controlled by a latch and switch driver. As the main goal of this prototype is to demonstrate the calibration concept, the CALADC was implemented off-chip using a commercial 16-bit ΣΔ ADC. Since the CALADC converts only DC signals, it can be implemented on-chip using a low-order ΣΔ modulator with a high oversampling ratio. We anticipate that in the 0.13μm process, the area of the modulator will not be larger than that required for the current cell array.

The floor plan of the current cell array is shown in Fig. 7.2.3 where all current sources are placed at the center being surrounded by the switches, latches and decoders. This arrangement minimizes the interconnections between the current sources and their switches, which is essential for improving the settling of the DAC. Since the LSB array is uncalibrated, it is placed in the middle of the array to minimize the gradient effects. The MSB array to be calibrated is partitioned into two rows being placed on the top and the bottom of the LSB array.

The measured static linearity of the DAC is shown in Fig. 7.2.4. Before calibration, the DAC has 9~10 bits of linearity and the major errors are from the MSB array. After calibration, both the INL and the DNL are below 0.5LSB at the 14b level. The SFDR at 100MS/s is plotted in Fig. 7.2.5. As the signal frequency increases, the SFDR of this design drops much slower than the previous designs [1,4], except that reported in [2] where return-to-zero technique was used to reduce the transition nonlinearity at the cost of halving the signal power. This technique can also be used in this design to further improve the SFDR. The figure also shows that for a given SFDR, the proposed structure offers a dramatic reduction in both power and die area. The active area of the DAC is only $0.1mm^2$. At 100MS/s, for a signal near the Nyquist rate, the power dissipation is only 16.7mW. More characteristics of the DAC are given in Fig. 7.2.6. The chip micrograph is shown in Fig. 7.2.7.

Acknowledgements

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References

[1] G. Van der Plas et al., "A 14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1708-1718, Dec. 1999.

[2] A. Bugeja et al., "A Self-Trimming 14-b 100MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1841-1852, Dec. 2000.

[3] D. Groeneveld, et al., "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," *IEEE J. Solid-state Circuits*, vol. 24, pp. 1517-1522, Dec. 1989.

[4] M. Tiilikainen, "A 14-bit 1.8-V 20-mW $1mm^2$ CMOS DAC," *IEEE J. Solid-state Circuits*, vol. 36, pp. 1144-1147, July 2001.

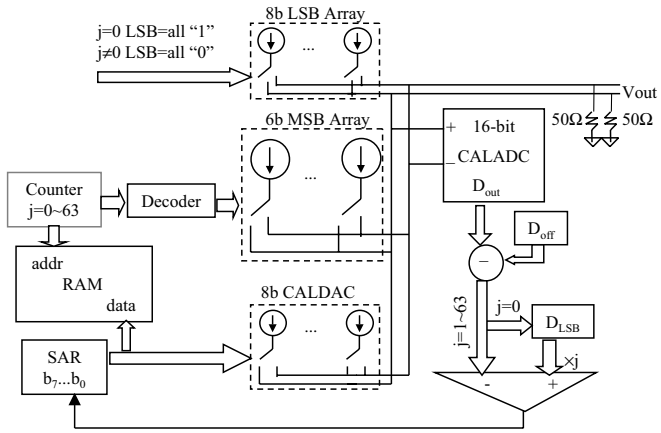

Figure 7.2.1: Block diagram of MSB array calibration.

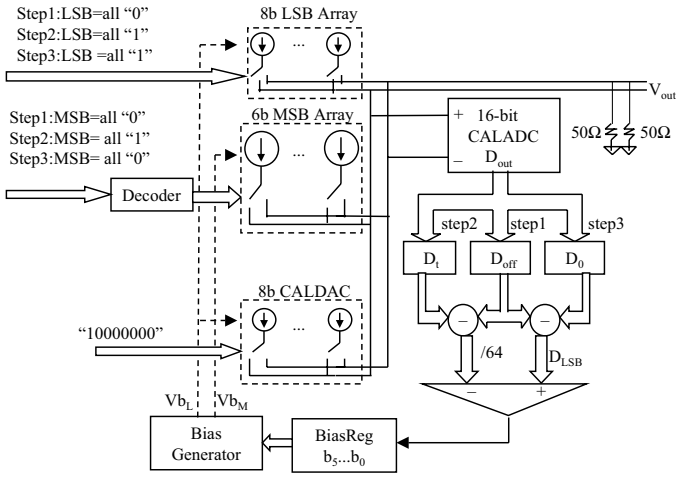

Figure 7.2.2: Block diagram of bias calibration.

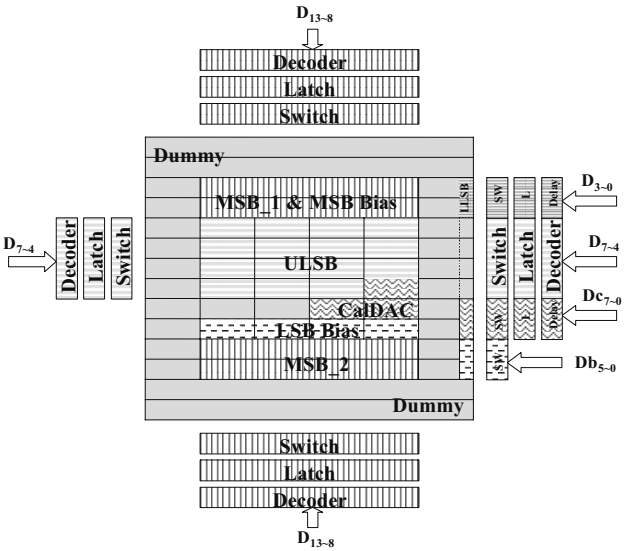

Figure 7.2.3: Floor plan of current cell array.

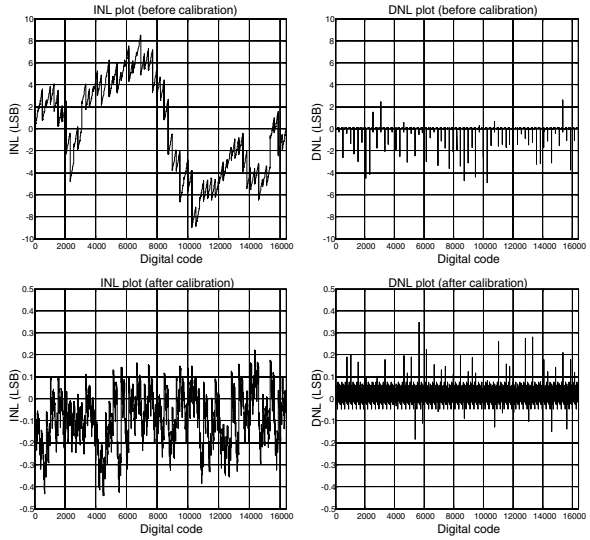

Figure 7.2.4: Static linearity.

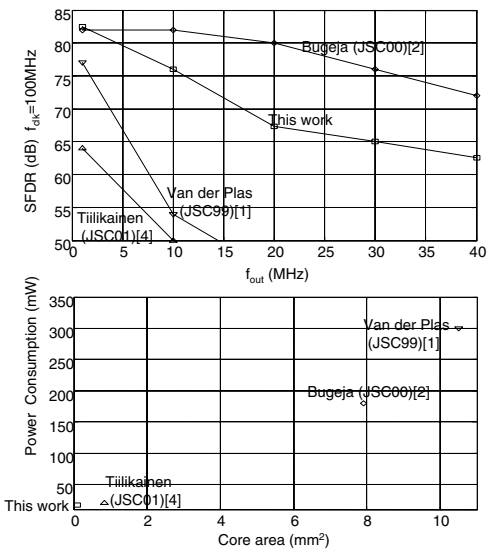

Figure 7.2.5: Comparison to the prior arts.

Resolution	14 bits
Maximum Sampling Rate	180MHz
Full-Scale Current	10mA
Maximum Output Swing	0.5V (single-ended) and 1V (differential)
Supply Voltage	1.5V (nominal) 1.25V (minimum)
INL	9LSB (before) 0.43LSB (after)
DNL	5LSB (before) 0.34LSB(after)
Single-Tone SFDR at f_{clk}=50MHz	64dB(before) 83dB(after) at f_{out}= 0.45MHz
	59dB(before) 64dB(after) at f_{out}=21 MHz
Single-Tone SFDR at f_{clk}=100MHz	63dB(before) 82dB (after) at f_{out}= 0.9MHz
	56dB(before) 62dB(after) at f_{out}=42 MHz
Single-Tone SFDR at f_{clk}=150MHz	61dB(before) 81dB(after) at f_{out}=1.4 MHz
	47dB(before) 50dB(after) at f_{out}=63 MHz
Two-Tone SFDR at f_{clk}=100MHz	66dB(after) at f_{out1}=23.5 MHz, f_{out2}=24.5 MHz
Power Dissipation in 1.5V Supply	16.7mW at f_{clk}= 100MHz, f_{out}=42MHz
Active Area	0.1mm^2 in 0.13μm CMOS process

Figure 7.2.6: Performance summary.

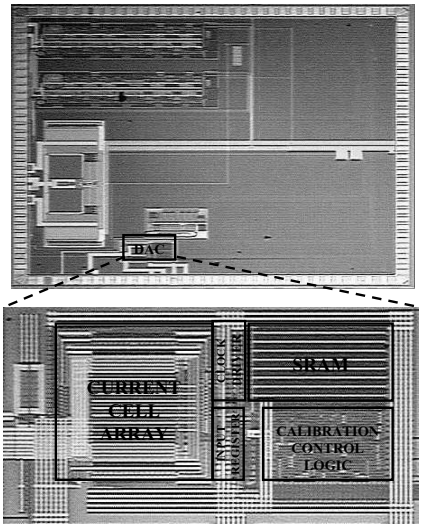

Figure 7.2.7: Chip micrograph.

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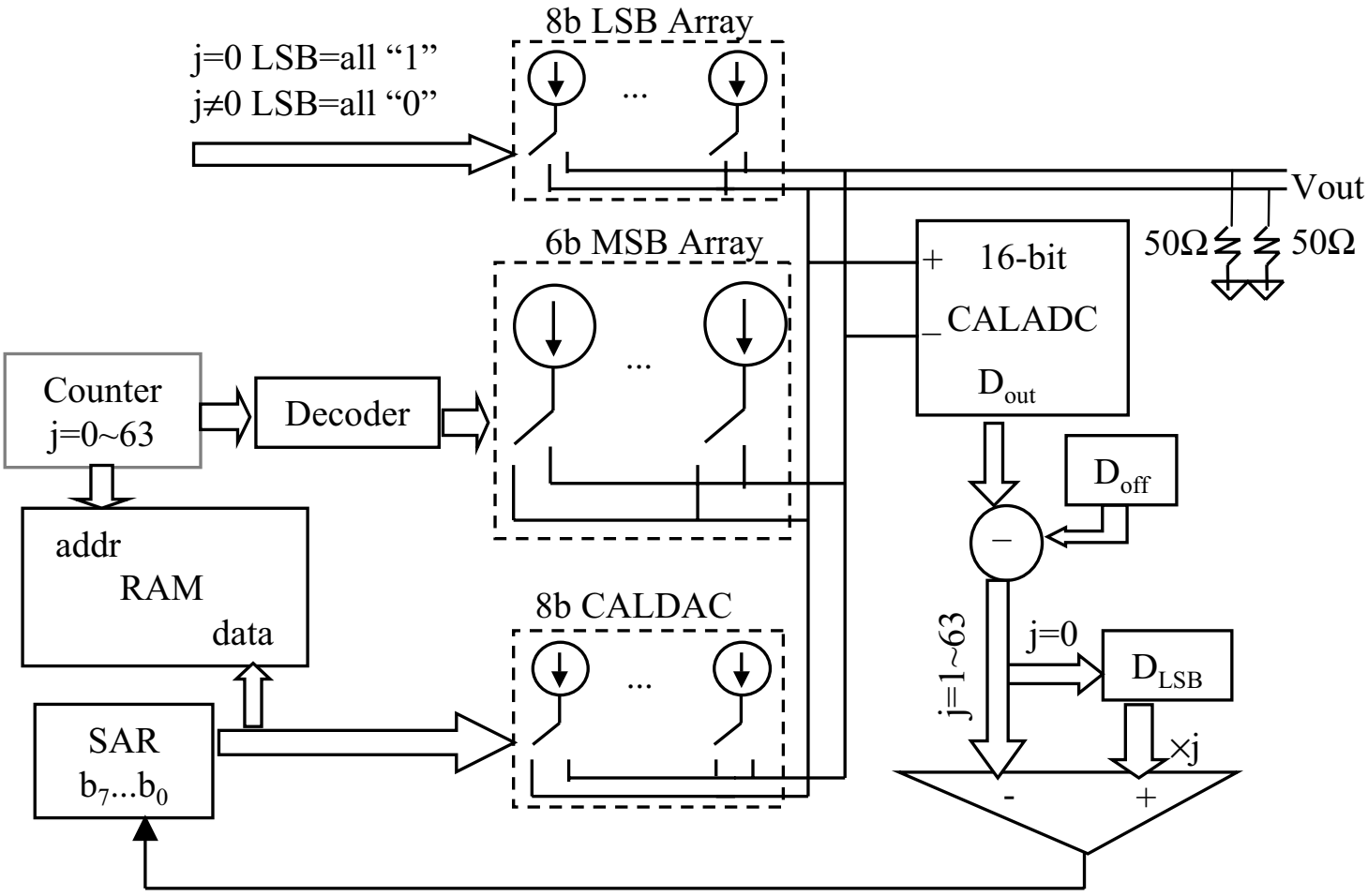

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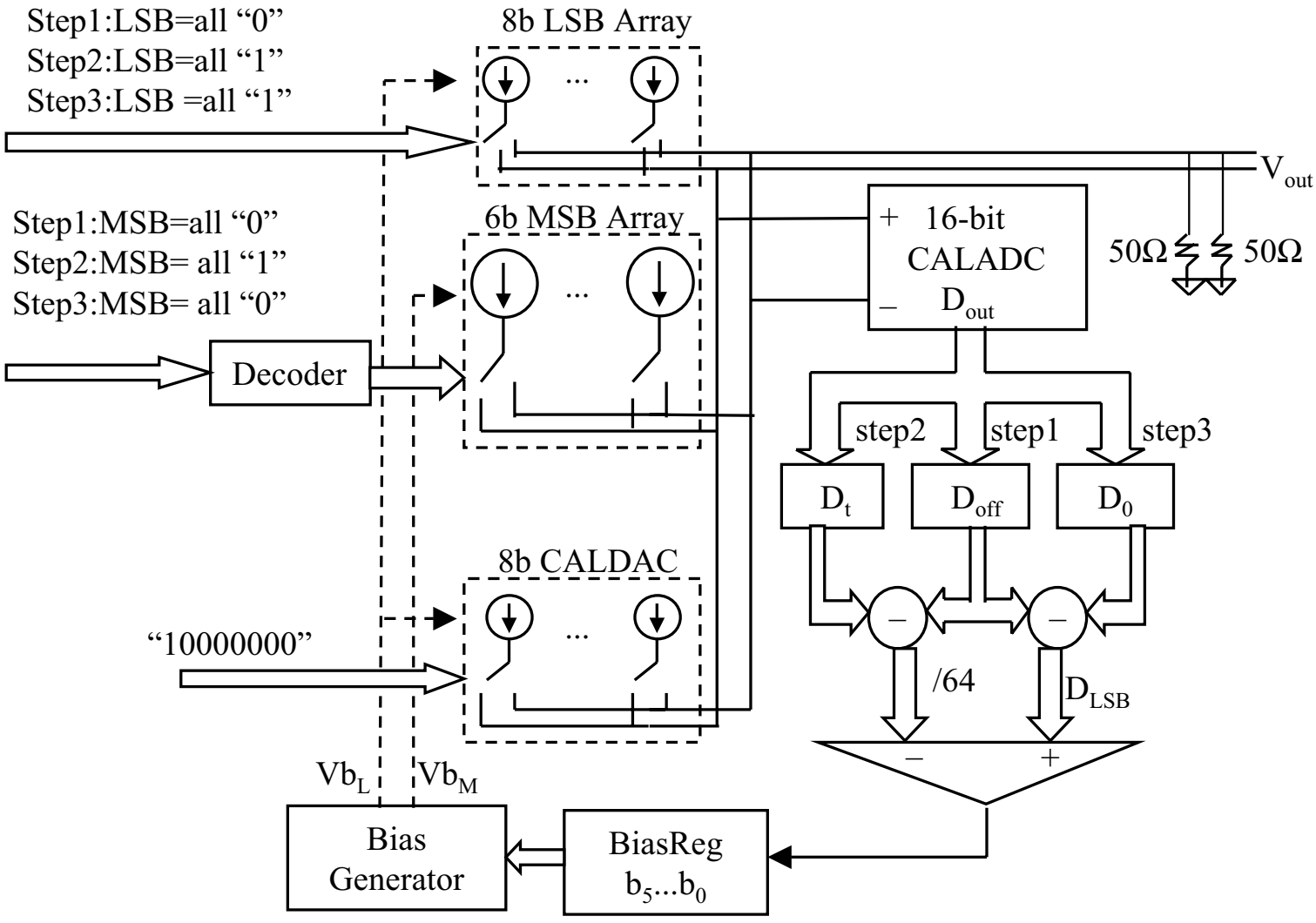
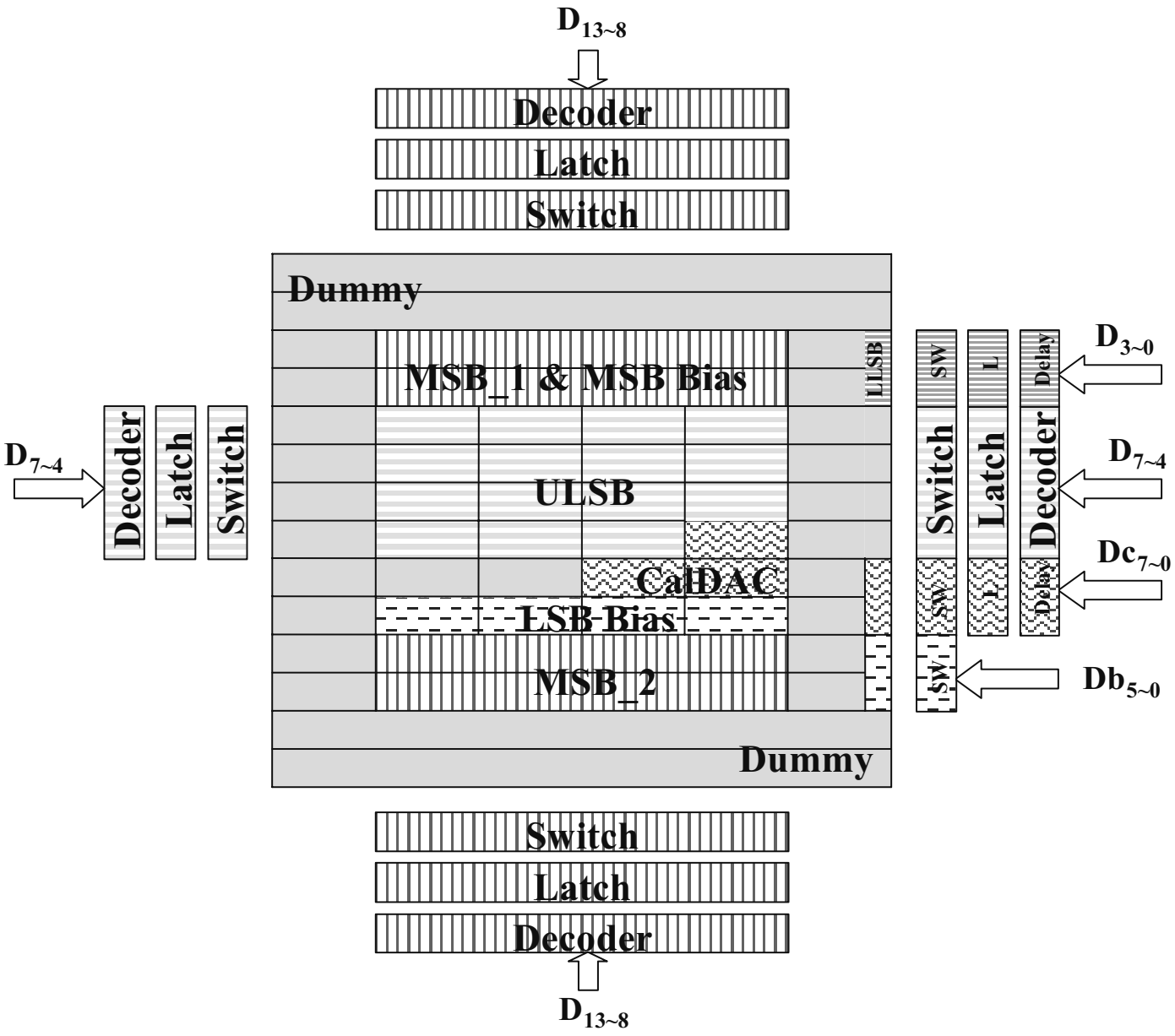


Figure 7.2.2: Block diagram of bias calibration.



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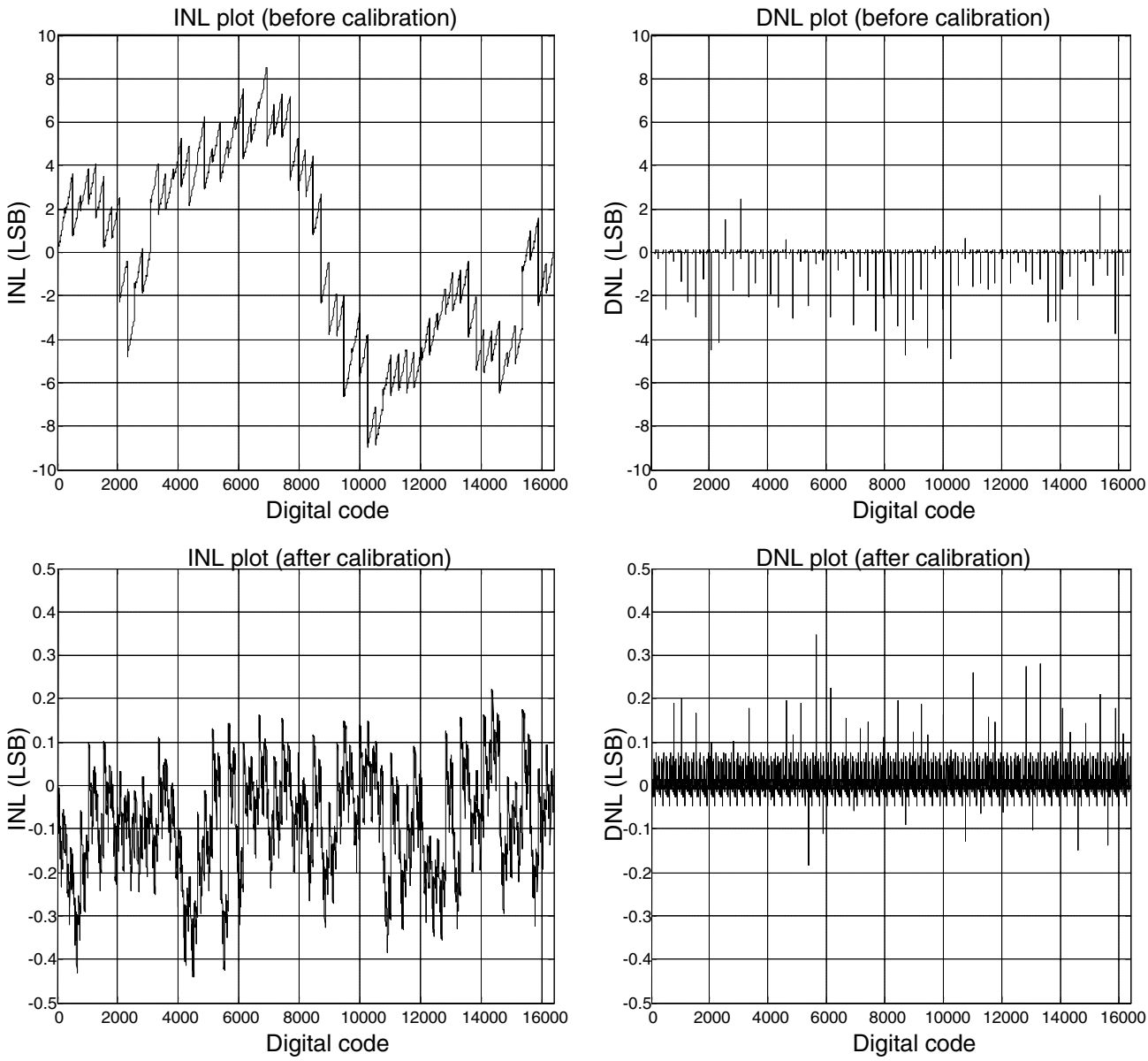
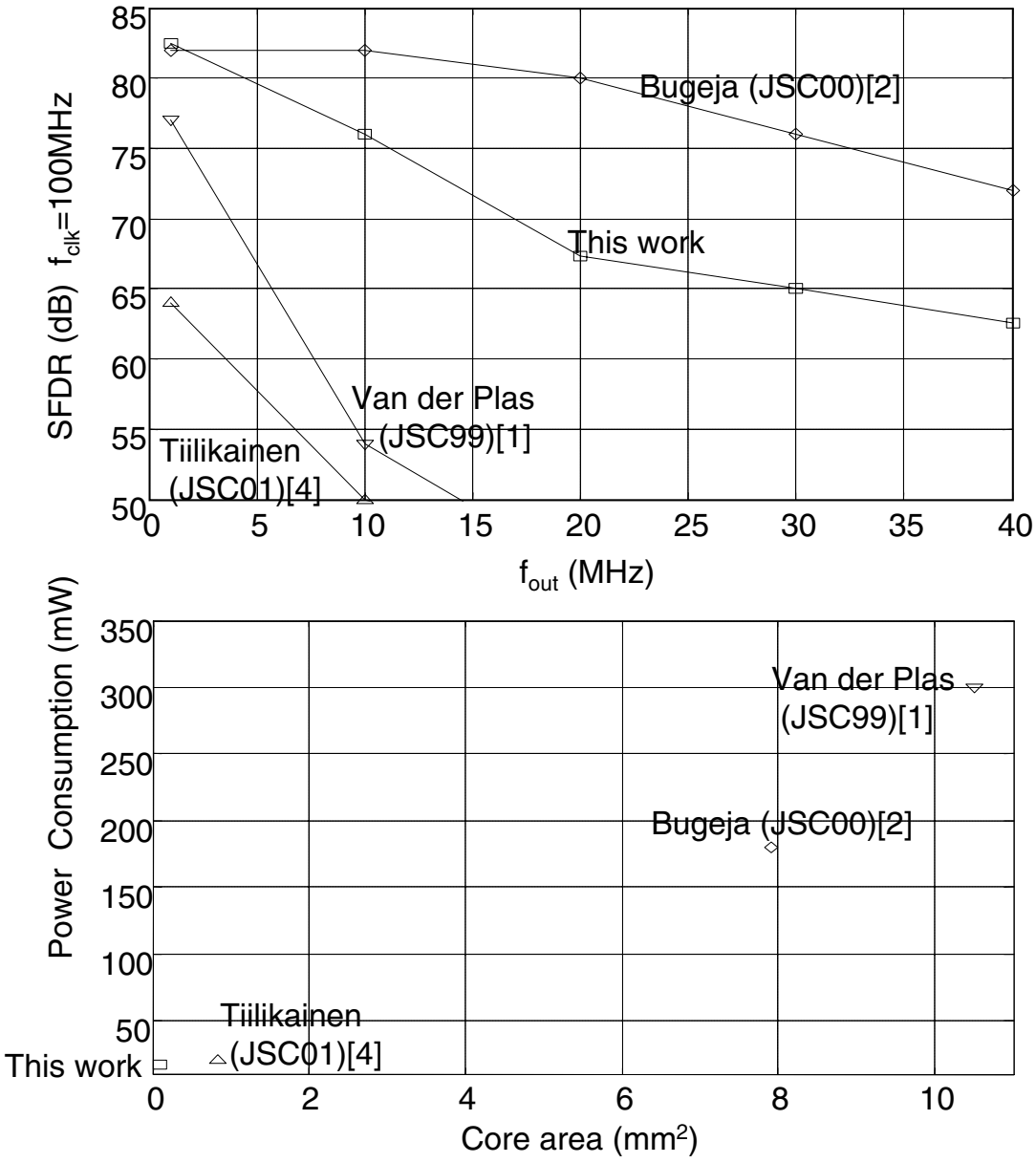


Figure 7.2.4: Static linearity.



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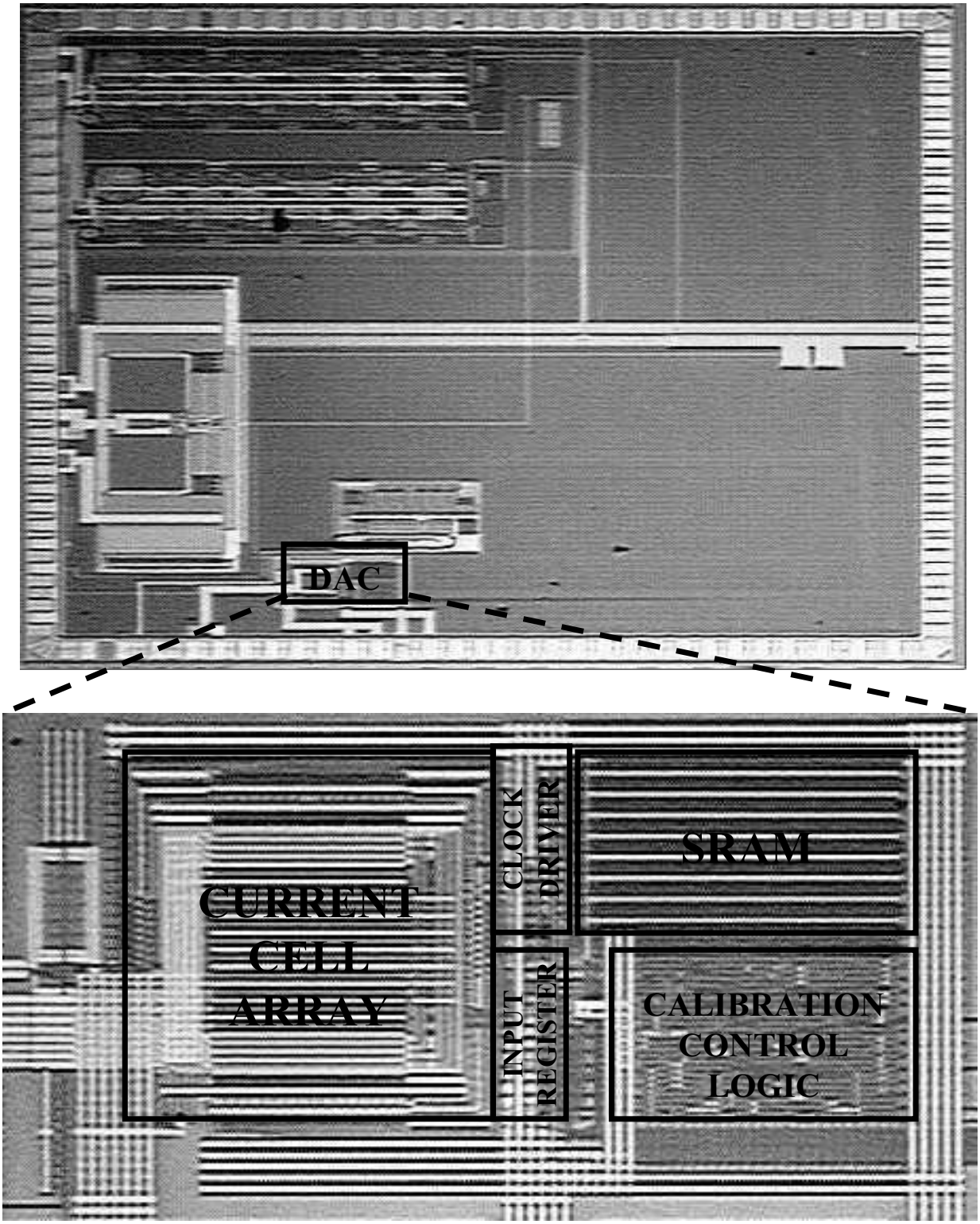

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