A DETERMINISTIC DYNAMIC ELEMENT MATCHING APPROACH TO ADC TESTING

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ABSTRACT

A deterministic dynamic element matching (DEM) approach to ADC testing is introduced and compared with a common random DEM method. With both approaches, a highly non-ideal DAC is used to generate an excitation for a DUT that has linearity that far exceeds that of the test stimulus. Simulation results show that both methods can be used for testing of ADCs but with a substantial reduction in the number of samples required for the deterministic DEM method. This technique of using an imprecise excitation to test an accurate ADC offers potential for use in both production test and BIST environments.

1. INTRODUCTION

The conventional approach to testing analog-to-digital converters (ADCs) is a non-trivial task when following the conventional wisdom that a very accurate input is needed. This input is typically generated by a digital-to-analog converter (DAC) with substantially higher resolution than the device under test (DUT). Following this approach in a Built-In Self-Test (BIST) environment, the real challenge is in designing the circuit to test the part since it needs to have substantially higher resolution and linearity than the DUT. In a BIST application, the high performance requirement of DAC often translates into an expectation that the DAC needs more silicon area than the ADC to be tested.

It has been demonstrated that dynamic element matching (DEM) can be used to generate analog signals with high "average" SFDR using moderately low-linearity digital-to-analog converters [1]. This is because the randomizing effect of DEM spreads the errors in the DAC over a wide spectrum so that higher SFDR becomes possible. In [1], it was specifically shown that, in a DAC with static errors, performance can be improved using random DEM. This characteristic of the dynamic element matching technique makes it a suitable candidate for generating the input of a DUT using a not-so-accurate DAC, and hence without the need of large silicon area and careful design of the test signal generator. A test strategy was recently introduced to use random DEM in a highly-nonlinear DAC to test high-resolution ADCs [2]. This work focuses on introducing the deterministic DEM testing technique and comparing it with the random DEM testing approach when a low accuracy DAC is used to characterize/test an ADC with higher linearity.

In the proposed schemes, the DAC will have nominally more bits of resolution than the ADC but it is not ideal due to large static errors caused by mismatch. Static mismatch errors can be caused by process variations and result in a nonlinear transfer curve in the DAC as characterized by the integral nonlinearity (INL). Although any number of ADC performance parameters may be characterized, in this work we will restrict the focus to INL performance with both proposed testing schemes.

This paper is organized as follows. An explanation of how the ADC is implemented and how the INL is calculated is given in Section 2. The dynamic element matching method is explained in Section 3. Details are presented in Section 3 about both the random and deterministic DEM implementations of the DAC, while in Section 5 simulation results are shown and discussed.

2. ADC MODEL AND INL CALCULATION

To test both methods, a flash ADC is characterized through the INL measurement as in [2]. A simple implementation of a flash ADC is shown in Figure 1.

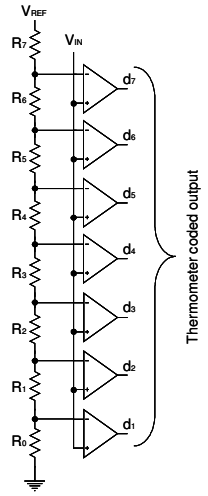

Figure 1: A 3-bit flash ADC.

The input signal to a flash converter is fed to the comparators in parallel. Each comparator is also connected to a resistor string, as shown in Figure 1. The output of the comparator is set to one if the input value is bigger than the voltage at the respective node of the resistor string, otherwise it is set to zero. The output code obtained is called a thermometer code. Resistor mismatches and comparator errors are the two primary sources of static errors in the ADC. However, since this paper focuses on INL and comparator

errors do not accumulate into large INL, only the static error caused by resistor mismatches is modeled.

There are several alternative but similar definitions of the INL of an ADC. The endpoint fit line method is used for this work. In this definition, the INL, as given in (1), is defined to be the maximum deviation of the ADC's transfer curve from the endpoint fit line, $V_{FITLINE}$. With this definition, the INL of an ideal ADC is 0.5 LSB.

$$INL = \max\left(\left|\frac{V_o - V_{FITLINE}}{V_{LSB}}\right|\right) \quad (1)$$

An example of a non-ideal ADC transfer curve and its corresponding fit line are shown in Figure 2. It is a 3-bit flash ADC with a voltage reference equal to 2V.

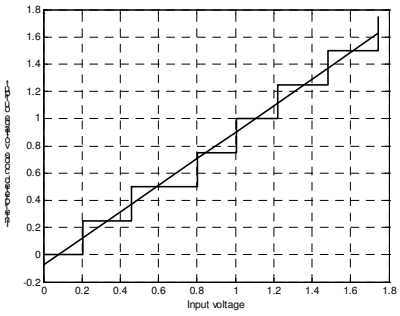

Figure 2: A non-ideal ADC transfer curve and its endpoint fit line.

As can be seen in Figure 2, the INL has local maximum values at the transition points when the output changes from one code to the next one. These are the points that need to be measured for characterizing the ADC under test.

3. DYNAMIC ELEMENT MATCHING

Element matching errors are inevitable due to inherent process variations. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The dynamic element matching technique accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average all element values are nearly equal. If the mismatched components are rearranged properly, the errors caused by them can be reduced or eliminated in some applications.

Existing DEM structures are used in real-time circuits making it difficult to fully exploit DEM potential since in short time intervals the mismatch still substantially degrades performance. Our approach is different since the DEM is not in the DUT but in the signal generator used to test it, eliminating the real-time concern when using DEM.

4. A DAC WITH DYNAMIC ELEMENT MATCHING

In order to construct a DAC with dynamic element matching, two different approaches can be found in the literature [1-3]. One is the partial randomization DEM. The other is the so-called full randomization DEM. This latter technique is one of the two techniques used in this work and will be explained next along with some modifications as seen in [2].

The full randomization DEM will be explained using a 3-bit current steering thermometer-coded DAC as an example as shown in Figure 3.

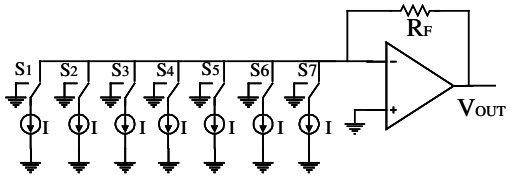

Figure 3: A 3-bit current mode thermometer-coded DAC.

In this case, when all switches are connected to ground, the output corresponds to the digital word zero. To generate the output voltage for the digital one, one switch needs to be connected to the inverting input of the operational amplifier (op amp). If the resistors and switches are matched, for a digital "k", any k of the switches needs to be connected to the inverting input. The resistor R_F is picked so that when all of the currents sources are on, the voltage output is at the desired maximum expected. The dynamic element matching idea for generating an output for a digital word "k" is to pick the switch location of k switches randomly each time an output corresponding to k is desired and then turn on these k switches. In this way, the average output error for any k behaves as white noise uncorrelated with the input digital word [3]

Our approach uses this technique but also takes advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static viewpoint. Since the output of the DAC is used as the input of the ADC, the same digital word, using different randomly chosen current sources, is going to be input to the ADC more than once. The ADC's output for each one of them is then stored for calculating the INL later. In this way, the real-time limitations are eliminated, and an arbitrarily accurate average input signal can be generated.

The second method implemented for this work picks the current sources to be switched deterministically. The pattern used attempts to distribute the sources to be switched on in a way that all sources are used uniformly. In this case, as in the first approach, the same input code is used more than once and the output results are stored for INL calculation. The INL is calculated using the average value obtained for that particular transition point of the DAC that is input to the ADC. Since each individual value was generated using a different combination of current sources, the average may be more accurate and may compensate for part of the mismatch. It can be shown that this approach can also yield arbitrarily accurate input linearity for some deterministic selection sequences.

5. SIMULATION RESULTS

To verify our approach, we simulated flash ADCs with resistor mismatch. These ADCs were tested using a simulated current mode thermometer-coded DAC with static error mismatch in the current sources. The mismatch ratio for the ADC resistors and the DAC current sources both had a Gaussian distribution with a standard deviation of 0.2 and a mean value of 1. The simulated ADCs and DACs had 7 and 10 bits of resolution respectively.

5.1 No Calibration of DACs

As a baseline, the testing of one ADC from our sample of 100 was selected and tested with 100 DACs. The sample ADC had an INL of 2.9LSB. The results are shown in Fig. 4. As expected, the high level of nonlinearity in the DACs caused a large error in testing of the ADC with a worst case error of 1.293 LSB and an average error of 0.524 LSB.

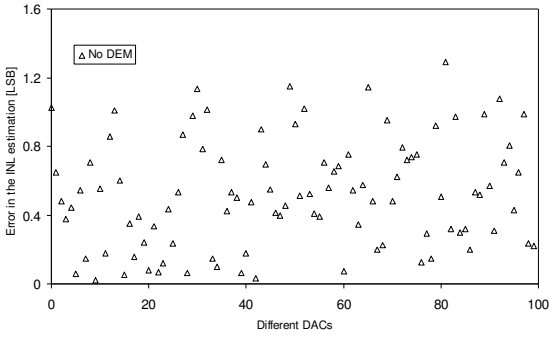

Figure 4: Error in the estimation of the INL of a given ADC for 100 different DACs without DEM.

5.2 Random DEM testing

In this test, one of the ADCs was selected and random DEM of the current sources in the DAC was used for testing the ADC. The test ADC had an INL of 2.9LSB. Each DAC has 1023 current sources. For each DAC the current sources were picked randomly following the DEM approach and each digital word was input to the ADC (with different random current source configurations) P times. The INL of the ADC was calculated and then compared to the actual INL of the ADC. In the simulation, the actual ADC INL was known since we know the transfer characteristics of the ADC. For every DAC, an INL error was calculated using the difference between the actual ADC INL and that estimated using the DEM approach. In Figure 5 the error in the calculation of the INL using 100 different 10-bit DACs is shown. In this set, the worst case INL of the DACs was 10.056 LSB at the 10-bit level. It can be seen that the random DEM algorithm estimated the INL of the 7-bit ADC to within 0.454 LSB in all 100 runs with P=8 random current source samples for each input code and to within 0.142 LSB with P=128 random current source samples.

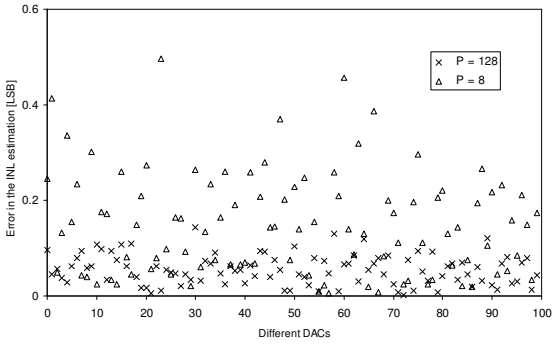

Figure 5: Error in the estimation of the INL of a given ADC for 100 different DACs using random DEM.

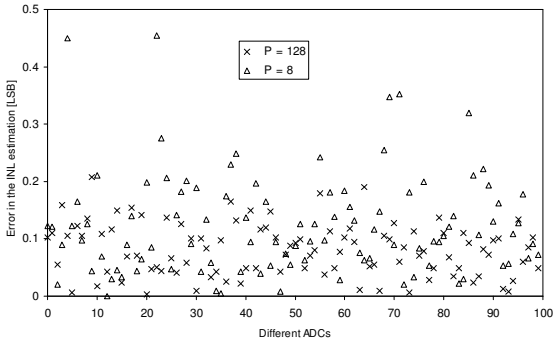

Figure 6: Error in the estimation of the INL of 100 different ADCs for a given DAC using random DEM.

In an attempt to assess the robustness of the algorithm, we then selected one DAC, the one with a worst-case INL of 10.056 LSB and used it to test the 100 ADCs that had INLs which ranged from 1.3 LSB to 4.3 LSB. The results are shown in Figure 6. As can be seen in both figures, when P equals 128, the error in both cases is less than 0.207 LSB, while for P equal to 8 the error is under 0.495 LSB. This can be contrasted to the P equals 1 case, i.e. no DEM, where the error was as high as 1.293 LSB in these 100 samples. It should be noted that the DAC with an INL of 10.056 LSB at the 10-bit level corresponds to an INL at the 7-bit level of 1.3 LSB. Thus, an excitation that has a nonlinearity of 1.3 LSB can be used to measure the INL of an ADC at a substantially higher resolution level.

5.3 Deterministic DEM testing

In the deterministic DEM approach, the current sources are picked in a deterministic way to create the input words to the ADC. The deterministic selection was based solely on position of the current sources and not on the particular mismatch characteristics of a given DAC. Due to space limitations, details about how the current sources were spatially selected will not be given in this paper. Again each word was input P times, each with different configurations of the current sources. Results are shown in Figure 7 for the single ADC with a 2.9 bit INL and 100 DACs and in Figure 8 for the single DAC with 10.056 LSB INL and the 100 ADCs. The DACs and the ADCs were the same as used in the random DEM testing.

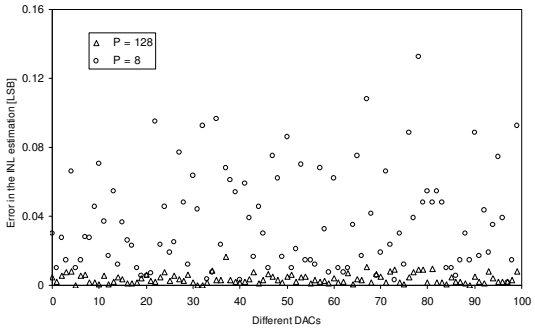

Figure 7: Error in the estimation of the INL of a given ADC for 100 different DACs using deterministic DEM.

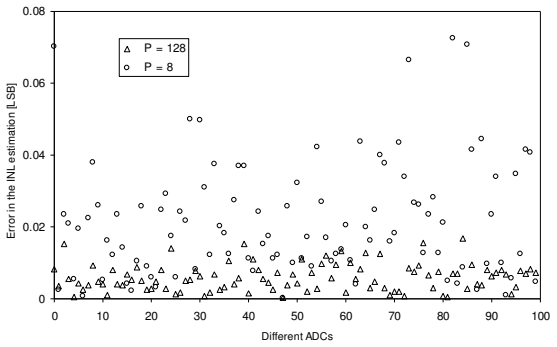

Figure 8: Error in the estimation of the INL of 100 different ADCs for a given DAC using deterministic DEM.

We see in these figures that the performance of this approach is significantly better than that obtained using randomly picked current sources in the DAC. The error is less than 0.017 LSB for all 100 DACs when P equals 128 and less than 0.132 LSB for P equals 8. Correspondingly, the error was 0.017 LSB when P equals 128 for the 100 ADCs and 0.072 LSB when P equals 8 for the same ADCs.

5.4 Comparison of random and deterministic DEM testing

A direct comparison of the random and deterministic DEM testing of the 100 ADCs was also made. In Figure 9 we compare the performance of estimating the INL for P=128 and in Fig. 10 for P=8. In these comparisons, the same DAC used in the previous sections with an INL of 10.056 LSB was used.

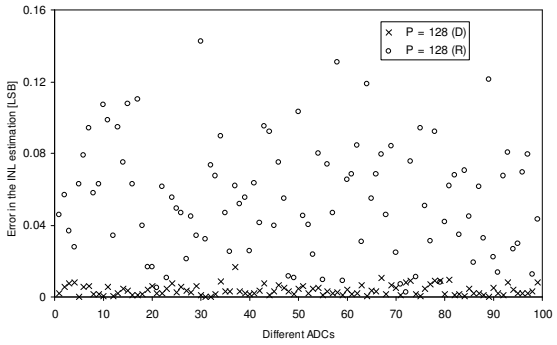

Figure 9: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 128.

From these figures, two important observations can be made. The deterministic DEM method offers substantial improvements in performance over that of the random DEM approach for a given number of samples. Second, it can be seen that the performance of the deterministic DEM approach with P equals 8 is comparable to that of the random DEM approach with P equals 128. This latter result is important, since substantially less testing time is needed which should be of particular benefit in a production test environment.

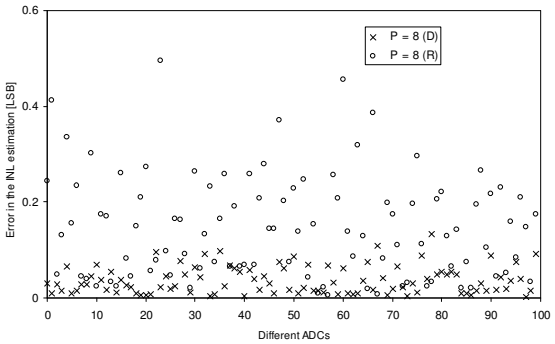

Figure 10: Comparison of the two methods for estimating INL error using 100 different ADCs and P equals 8.

Whether the specific spatial current source selection algorithm used for the deterministic DEM approach in these simulations is optimal or not has not been studied but even in its present form it offers substantial improvements over what is attainable with the random DEM approach.

6. SUMMARY

In this paper we introduced a deterministic DEM method for testing ADCs and compared this technique with a recently introduced random DEM testing strategy. With this approach, DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADC. In both test strategies, the DEM is not used in real-time single path thus circumventing some of the limitations related to "specification averaging" inherent in using DEM for real-time signal processing. Through simulations, it was observed that the performance of the deterministic DEM method is substantially better from a testing viewpoint than what is attainable with a standard random DEM approach but both approaches offer major improvements over what can be achieved using the same DAC with no dynamic element matching involved. These techniques offer potential for use both in BIST and production test environments.

7. REFERENCES

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[4] Galton I. and Carbone P. "A Rigorous Error Analysis of D/A Conversion with Dynamic Element Matching". *IEEE Transactions on Circuits and Systems,* Vol. 42, pp. 763-772, December 1995.