EXPERIMENTAL EVALUATION AND VALIDATION OF A BIST ALGORITHM FOR CHARACTERIZATION OF A/D CONVERTER PERFORMANCE*

*Kumar L Parthasarathy, Le Jin, Turker Kuyel**, Dana Price***, Degang Chen & Randall Geiger*

Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011, U.S.A.
**Texas Instruments, Inc., ***Motorola Inc.
Email: rlgeiger, djchen@iastate.edu, kuyel@ti.com, dana.price@motorola.com

ABSTRACT

A new histogram based algorithm for characterization of Analog-to-Digital converters has been introduced. The proposed method is based on using highly nonlinear but stationary signal, which can be easily and practically generated on chip. This not only relaxes the requirement on the signal generator, but also enables the use of fast sources, thereby reducing test time and test costs. Experimental test results on commercially available 10-bit pipelined ADCs indicate that the algorithm can estimate the linearity specifications of the device to within 0.5LSB by using an input signal of just 2-bit linearity.

1. INTRODUCTION

One of the main classes of mixed-signal circuits that are widely used in communications and signal processing arena is Analog-to-Digital Converters (ADC). With the increasing complexity of these circuits, testing of these devices has become a challenging and costly process [1]. Long test time and huge investment on commercially available mixed-signal testers have resulted in the need for alternate testing strategies. BIST structures offer potential solution not only in terms of reduction of costs associated with using testers, but also in terms of its ability to test deeply embedded SoC and provide additional self-calibration facilities resulting in value addition of the parts [2].

Traditional approaches to BIST solutions for ADC characterization have been aimed at generation of precise input stimuli on chip that can be used to characterize the device. A new approach based upon using nonlinear and stationary stimuli has been proposed by the authors and the preliminary results are given in [2, 3]. In this work experimental test results performed on commercially available chips have been presented to confirm the validity of the algorithm.

2. ALGORITHM DESCRIPTION

Unlike the standard approach of using a highly precise ramp signal to characterize the device, the proposed method uses two highly nonlinear but stationary signals as inputs and the outputs obtained are then analyzed to characterize the device. A complete formulation of the algorithm with the detailed equations is presented in [3]. A brief summary of the various notations used and the final equations are given below for reference.

Figure.1. shows a plot of the transfer-characteristics of the input excitation signals. Overlaid on top are the ideal and non-ideal trip points of the flash converter. The various symbols that are used in the figure are described below:

$\mathbf{I_i}$: i^{th} transition level (trip point) of an ideal ADC
$\mathbf{T_i}$: i^{th} transition level of an actual (non-ideal) ADC
$\mathbf{\Psi_i}$: Deviation of Ti from Ii
F1 : 'ramp-like' input signal
F2 : F1 shifted by α
$\mathbf{C_i'}$: Sample count in i^{th} bin with F1 as input signal
$\mathbf{C_i''}$: Sample count in i^{th} bin with F2 as input signal

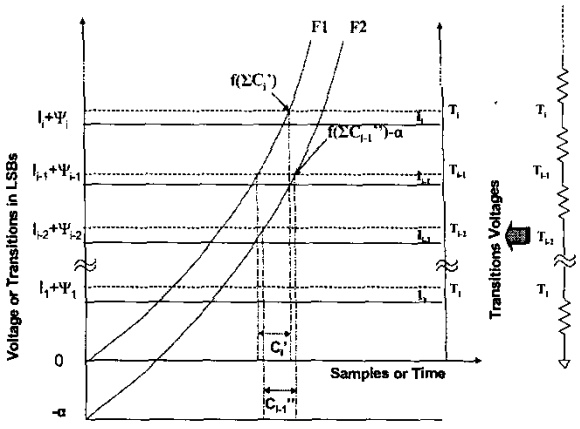

Figure.1. Transfer Characteristics of the Input Excitation

The signal F2 is obtained by shifting F1 by a fixed voltage level α. The trip points of the non-ideal ADC and that of the ideal ADC are related as:

$$T_i = I_i + \Psi_i, i = 1, 2, ..., 2^N \quad (1)$$

where N refers to the resolution of the ADC. Our goal in identifying the system is to determine the actual deviations of the ADC under test from that of an ideal ADC. In terms of the notations used, the goal is to determine the sequence $<\Psi_1, \Psi_2, ..., \Psi_2^N>$.

If the input signal is assumed to be defined by a function 'f' and if the signal is sampled uniformly in time, then the samples obtained in each bin can be related to trip points as follows:

* This work was supported, in part, by the Semiconductor Research Corporation, the National Science Foundation, and the R. J. Carver trust.

0-7803-7761-3/03/$17.00 ©2003 IEEE

$$f(\sum_{j=1}^{i} C_j') = T_i = I_i + \Psi_i, i = 1,2,...,2^N \quad (2)$$

Also since the second signal, F2, is obtained by shifting the first signal, F1, by a constant value (α), we get:

$$f(\sum_{j=1}^{i} C_j'') = I_i + \Psi_i + \alpha, i = 1,2,...,2^N \quad (3)$$

Subtracting the (i-1)th equation in (3) from the ith equation in (2), we get:

$$f(\sum_{j=1}^{i} C_j') - f(\sum_{j=1}^{i-1} C_j'') = 1 + \Psi_i - \Psi_{i-1} - \alpha; i = 2,3..2^N \quad (4)$$

where $I_i - I_{i-1} = 1$ LSB. The above equations relate the histogram values to the trip points of the converter. Using a simple linearization technique as explained in [3], we reduce the equations in (4) as follows:

$$1 = \frac{1}{1-\gamma_i}\alpha + \Psi_{i-1} - \Psi_i, i = 2,3,...,2^N \quad (5)$$

$$\text{where, } \gamma_i = \frac{1}{2}\left(\frac{1}{C_i'} + \frac{1}{C_i''}\right)\left(\sum_{j=1}^{i} C_j' - \sum_{j=1}^{i-1} C_j''\right) \quad (6)$$

These sets of equations can then be simultaneously solved for all of the unknowns. Two possible methods of solving the above equations have been considered. One method involves using L2 norm to find the variables as described in [3]. However, this involves a 'matrix inversion' step that increases the computational complexity for ADC resolution in excess of 9~10 bits. An alternate approach is based on solving the value of α first. With the value of α available, a much simpler set of equations given in (7) is obtained.

$$\Psi_i = N - i - \sum_{j=i}^{N-1} \frac{1}{1-\gamma_{i+1}}\alpha, i = 1,2,...,2^N - 1 \quad (7)$$

The computational complexity of equation (7) is proportional to the number of equations (2^N), as compared to the complexity for matrix inversion method that is of the order of 2^{3N}. The latter solution is more attractive from complexity viewpoint, provided α can be determined by some alternate method with sufficient accuracy. One proposed method is to use all C_i' and C_i'' to estimate α, and then replace its value in equation (7). The equation used to determine α is given by:

$$\alpha = \left(\frac{\sum_{i=1}^{N-1} C_{i+1}'}{\sum_{i=1}^{N-1} \frac{1}{1-\gamma_i}}\right)\left(\frac{N}{\sum_{i=1}^{N} C_i'}\right) \quad (8)$$

Detailed simulation results using both the approaches have been presented in [3]. The modeling of the input signals generator and the ADC that was used for various simulations have also been described. Simulation results, given in [3] shows that a 10-bit flash ADC can be characterized to the 13-bit level from initial 6-bit accuracy or worse while using a stimulus that is only 5-bit accurate.

3. EXPERIMENTAL RESULTS

The proposed algorithm was then tested on different commercial ADCs to verify the functionality. Support in testing, in terms of the tester time, different DUTs and raw data were obtained through an industrial liaison sponsoring the project. A 10-bit pipeline ADC was considered as the device-under-test to prove the concept. Although the algorithm above has been described assuming the ADC is of flash architecture, the concept can be extended to other types of architectures as well.

A commercial tester used in production testing was used to generate the input signals and collect the output histograms. The tester was programmed to generate the non-linear input signals. A very highly non-linear signal (approximately just 2-3 bit linear) was used as input to the device. Although signals of much better linearity can be generated on-chip, to confirm the robustness of the algorithm and to consider the case of high resolution ADCs (14 bit and above) where 8-9 bit linear input signals are limiting factor, the input signals in the test runs were intentionally limited to 2 bits. The second signal was obtained by adding a DC shift value to the first signal, amounting to approximately 10 LSBs of the ADC. This information about the non-linearity of the input signal and the amount of shift was initially known only to the liaison and was not supplied. The parameters were independently calculated as part of the algorithm and were then confirmed through the liaison.

In addition a highly linear ramp signal was used to identify the device's actual characteristics, so that the results of the proposed algorithm can be compared and analyzed. The signals were sampled such that on average, the number of samples in each bin is nearly 32. Both the proposed algorithms were then implemented on the nonlinear histogram data and the results obtained are summarized below.

3.1. Result of Matrix-Inversion approach

The INL of the device was first calculated using matrix inversion approach. The INL of the first and last point was not zero. The data was then corrected for gain error. The plot of the actual INL (obtained using a linear ramp signal) and that estimated is given in figure 2.

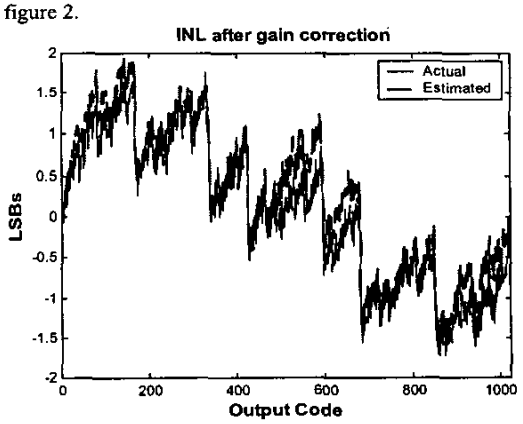

Figure.2. INL estimated using matrix-inversion approach

It can be seen from the figure that the predicted INL values closely follows the actual value. The error in prediction is shown in Figure 3. The results obtained from the actual experimental results are not as good as that obtained from simulations [given in 3]. This is mainly because of effects of noise in the ADC, noise in the measurement system and tester and additional higher order nonlinearities in the input signals that were not considered in the simulation.

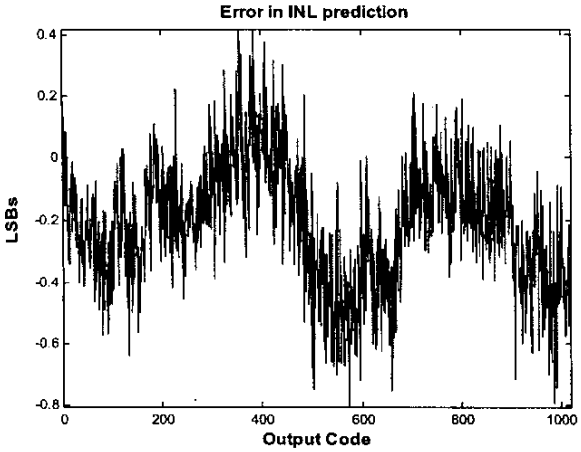

Figure.3. Error in INL prediction

However what is of more importance is the fact that with an input signal of just 2 bit linearity, a 10 bit ADC can be characterized to within +/- 0.5 LSBs. This result supports the existence of a promising solution to the traditional testing problems. The input signal nonlinearity and the shift between the two signals were then estimated using the algorithm. The shift estimated by the algorithm was 10.8314 LSBs, close to that provided by the liaison.

3.2. Result of Alpha-Estimation approach

The same histogram data was then used with the alpha-estimation method to characterize the device again. Figure 4 gives the plot of the INL after gain correction. The error in prediction is given in Figure 5.

The error in prediction is nearly of the same magnitude as that obtained using the matrix inversion approach. It was observed in the various simulated results [3] that by using the matrix inversion algorithm the error in prediction can be reduced to nearly 0.02~0.05LSB, while that using the alpha method was in the range of 0.2~0.3LSBs. This order of improvement is not evident in the experimental results even with matrix inversion approach. This is mainly because of the inherent noise in the system, which limits the overall accuracy of the results obtained.

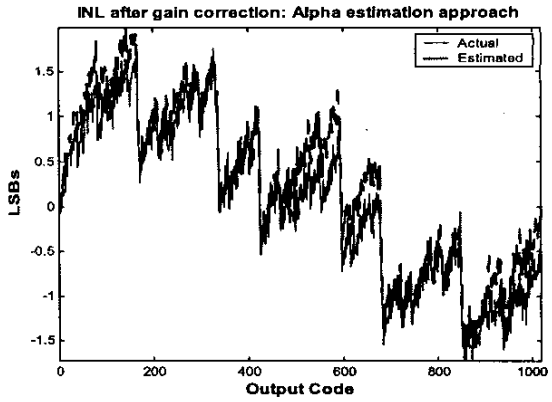

Figure.4. INL estimated using alpha-estimation approach

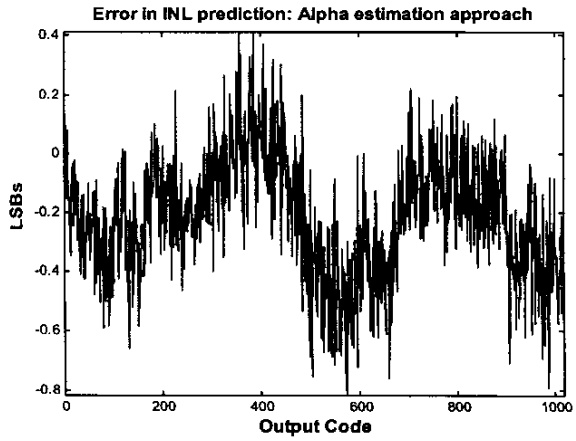

Figure.5. Error in INL estimation - using alpha-estimation

Further simulations were performed to understand the effect of noise in the test setup. Typically, when a histogram test is performed, multiple ramps are input to the device and the output histograms are averaged to get the final histogram. This is essential because the noise in the test setup results in samples corresponding to a particular bin falling in adjacent bins, thereby changing the histogram count. To eliminate this random noise, multiple runs are performed and the results averaged. However, this does not completely eliminate the noise in the measured data. This is one of factors affecting the results of the algorithm in the experimental tests.

To see the effect of averaging, one similar 10 bit part was randomly picked. The same histogram test described above was performed three times, but with the number of ramps (used in averaging) being different each time. The INL predicted by using the histogram data obtained using one ramp is shown in figure 6. It can be seen that the error in prediction is in the order of couple of LSBs.

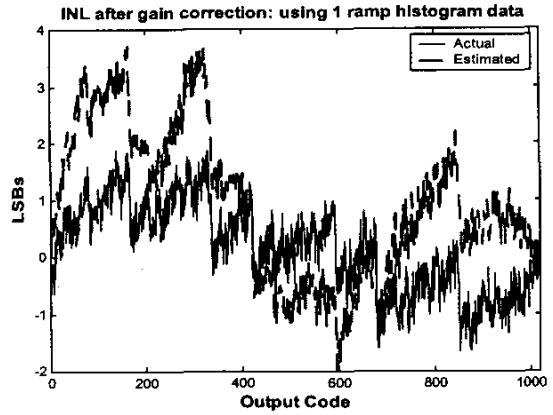

Figure.6. INL estimation – for 1 ramp histogram data

Two more runs with histogram averaged over 10 ramps and 50 ramps were performed. The error in prediction reduced to within 1LSB for the 10 ramp data and to nearly 0.6LSB for the 50 ramp data as shown in figure 7. This improvement in result with averaging, confirms that the effect of noise in measurement is one of the main factors limiting the performance of the algorithm. However, considering the fact that a 2 bit linear signal is used to characterize a 10 bit device, the estimation is still within reasonable range.

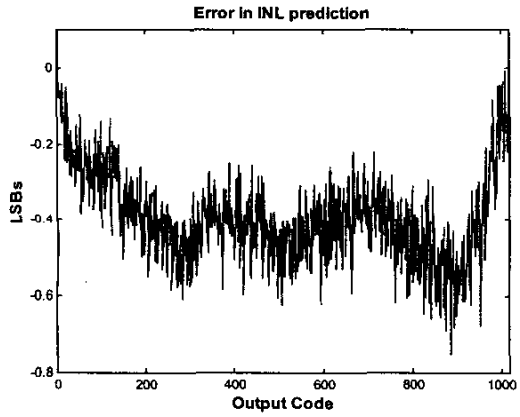

Figure.7. Error in INL estimation - using 50 ramps averaged histogram data

Having seen the performance of both the algorithm on the actual test data (for 1 device) and the effect of noise in the measurement setup, the experiments were repeated on 20 different samples (different ADCs). Similar input signal (nearly 2 bit linear) was used to test all the devices. The amount by which the second nonlinear signal is shifted with respect to the first one was nearly 10LSBs for all devices. The histograms obtained for the devices were then used to characterize the devices. Figure 8 shows the maximum error in prediction for each device.

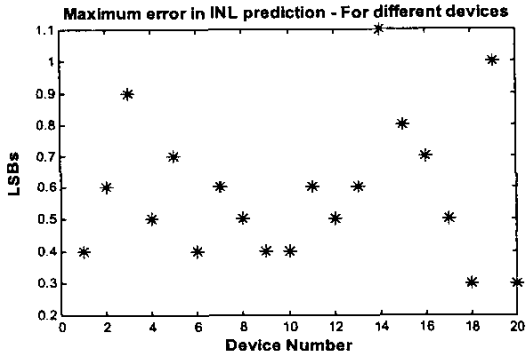

Figure.8. Error in INL estimation – for 20 devices

It can be seen that for most of the parts, the error in prediction is around 0.6LSBs. To see the effect of noise, one part was picked again, and linear ramp test was performed on the same device twice; and the INL predicted using the two linear ramp data were compared. Ideally we would expect the INL prediction to be same, since they represent the same device. But a maximum error of 0.7LSB was found using the two linear data, indicating that noise in measurement is a major limiting factor. Given this effect of noise in measurement, due to factors like temperature and time related drift, the above errors in estimation using the proposed algorithm is very reasonable.

4. CONCLUSION

A new code-density based algorithm for ADC characterization has been introduced. Two methods of solving the characterization problem have been considered. A detailed formulation of the algorithm with simulations results were provided in [3]. In this work, experimental test results on commercially available ADCs have been provided. Chip test results indicate that by using 2-bit linear input stimuli, the algorithm can still estimate the INL of a 10-bit device to within 0.5LSB. Experimental results to understand the effect of noise in measurement on the performance of the algorithm have also been provided.

5. REFERENCES

[1] M.Burns and G.W.Roberts, "*An Introduction to Mixed-Signal IC Test and Measurement,*" Oxford University Press, New York, USA 2000.

[2] K.L.Parthasarathy, Le Jin, Degang Chen & R.L.Geiger, "*A Modified Histogram Approach for Accurate Self-Characterization of Analog-to-Digital Converters*", Proceedings of 2002 IEEE ISCAS, Arizona, May 2002.

[3] K.L.Parthasarathy, Le Jin, Turker Kuyel, Degang Chen & R. L. Geiger, "*A Histogram Based AM-BIST Algorithm for ADC Characterization using Imprecise Stimulus*", Proceedings of the 2002 IEEE MWSCAS, Aug 2002.