A 9b 165MS/s 1.8V Pipelined ADC with All Digital Transistors Amplifier*

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Abstract

A 9bit, 1.8V, 165MS/s pipelined ADC was built in a 0.21μ CMOS digital process. The inter-stage amplifier in this converter was built using all digital transistors. To get sufficient gain with digital transistors a self-adjusting positive feedback operational amplifier that shows low sensitivity to output swing was used. The ADC consumed a total power of 90mW when operated at full speed.

1. Introduction

There is an increasing demand for high-speed low cost signal processing functions in applications such as HDTVs, digital camcorders, and portable data communications (1). ADCs for these applications require a low-supply voltage, low power consumption, 8-10 bits of accuracy and a high sampling rate of 100MHz or higher (1). The most recently reported single-channel CMOS ADCs with high sampling rate are compared in Fig. 1 (1-10). Analog integration in deep sub-micron CMOS has become an economic necessity for such applications. One of the most important and most difficult challenges is to integrate such circuits in purely digital sub-micron technologies (2,11). Central to these challenges is the ability to build fast settling high gain operational amplifiers (Op-Amps) in the purely digital processes. Other challenges relate to switch resistance issues.

New digital processes provide fast devices with low supply voltage operation but at the cost of a relatively high threshold voltage, V_t, and a high output conductance. Traditional methods of enhancing DC-gain such as cascading, cascoding, and regulated cascoding are loosing their ability to provide adequately high DC gain due to the high output conductance of digital transistors (11-14). In spite of the fact that design challenges can be reduced by using analog friendly, low threshold voltage devices, this approach leads to increased fabrication costs. Moreover, analog friendly devices are leaky, their sizes are larger than the counterpart digital transistors, and generally the analog friendly devices require increased power dissipation (11,12).

The implementation of a low supply voltage low power dissipation 9bit 165MS/s pipeline ADC using all digital transistor Op-Amp with positive feedback is described in the following sections. The implemented positive feedback technique has a low gain sensitivity to both temperature and process variations.

* This work was completed at Texas Instruments Inc.

2. Proposed Architecture

In this work, a 1.8V 9-bit pipelined ADC that can run as fast as 165MS/s is described. The block diagram of this ADC is shown in Fig. 2. The pipeline is constructed using four 3-bit stages. The first three stages have one bit of redundancy to provide relaxed requirements for the comparator and amplifier offsets, As shown in Fig. 2. The ADC is preceded by a switched capacitor programmable gain amplifier. The ADC consists of three bit (3b) multiplying analog to digital converters (MDACs), 3b flash sub-ADCs, and supporting circuits that include non-overlapping clock generators, and digital decoders. Each of the first three stages produces 3-bit codes, after the digital error correction (DEC) process the final ADC output word will be 9-bits long. A maximum comparator offset of $0.125V_{ref}$ can be tolerated. The voltage comparators have two stages, a pre-amplifier followed by a dynamic latch. An auto-zero technique is used for the voltage comparators to eliminate the offset effect (8). As shown in Fig. 3 the MDAC has gain of 4. For improved speed and linearity, one of the sampling capacitors (C_{sf}) is used as a feedback capacitor too by flipping it between input and output nodes. Fringing capacitors were used to realize the capacitors in the MDAC because they have excellent matching properties, good linearity, and a high capacitance density. Input and output common mode voltages for the MDAC are the same. The input/output common mode reference voltage is generated internally. The 3-bit DAC threshold voltage levels, $\pm0.75V_{ref}$, $\pm0.5V_{ref}$, $\pm0.25V_{ref}$, and 0 level were generated by connecting each of the three MDAC sampling capacitors either to $-0.25V_{ref}$, 0 , or $+0.25V_{ref}$ reference voltages.

The main challenge in building this fast, low supply, low power, ADC is the design of the inter-stage amplifier. In very high speed applications parasitic capacitances of transistors at the amplifier's input/output nodes become an important factor that limits the settling speed. Digital transistors are smaller in size and thus have smaller parasitic capacitances than the analog friendly transistors. The fact that digital transistors have higher threshold voltages than analog friendly devices makes the difference in size for a specific current more significant. Since we are targeting a very high sampling rate, we chose to build the amplifier using all digital transistors.

The two-stage amplifier architecture of Fig. 4a was built to achieve a high differential output swing of $1.1V_{p-p}$ while using a single 1.8V supply. The first stage is a new

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telescopic cascode Op-Amp with positive feedback for gain boosting. The second stage is a simple differential pair. The positive feedback signal used to enhance the DC-gain is derived from the cascode nodes of the first stage. This feedback signal has a very low swing compared to the swing on the output node. Using this node as the sense node will substantially reduce the effect of the output voltage swing on the amplifier gain. The first stage of the amplifier has a simplified half circuit small signal model shown in Fig. 4b. Small signal analysis shows that the first stage has an open-loop gain, A_v, of the form;

$$A_v \approx \frac{g_{m1}\cdot(g_{o2}+g_{m2})g_{m3}}{\left[g_{o1}g_{o3}g_{o4}+g_{o2}g_{o3}g_{o4}+g_{o1}g_{o2}g_{m3}+g_{o3}g_{o4}g_{m2}-g_{o1}g_{o3}g_{m2}\right]} \quad (1)$$

Equation (1) shows that the DC-gain of the first stage becomes very large as $(g_{o1}\cdot g_{o3}\cdot g_{m2})$ approaches $(g_{o1}\cdot g_{o2}\cdot g_{m3}+g_{o3}\cdot g_{o4}\cdot g_{m2})$. To be more precise, achieving this equality makes the gain of the amplifier comparable to what would be achieved with a double cascode structure that would require the stacking of two additional transistors in each half-circuit. Transistor output conductance is given by

$$g_{oi}=\lambda_i I_{dsi} \quad (2)$$

where λi is the channel length modulation coefficient and I_{ds} is the common drain current. It is well known that the λ parameter is dependent on gate length and is given by the relationship

$$\lambda_i = \frac{1}{L_i}\cdot\frac{\partial X_{di}}{\partial V_{dsi}} \quad (3)$$

where X_d is the gate reduction of the channel due to V_{ds} (15). So transistor output conductance is sensitive to both transistor gate length and to the drain to source voltage, V_{ds}. By carefully choosing transistor lengths $L_{1,2,3,4}$, and selecting the biasing point, it follows that the positive feedback resulted in a boost in gain of $(4g_{m2}/3g_{o4})$ which can be quite significant. To view how process variations will affect the quiescent voltages and currents of the circuit in Fig. 4a. By focusing on the common mode operation, Fig. 4c, let us consider the strong PMOS case. For this case, the magnitude of V_{th} for the PMOS transistors will be lower resulting in larger $g_{o3,4}$ and $g_{m3,4}$ since transistors M_3 and M_4 are connected to fixed bias references. Therefore, both the nodes V_{out_T} and V_x will be pulled up towards V_{dd}. Since the operating point of the transistor M_2 is set by the positive feedback connection, and form common mode perspective, M_2 forms an inverting common source amplifier with source degeneration, then increasing its V_{gs} and V_{ds} will turn it on harder increasing g_{m2}, g_{o2}, and g_{o1}. This change will make the increase in the value of the negative term in the denominator of (1) able to track the increase of the sum of the positive terms and adjusting the gain. Note that the change in the excess bias of transistor M_3 is equal to the change of the excess bias of transistor M_2 that helps g_{m2} and g_{m3} to track each other under the assumption of fixed voltage at node V_y. The negative feedback loop of M2, and M3 in the common mode operation has a large gain and its operation is consistent with the operation of the common mode feedback circuit. Similar arguments can be made for the other process corners. The existence of the extra biasing circuitry, shown in faded color in Fig. 4a has two main functions: First, it defines the quiescent biasing voltage, V_y. Second, it helps to fix the voltage of node V_y. Observing nodes $V_x^{\pm}$ we notice that they experience very small swings compared to $V_{out}^{\pm}$. For $V_{out}^{\pm}$ swing of $1V_{p\text{-}p}$ $V_x^{\pm}$ will experience less than $5mV_{p\text{-}p}$ swing. Therefore, the feedback is almost unaffected by the output signal level. The two stages amplifier is Miller compensated. Compensation capacitors (C_{C1}, C_{C2}) where connected to the cascode nodes, for simplicity, only one side of the compensation capacitors is shown in Fig. 4a.

3. Simulation Results

The proposed ADC and amplifier were simulated using Texas Instruments digital 0.21μm CMOS process. Each amplifier in the ADC draws a total current of 6.5mA. All simulation results presented are for differential signals. An AC analysis shows that the amplifier has a DC gain of 81dB with a unity gain frequency of 1.218GHz while driving a 1pF load. Results are shown in Fig. 5. The phase response is shifted up by 180 degrees to give a direct reading for the phase margin. Fig. 5 shows a comparison between the AC analysis of the proposed amplifier and the traditional telescopic amplifier followed by the common source amplifier built using all digital transistors under the same biasing conditions. AC analysis shows that we where able to enhance the DC gain from 64dB to 81dB without sacrificing the bandwidth or phase margin. The DC sweep shows that the amplifier has a maximum swing of $1.5V_{p\text{-}p}$ while maintaining a gain higher than 68dB under nominal conditions. Post layout transient simulation for the whole ADC was performed. At a sampling speed of 165MS/s and using a sampling capacitor, C_s, of 125fF, simulation shows that the amplifier was able to slew and settle to an error less than 0.2mV for a $1V_{p\text{-}p}$ output swing within 2.1nsec. Due to the use of digital transistors as switches in the common mode feedback circuit with low switching voltage, a memory effect, incomplete reset, may appear by sampling at higher frequencies.

4. Test Results

The prototype 9-bit 1.8V pipelined ADC was fabricated in a 0.21μm, 5 metal layer, double poly, CMOS copper technology. A die photo of the ADC is shown in Fig. 6. The die surface was covered with dummy metal layers thus obscuring most relevant details. The total die area for the ADC, a front end programmable gain amplifier (PGA), and a reference amplifier is 711μm X 743μm. The input/output swing of the MDAC is $1.1V_{p\text{-}p}$. The ADC was tested at different sampling speeds. The measured DNL/INL was 0.305/0.7LSB, 0.33/1.03LSB, and 0.87/1.8LSB at 27MS/s, 80MS/s, and 165MS/s respectively. The measured DNL and INL curves at 165MHz are presented in Fig. 7. Test results at

different sampling speeds are listed in Table 1. Sampling errors due to switch resistance became apparent at 165MS/s. The measured total power dissipated in the ADC was 90mW at 165MS/s and 1.8V supply voltage.

The ADC dynamic performance is evaluated by measuring signal to noise and signal to noise plus distortion ratios (SNR and SNDR) in addition to measuring the spurious free dynamic range (SFDR). The measured SNR, SNDR, and SFDR at 165MS/s were 44.3dB, 44dB, and 57dB respectively. SNR measurement for a 0.5V sinusoidal input is shown in Fig. 8. Summary of other measurements appear in Table 1.

5. Conclusions

A 1.8V, 9b low power, pipelined ADC was built using all digital transistors Op-Amp in a 0.21μm CMOS copper technology. Test results show no missing codes at sampling rate of 165MS/s with a total power dissipation of 90mW. An energy efficient fast settling positive-feedback technique with self-adaptive gain adjustment and very low gain sensitivity to output swing was used to build the Op-Amp.

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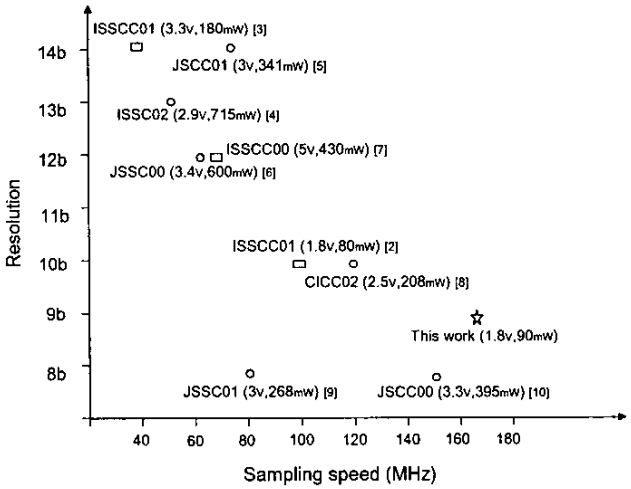

Fig. 1 Previously published fast CMOS pipeline ADCs.

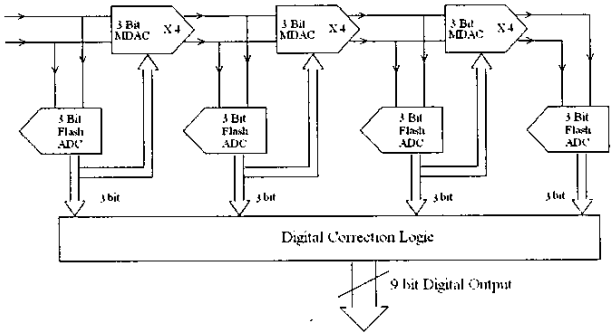

Fig. 2 ADC block Diagram.

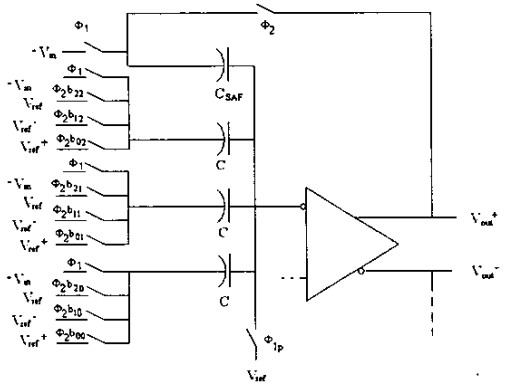

Fig. 3 MDAC schematic.

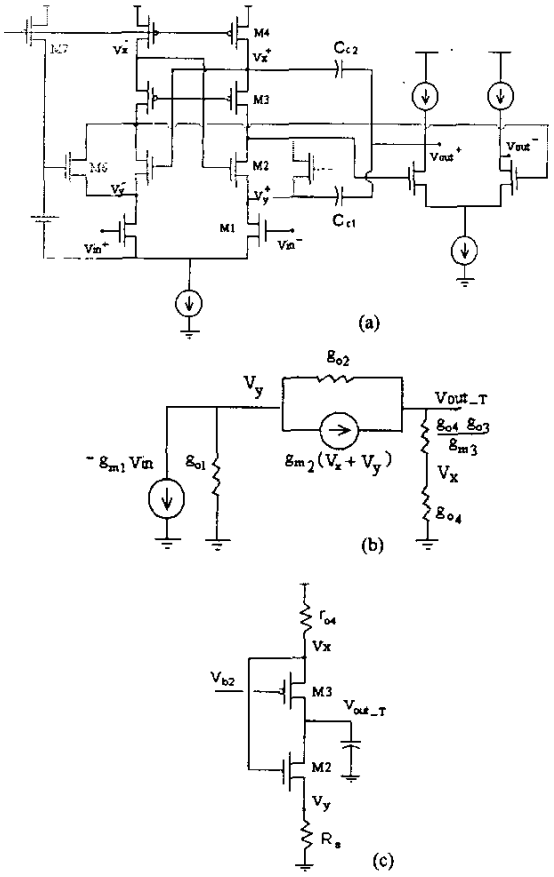

Fig. 4. Proposed amplifier with positive feedback. (a) Amplifier schematic. (b) Small signal model of one side of the 1st stage of the amplifier. (c) Simplified schematic of the common mode of the 1st stage amplifier.

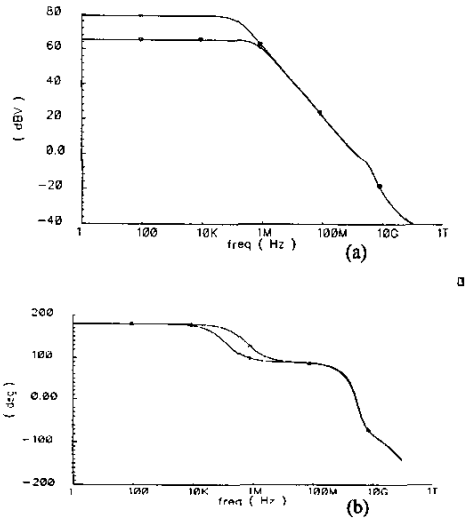

Fig. 5. AC characteristics of the amplifier with and without positive feedback. (a) Magnitude response. (b) Phase response.

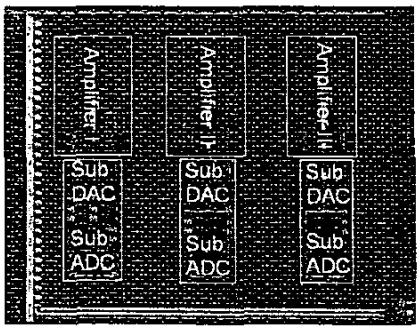

Fig.6 Die photo of the 9-bit pipeline ADC.

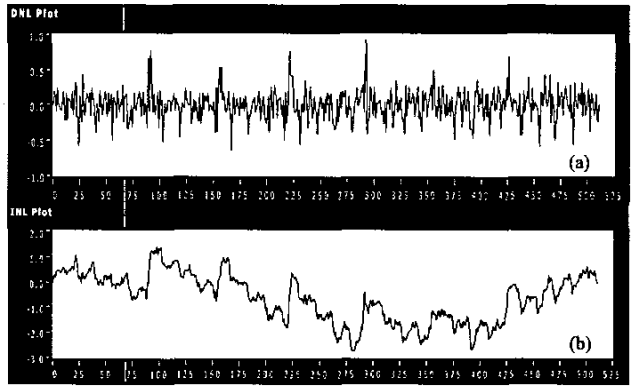

Fig. 7 Linearity measurements for the ADC at 165MS/s. (a) Measured DNL. (b) Measured INL.

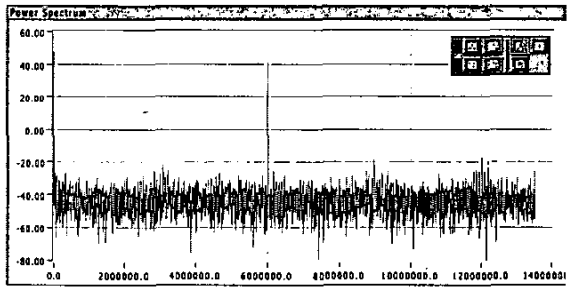

Fig. 8 Measured signal to noise ratio (SNR) for 10MHz input frequency and 165MS/s sampling rate.

Table 1. Summary of ADC performance measurements

Resolution	9-bits		
Process	0.21μm, 2 poly, 5 metal, CMOS		
Power Supply	Single ended 1.8V		
Total Power	90mW		
Die Size	711μm X 743μm		
Sampling Freq.	27 MS/s	80 MS/s	165MS/s
Max swing	1.1 $V_{pk\text{-}pk}$	1.1 $V_{pk\text{-}pk}$	1.1 $V_{pk\text{-}pk}$
DNLmax	0.305 LSB	0.333 LSB	0.87 LSB
INLmax	0.706 LSB	1.026 LSB	2.7 LSB
SNR_{dB}	48.193dB, f_{in}=6MHZ	46.78dB, f_{in}=10MHz	44.48dB, f_{in}=10MHz
$SNRD_{dB}$	47.9dB	46.3dB	44dB