A High-Frequency 750mV Operational Amplifier in a Standard Bulk CMOS Process

Yonghui Tang and Randall L. Geiger

Department of Electrical and Computer Engineering
Iowa State University, Ames, IA 50011, U.S.A

Abstract: A 750mV operational amplifier was designed in a standard 0.5μm 5V CMOS process using a threshold voltage tuning technique. It exhibits 62dB DC gain, a gain bandwidth product of 3.2MHz and a power consumption of only 38μW. Compared to its 5V counterpart biased at the same current level, the new amplifier maintains nearly the same gain bandwidth product when driving a 15pF load but consumes less than 20% of the power with over a factor of 6 reduction in the supply voltage.

I. Introduction

With the popularity of battery-powered devices and mobile systems, the design of low voltage low power CMOS analog circuits has become a subject of considerable interest. This interest has been driven primarily by the emergence of fine feature processes and the associated potential for a reduction in supply voltage and power dissipation. The drop in threshold voltage has not been as aggressive thus limiting the potential for high speed analog circuits to fully benefit from the scaled technology. The concept of operating high speed analog circuits at supply voltages at 2 or 3 threshold voltages (V_T) is challenging. The literature is void of the concept of operating these circuits at supply voltages at or below the threshold voltage.

As the fundamental building block for analog signal processing, the operational amplifier (op amp) is generally chosen as the test bed for new low voltage analog design methodologies with considerable research efforts focused on CMOS low voltage operational amplifier design. Most can be classified into one of three design strategies.

The first is based upon new low voltage circuit structures that use standard transistors. With this approach, the goal is to maintain key circuit performance metrics at reduced supply voltages. Included in this category are dynamic biasing circuits [1] and regulated-cascode structures [2]. Both approaches offer performance comparable to that attainable with traditional higher voltage design but the voltage scaling achievable with this approach is limited. A second strategy is based upon using bulk-driven transistors. This approach can be used in standard bulk CMOS processes but only the p-channel devices can be bulk-driven in an n-well process. A major disadvantage of the bulk-driven MOSFET is the substantially lower transconductance compared to that of a conventional gate-driven MOSFET when compared at the same current levels [3]. This generally results in a much lower gain bandwidth product (GB) and poorer frequency response at a given power level. Bulk-driven amplifiers were reported in [4] and [5]. The third strategy is based upon using special devices in non-standard processes. Depletion-mode devices were used in [5] and floating-gate transistors were used in [6]. Good floating-gate transistors require a special thin-oxide double-poly process (often termed a "flash process"). Depletion-mode transistors are rarely available in standard bulk CMOS process.

The value of and the matching of threshold voltages are fundamentally limiting the ability of designers to realize low voltage analog and mixed-signal circuits. If the effective threshold voltage could be predictably reduced using circuit design techniques, very low voltage analog circuits could be implemented. In this paper, a threshold voltage tuning technique is introduced that allows strong inversion operation at supply voltages below the threshold voltage in any standard bulk CMOS process.

II. Threshold Voltage Tuning Scheme

The threshold tuning technique is illustrated in Fig. 1. Low V_T transistors with lower effective threshold voltages are created by adding voltage sources in series with the gates of a standard transistor. The effective threshold voltages can be controlled by the bias voltages V_{dcp} and V_{dcn}. Assuming an ideal voltage source, the performance of the low V_T transistor at a given quiescent current level will be nearly the same as that of a normal transistor except it will appear to have a lower threshold voltage. Circuits built with virtual transistors can be designed to consume less power than those built with standard transistors because the supply voltage can be significantly reduced.

Fig. 1(c) shows a switched capacitor (SC) implementation of the voltage sources for both n-channel and p-channel transistors. The concept depends on keeping a constant voltage across the capacitors. Due to current leakage in the switches, the capacitors need to be recharged periodically. In order to accomplish this, a bias voltage V_{dcn} or V_{dcp} charges the capacitor C_1 when the

0-7803-7842-3/03/$17.00 © 2003 IEEE

switch controlled by ϕ_2 is on. When the switch controlled by ϕ_1 is on, C_1 is connected in the signal path and shares its charge with C_2. Because the current leakage is very small, the frequency of the clock signals ϕ_1 and ϕ_2 can and should be very low in order to reduce the noise injected to the signal path during switching. To ensure correct operation, ϕ_1 and ϕ_2 are assumed to be non-overlapping clocks such as are commonly used in many existing SC circuits. C_2 is included so the voltage can be refreshed in the background without the need for interruption of the normal operation of the circuit. With this approach, the standard deviation of the threshold voltage of adjacent devices is essentially the same as that of the standard transistor but with a replica biasing circuit for generating the bias voltages, process and temperature variations will be compensated. Variants of the implementation in Fig. 1(c) can be used to reduce the standard deviation of the effective threshold voltage below that of the parent devices but will not be discussed in this paper.

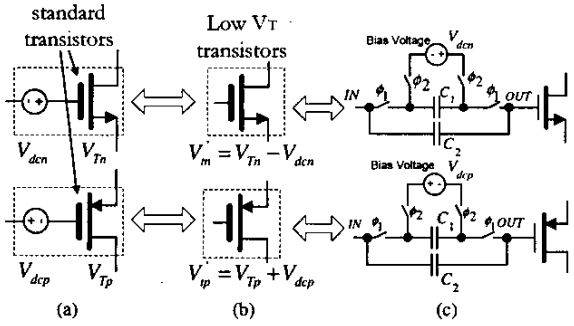

Fig. 1 (a) Standard transistors; (b) Low V_T transistors; (c) An SC implementation of the voltage sources

III. Low Voltage Op Amp Implementation

A low voltage two-stage op amp was designed to demonstrate the proposed threshold voltage reduction technique. The basic structure of this op amp, derived from a basic two-stage op amp, is shown in Fig. 2. Since transistors that have the same gate connection can share a single voltage source, only 6 voltage sources are needed for this 9-transistor circuit. The goal in this design is to maintain the same gain and GB for the low voltage op amp as for a 5V op amp designed in the same process with the same circuit structure and the same current levels. In what follows, the counterpart 5V op amp will be termed the "parent" amplifier.

The seemingly simple switched capacitor voltage source of Fig. 1(c) actually presents the biggest challenge in this design because when operating at supply voltages at or below the threshold it is difficult to turn on the switches. Since the switched capacitor circuits are in the control path rather than the signal path of the op amp, the performance requirements of the switched capacitor circuit are, however, relaxed. In order to realize the switch capacitor voltage sources, some support circuitry is needed.

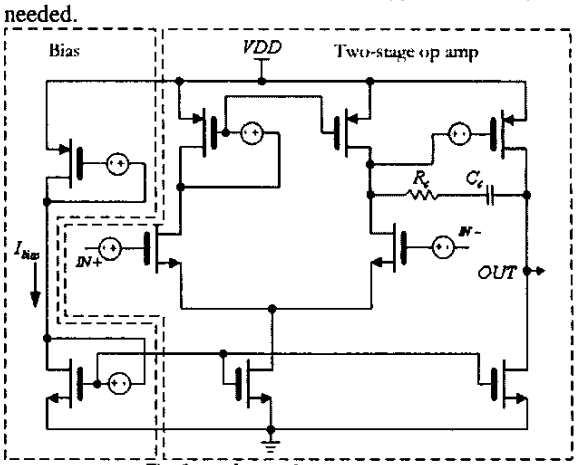

Fig. 2 Low voltage op amp core

A block diagram of the support circuitry used in this implementation is shown along with the op amp core in Fig. 3. The Oscillator generates a relatively high frequency clock signal which is reduced in frequency by a Frequency Divider. A Pulse Generator is then used to drive a Non-overlapping Clock Generator that creates the non-overlapping clock signals ϕ_1 and ϕ_2 . A Clock Booster boosts these clock signals to about $3V_{DD}$ so that they can be used to drive switches. These boosted clock signals along with the Bias Voltage Generator are used to drive the Switched Capacitor Voltage Source. The Bias Voltage Generator generates the DC voltages V_{dcn} and V_{dcp}. Since the dynamic performance of the support circuitry is not critical, all support blocks except the Clock Booster were designed to operate in either the subthreshold region or the weak inversion region and all are biased with the supply voltage V_{DD}. By operating as much of the support circuitry in the subthreshold or weak inversion regions as possible, the power consumption of the support circuitry can be maintained at a low level. The Low-Voltage Op Amp Core and the Switched Capacitor Voltage Source operate in the strong inversion region to maintain good high frequency performance of the op amp.

The Oscillator that used in this design is a 7-stage ring oscillator. Each stage is simply a CMOS inverter. The Frequency Divider is implemented with a four-stage DFF architecture to provide a 16:1 reduction in the clock frequency.

Fig. 4 shows a block diagram and the output of the Pulse Generator. The Pulse Generator is used to generate a short-pulse "A" over a long period. During "A", capacitors C_1 of Fig. 1(c) are charged to the bias voltages V_{dcn} or V_{dcp}. But most of the time all the

capacitors are connected to the signal path without charging.

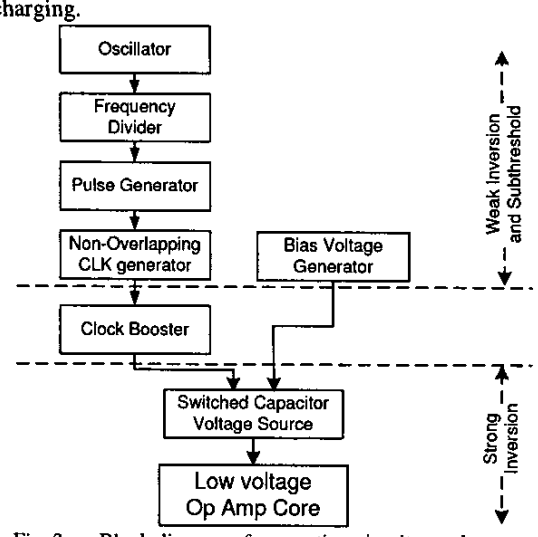

Fig. 3 Block diagram of supporting circuitry and op amp core

The clocks ϕ_1 and ϕ_2 should be non-overlapping to ensure correct operation, that is, ϕ_1 must turn off before ϕ_2 turns on at the beginning of charging and ϕ_2 turns off before ϕ_1 turns on at the end of charging. A non-overlapping clock generator that is commonly used in SC circuits was used to fulfill this task.

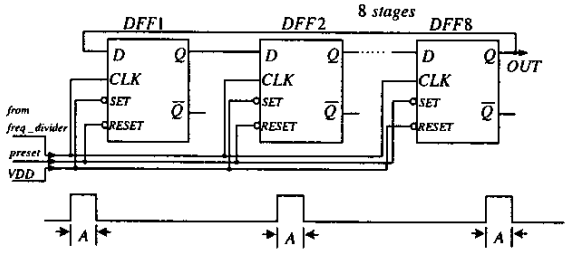

Fig. 4 Pulse generator structure and its output

Clock booster circuit is shown in Fig. 5. When the input is low, M3 and M5 are on (sub-threshold or weak inversion), M4 is off, the capacitor C is charged to VDD, and the output is zero. When the input is high, M3 andM5 are off and M4 is on. This forces the voltage level at C- to VDD and the voltage level C+ to 2VDD. The voltage at C+ is transferred through M4 to the output. When the voltage at C+ becomes higher than VDD, some charge will leak through M3 because the drain voltage of M3 becomes higher than its source voltage. To minimize this leakage, the size of M3 has been kept small in our design. The leakage in M3 practically limits the amount of boosting achievable with this simple booster circuit to the 1.5VDD–1.8VDD range in typical processes. In our design, two stages were used to boost the high clock level from VDD to about 3VDD.

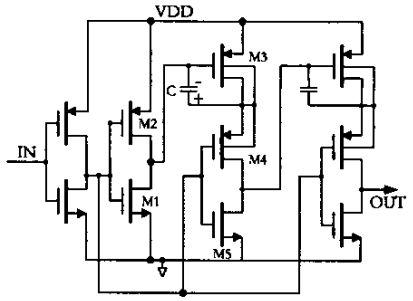

Fig. 5 Clock booster

IV. Experimental results

A 750mV operational amplifier was fabricated in an AMI 0.5μm CMOS process with $V_{TP} \approx -0.9V$ and $V_{TN} \approx 0.8V$ through the MOSIS program. In order to make a fair performance comparison with a standard op amp, we also designed a "parent" 5V op amp which has the same two-stage structure, the same transistor sizes and the same current levels as the low voltage op amp but without the voltage sources V_{dcn} and V_{dcp}.

Both were fabricated on the same die as shown in the die photograph of Fig. 6. The active area is 560μm ×760μm. About 80% of the die area is occupied by supporting circuits including capacitors. At the outset, it may appear that the overhead for the supporting circuitry is quite large. It should be observed, however, that if a larger number of operational amplifiers or other analog circuits using the reduced effective threshold voltage transistors were used, much of the support circuitry would not need to be repeated thus the area overhead per transistor would drop dramatically.

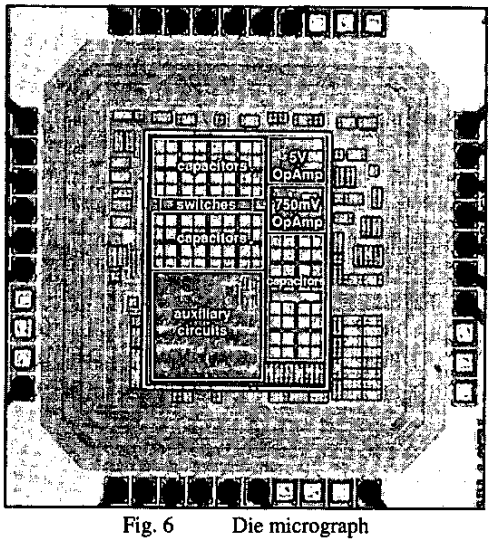

Fig. 6 Die micrograph

Table 1 Summary of the measured op amp performance, ~15pF load capacitance

	@750mV	@800mV	@900mV	@1V
Slew Rate	3.1V/μS	3.8 V/μS	5 V/μS	6.36 V/μS
GB	3.2MHz	3.7MHz	3.9MHz	4.2MHz
DC gain	62dB	64dB	64.6dB	64dB
Input offset voltage	2.2mV (avg. of 15 samples)	N/A	N/A	N/A
Input common mode range	0.1V-0.58V	0.07V-0.64V	0.02V-0.76V	0V-0.89V
Output swing for linear operation	0.31V-0.58V	0.27V-0.67V	0.15V-0.78V	0.1V-0.82V
PSRR at DC	82dB	N/A	N/A	N/A
CMRR at DC	56dB	N/A	N/A	N/A
Total power consumption	38.3μW (4% by supporting circuits)	53.6μW (3.4% by supporting circuits)	81μW (2.7% by supporting circuits)	106μW (2.4% by supporting circuits)

The measured performance of the op amp is summarized in Table 1. It works with a supply voltage as low as 750mV which is about $0.9V_T$.

Fig. 7 shows the waveforms for step response of the non-inverting unity gain feedback configuration when powered with a supply voltage of 750mV.

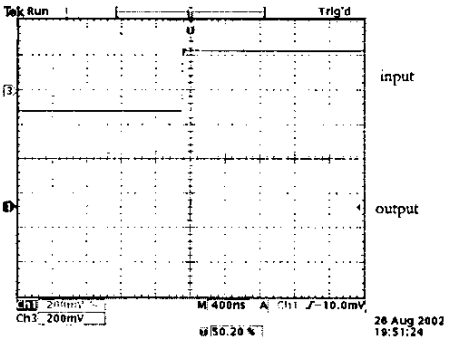

Fig. 7 Step response of the unity gain feedback configuration

Table 2 Comparison of low voltage and 5V op amps

	DC gain	Current	Power	GBW	Slew Rate
LV op amp@750mV	62dB	51μA	38.3μW	3.2MHz	3.1V/μS
LV op amp@800mV	64dB	67μA	53.6μW	3.7MHz	3.8V/μS
5V op amp	84dB	70μA	350μW	4MHz	3.9V/μS

Table 2 shows the comparison of the experimental results of the low voltage and the parent 5V op amps. All parametric performance data is comparable to that measured from the "parent" 5V op amp with the exception of the power dissipation which for the 750mV op amp is a factor of 9 less. In particular, the targeted high frequency performance as determined by the GB is comparable between the low voltage amplifier and its parent circuit. The DC gain of the low voltage op amp is about 20dB lower than the parent amplifier. This is due to a reduction in output impedance because of the lowered V_{ds} for the MOSFETs in the low voltage op amp. A total of 15 circuits were fabricated and all 15 were tested giving comparable measurement results. This, in part, suggests this approach shows reasonable robustness.

V. Conclusion

A threshold voltage tuning technique that provides for operating analog and mixed-signal circuits with supply voltages at or below the threshold voltage of a process while still maintaining high frequency performance characteristic of strong inversion operation has been introduced. To validate this technique, a 750mV op amp was designed and tested. It uses only standard transistors available in any bulk CMOS process and operates at supply voltages LOWER than the threshold voltage of the process. Critical transistors in the op amp core operate in the strong inversion region despite the extremely-low supply voltage. The low voltage op amp maintains performance comparable to that achievable in traditional high voltage design while substantially reducing both the supply voltage and the power consumption. This is the first reported op amp designed in a standard process that operates with a supply voltage below the threshold voltage of the process.

References

[1] G. Giustolisi, G. Palmisano, G. Palumbo, T. Segreto, "1.2V CMOS op-amp with a dynamically biased output stage", IEEE J. Solid-State Circuits, Vol. 35, pp. 632-636, April 2000

[2] G. N. Lu, G. Sou, "1.3V single-stage CMOS opamp", IEE Electronics Letters, Vol.34, pp. 2073-2074, Oct. 29, 1998

[3] E. Sanchez-Sinencio, "Low voltage analog circuit design techniques: a tutorial", IEEE Circuits and Systems Dallas workshop 2000, March 27, 2000

[4] P. E. Allen, et al. "A 1V CMOS op amp using bulk-driven MOSFETs", Digest of Technical Papers of IEEE International Solid-State Circuits Conference, pp. 192 -193, 1995

[5] T. Stockstad, H. Yoshizawa, "A 0.9V 0.5μA rail-to-rail CMOS operational amplifier", IEEE J. Solid-State Circuits, Vol.37, pp. 286-292, March 2002

[6] J. Ramirez-Angulo, et al. "Low-voltage CMOS op-amp with rail-to-rail input and output signal swing for continuous-time signal processing using multiple-input floating-gate transistors", IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, Vol. 48, pp. 111-116, Jan 2001