BIST and Production Testing of ADCs Using Imprecise Stimulus

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A new approach for testing mixed-signal circuits based upon using imprecise stimuli is introduced. Unlike most existing Built-In Self-Test (BIST) and production test approaches that require excitation signals that are at least 3 bits or more linear than the Device-Under-Test (DUT), the proposed approach can work with stimuli that are several bits less linear than the DUT. This dramatically reduces the requirements on stimulus generation for BIST applications and offers potential for using inexpensive signal generators in production test, or for testing DUTs that have a linearity performance exceeding that of the available test equipment. As a proof of concept, a histogram-based algorithm for linearity testing for Analog-to-Digital Converters (ADCs) has been proposed. It can estimate the Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) of an n-bit ADC by using a ramp signal of much less than n-bit linearity and a shifted version of the same nonlinear ramp as excitation. The performance of the algorithm is comparable to that of the traditional method which uses (n+3)-bits or a decade more linear input signals. Complete algorithm description, extensive simulation results and experimental results obtained from using a production tester on commercially available ICs are presented to validate the potential of this algorithm.

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Additional Key Words and Phrases: Production test, built-in self-test, ADC linearity

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1. INTRODUCTION

The rapid growth in the application of increasingly complex mixed-signal circuits in the communication and signal processing arenas coupled with industry-wide improvements in semiconductor processing has created a large market for low-cost mixed-signal integrated circuits. Paralleling this downward cost pressure are increasing demands on the number, accuracy and complexity of parametric testing steps in the production test environment and increasing incentives to develop a viable approach for implementing parametric BIST [1]. The standard approach to production test of analog and mixed-signal devices is depicted in Fig. 1.

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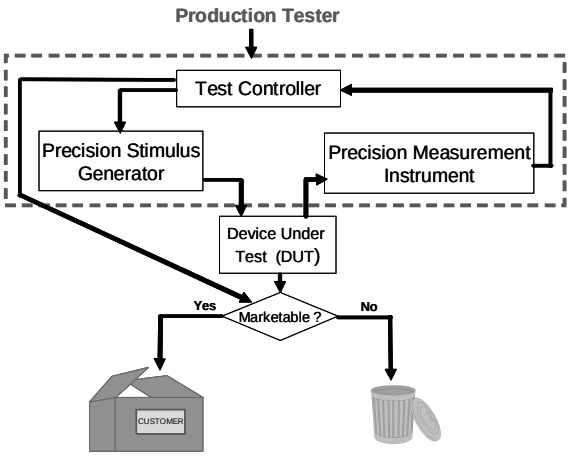


Fig. 1. A standard approach to analog and mixed-signal production test

As shown in the figure, in a typical production test environment a test controller controls the signal generator that is responsible for generating precise input stimuli for the DUT. The test controller also controls a measurement instrument that monitors and captures the DUT response. The measured results are then used by the test controller to evaluate the various performance parameters of the DUT. The device passes the test and becomes marketable only if the measured response is within a predetermined acceptable performance window. An implicit assumption that is often made is that both the stimulus generator and the measurement instrument are sufficiently more precise than the DUT and that most differences between the expected and measured output of the DUT are due to the device. However, this places stringent requirements on the design of the signal generator and the measurement instrument.

The challenges associated with parametric production test can be attributed to primarily three factors. The first is the cost associated with the test and that is determined primarily by the direct testing cost in terms of the time the device spends on the tester and the indirect testing cost associated with the investment on the tester itself. The second is the availability of sufficiently precise stimulus generators and measurement systems. Invariably test engineers strive to use test equipment with performance that is a decade better, or even more, than the performance of the DUT. Although many mixed-signal parts are designed for performance that is well below the state of the art in tester technology, many high-end mixed-signal ICs have performance requirements that are approaching those of the best commercial test equipment or, in some cases, the performance requirements may actually lead that available from the test equipment manufacturers. The third is in the de-embedding of the DUT for testing. Often the tester will present a load to a mixed-signal circuit, particularly when the DUT is embedded in a

System-on-a-Chip (SoC) -scale circuit that is much different from what the circuit will experience in normal operation. This change in loading conditions may result in varied performance of the device and wrong interpretation of the device performance. It is important that the tester loading does not mask or alter the actual performance metrics of the DUT.

This has resulted in a slow movement towards Built-In Self-Test structures for mixed-signal circuits. Many approaches to parametric BIST have been proposed in the literature [1, 5-8]. Most of these structures are based upon the basic flow depicted in Fig. 2.

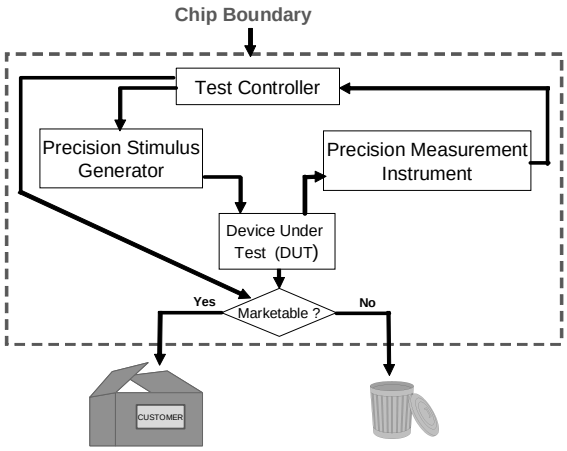


Fig. 2. A standard approach to BIST for mixed-signal circuits

The big distinction between the BIST approach and the production test approach is in the inclusion of the stimulus generator and the measurement system on the chip along with the DUT. This step is a natural extension of the parametric production test environment and is particularly attractive considering the fact that the same type of testing algorithms that are used on production testers can be adopted in the BIST flow. Invariably the major research challenge with this approach is on achieving an acceptable level of precision in the stimulus generators and in the measurement systems.

The most widely used mixed-signal component is analog-to-digital converters (ADCs). In the arena of ADCs, a widely used input stimulus for linearity estimation of the device is a ramp signal. Considerable research has been done towards generation of precise ramp signals on-chip for linearity testing. In [5] the authors reported simulation results for linearity of a ramp-generator that is capable of producing 11-bit linear signal. (For a continuous ramp signal, “n-bit linearity” means the difference between the actual signal and an ideal signal is in the range of $1/2^{n+1}$ to $1/2^{n}$ of the total signal swing.) A Sigma-Delta modulator was used to generate a bit stream that feeds a low pass filter to produce the linear ramp signal used in [6]. With a bit stream of 2^{14} bit in length, reported

simulation results indicate that an 8-bit ADC can be tested to 5% LSB accuracy. A cascaded current-source ramp generator was used in [7] to obtain reported simulation results with sufficient linearity to test 14-bit ADCs. More recently the authors of [8] reported a current-source based ramp generator with experimentally verified linearity at the 15-bit level. However, with an increasing demand on the performance of the signal generator, it can be seen that the challenge of building these blocks on chip is often bigger than the challenge of building the DUT itself. Furthermore, the silicon area overhead for achieving this level of performance can be unacceptably large. For these reasons, there is minimal industrial adoption of BIST for most analog and mixed-signal functions, leaving BIST for ADCs however an open problem at essentially all resolution and speed levels.

With little success in the research community at developing viable techniques for parametric BIST, production parametric testing costs have become a rapidly growing and increasingly significant portion of the overall manufacturing costs of mixed-signal circuits. Parametric ADC testing, in particular, has become very challenging and costly. Production testing of low to medium resolution ADCs, 12 bits and below, at low and medium frequencies, has become known art but major testing challenges remain for 16 bits and above while 13 to 15 bit ADCs can be considered borderline in terms of test capability and test cost on today's production testers. Testing of ADCs at the 10-12 bit level that are used in communication circuits is still a challenge due to the high clock rates and the high-speed stimulus and low clock jitter requirements.

Production test costs for high resolution ADCs, 16 bits or above, are determined primarily by the resolution of the ADC, and not by the sampling rate. In existing production test environments, as the number of codes increases, the linearity requirement of the source driving the ADC increases. This performance requirement necessitates the use of slow, high-precision signal generator architectures that require long settling times, thereby increasing the overall test time and the associated test cost. Even if the sampling rate of the ADC is of the order of tens of megahertz, the ADC has to wait for the source to settle before a sample can be taken. For example, testing a 16 bit ADC using a 20-bit delta-sigma DAC with a 1 mS settling time and 10 steps per code will require approximately 11 minutes of time on a tester to test all the codes of the ADC for a single temperature. For 3 temperature tests, the test time can exceed half an hour for a single ADC. The cost of performing an all-codes test on a high performance mixed-signal tester for a 16-bit part can exceed $30 per ADC based on a rate of $1/minute for the tester cost. These prohibitively high test costs are generally considered unacceptable to the industry.

In addition to the high test costs, the testing itself becomes more challenging because of 'voltage drift' in the tester. Although state of the art test equipment may have a stationary effective reference voltage over short time intervals, it will drift significantly over test times of a few minutes with a drift of several hundred microvolts over a 10 minute interval being common. This nonstationarity of the source must be managed with more complicated testing algorithms if long test times become necessary.

Due to cost constraints, ADC manufacturers have chosen to do "reduced code testing" using servo-loop techniques to dramatically reduce test times at the expense of a corresponding dramatic reduction in the test coverage. Reduced code testing techniques are only useful for ADC architectures that can be fully characterized by reduced codes, such as the SAR architecture. However, even for the SAR architecture, the non-linearity of the Sample-and-Hold (S/H) circuit cannot be fully characterized by reduced code testing. And, unfortunately, servo-loop methods cannot guarantee nonexistence of missing code.

From the discussions above, it is clear that the reliance on high-precision stimulus signals is critically hampering, or preventing, adequate testing of ADCs in both production test and BIST, because of a) the technical difficulties in generating the precision signals and the cost (design effort, manufacturing cost, or capital investment) associated with such signal generators, b) the long testing time imposed by the settling requirements of such signals and the associated testing cost, and c) the difficulties in testing in terms of maintaining a sufficiently stationary testing environment over the long testing time. In this paper, we introduce a new approach to analog and mixed-signal testing based upon using imprecise excitations and imprecise measurements. Our goal is to eliminate the need of highly precise input signals or highly precise measurement devices, and hence eliminate all the technical difficulties and cost factors associated with such precision inputs and measurements, thus providing an enabling technology for cost-effective analog and mixed signal (AMS) production test and BIST. As a proof of concept, the technique is applied to the testing of ADCs. With the proposed approach, the performance requirements of the stimulus generator can be dramatically reduced. In particular, a highly non-linear but short-time stationary source, such as what can be readily realized either on-chip or in a production test environment with a resistor string DAC, is used to test the linearity of an ADC.

2. TESTING WITH IMPRECISE STIMULUS AND MEASUREMENT

A standard test flow for parametric mixed-signal testing is shown in Fig. 3. X_{IN} is a known input digital signal and X_{OUT} is the observed output digital signal. These signals

serve as test vectors for the mixed-signal test. The internal signals X_F and X_U can be either analog signals or digital signals depending on the DUT, but generally at least one of them is analog. If X_F is a digital signal, the stimulus block is unnecessary and can be eliminated. If X_U is a digital signal, the measurement block can be eliminated.

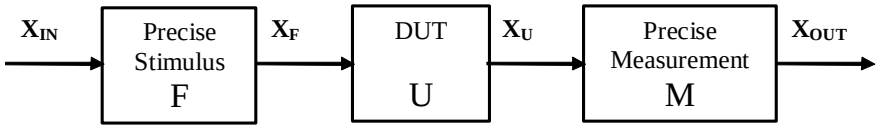


Fig. 3. A standard test flow to parametric mixed-signal test

For example, when testing the low frequency spectral characteristics of an ADC, the measurement block can be eliminated and the digital output of the ADC, X_U, is the final output. When testing the low frequency spectral characteristics of a DAC, the stimulus block is not required and the input to the DAC, $X_{F,}$ is the original input. In the above figure, functions F, U and M represents the transfer characteristics of the Stimulus, DUT and Measurement blocks, respectively. For most DUTs, the goal in parametric testing is to define a test so that the transfer characteristic U can be used to determine the performance parameters of interest. Mathematically, the relationship between the test vectors X_{OUT} and X_{IN} can be expressed as

$$X_{OUT} = M(U(F(X_{IN}))) + N(X_{IN}) \quad (1)$$

where N is a noise function in the measurement. If M and F are known, for an effective test, sufficient information will exist in the vectors X_{IN} and X_{OUT} to determine U. The computational complexity, the size of the vectors X_{IN} and $X_{OUT,}$ and ultimately the test time and test costs needed to determine U are strongly dependent upon the nature of F and M and on the noise N. If M and F are the identity functions, then the computational effort and the size of the vectors X_{IN} and X_{OUT} are often quite attractive. But even in this situation, the total time required on the tester may be unacceptably long for some useful functions. In most production tests, a precise stimulus is applied and precise measurements are made so that it can be assumed that F and M are known. The importance of using a precise stimulus and making precise measurements when developing a test flow depicted in Fig. 3 is apparent, whether in a production test or a BIST environment.

An alternative test flow based upon using imprecise stimulus and imprecise measurements is depicted in Fig. 4. In contrast to the standard test flow of Fig. 3, the alternative test flow uses multiple imprecise excitations and correspondingly has multiple imprecise measurements.

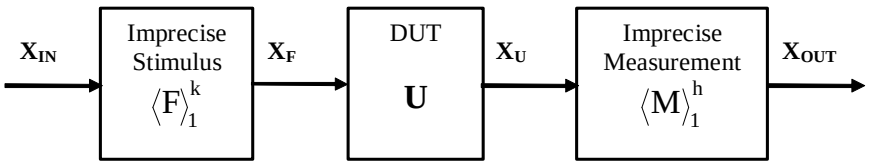


Fig. 4. An alternative test flow based upon imprecise stimulus and imprecise measurement

As shown in the figure, it is assumed that there are k imprecise stimuli presented to the DUT and there are h imprecise measurements. If all h imprecise measurements are made for each imprecise excitation, a set of input and output test vectors are obtained for each stimulus-measurement combination. Mathematically, the resultant family of test vectors can be expressed as

$$X_{OUT(i,j)} = M_i(U(F_j(X_{IN(i,j)}))) + N(X_{IN(i,j)}) \quad for 1 \le i \le h, 1 \le j \le k \quad (2)$$

The immediate question that needs to be addressed is whether sufficient information exists in the resultant family of test vectors to uniquely determine U. The answer to this question depends strongly on the nature of the sequences of stimulus and measurement functions. We will show by an example later in this paper that sufficient information does exist for testing ADCs with one class of imprecise stimuli. There are many other classes of stimulus and measurement functions that will provide sufficient information to uniquely determine U as well. At this point it may appear by comparing equation (2) to (1) in the case where F and M are assumed known that even if sufficient information is available for determining U with the alternative test flow, a large number of measurements must be made and a large amount of computation time will be required to determine U, both undesirable if attempts are made to practically use this approach in either a production test or BIST environment. However, since imprecise stimuli and imprecise measurements are allowed in equation (2), the settling time for each measurement point could be reduced by a factor of thousands or tens of thousands. For example, if a sigma-delta DAC signal generator with a settling time of 1 mS is replaced by a simple analog ramp generator using a current source charging a capacitor, the measurement time for each sample in a 10 MSPS ADC testing will be limited by the clock rate of 10 MSPS, representing a factor of 10,000 speedup. Therefore the total measurement time implied in equation (2) can still be thousands of times less than that in equation (1). Furthermore, the computational time is typically insignificant as compared to data acquisition time for high performance ADC testing and could be pipelined so that it does not add to the total testing time at all.

In what follows, a proof of concept will be presented based upon using imprecise stimuli to test ADCs. The performance of this approach will be supported by computer

simulations and measured results obtained from a production test environment. The ADC example shows that both the number of measurements and the number of arithmetic manipulations needed are manageable. Preliminary results of algorithms using this idea are presented in authors' earlier works [9-11, 13, 14].

3. TRADITIONAL ADC LINEARITY TESTING

The test flow that is generally used for ADC testing is shown in Fig. 5. Since the output of an ADC is a digital signal, the measurement block depicted in Fig. 3 is not required.

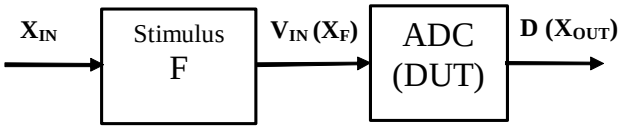


Fig. 5. Experimental setup for ADC testing

Ideally, an ADC transforms an analog input voltage (or current), V_{IN}, to a digital code, D. The static performance of an ADC can be mathematically characterized by a set of distinct and monotonically increasing voltages T_0, T_1…, T_{N-3}, T_{N-2}, called transition points together with the associated digital output codes D_0, D_1 …, D_{N-2}, D_{N-1}. N is the total number of decision levels of an ADC and is related to the resolution of the ADC, n, by the following expression.

$$N = 2^n \tag{3}$$

The dc transfer characteristics of the ADC are given by the expression

$$D = \begin{cases} D_0, & V_{IN} \le T_0 \\ D_i, & T_{i-1} < V_{IN} \le T_i \\ D_{N-1}, & T_{N-2} < V_{IN} \end{cases} \qquad i = 1, 2..., N-2 \tag{4}$$

In what follows it will be assumed that the ADC is monotonic and increasing so that

$$D_i < D_{i+1}, \qquad i = 0, 1, 2..., N-1 \tag{5}$$

Several different definitions of linearity for ADCs are used in the industry. In this work, the linearity will be defined relative to an end-point fit line over the input voltage range between the first transition point T_0 and the last transition point T_{N-2}. The end-point fit line transition points I_k are defined by the linear equation

$$I_k = T_0 + k\frac{T_{N-2} - T_0}{N-2} = T_0 + k \times \bar{I}, \qquad k = 0, 1, 2..., N-2 \tag{6}$$

The ideal spacing between two adjacent end-point fit line transition points is called a Least Significant Bit (LSB) and is defined by the expression

$$1LSB = \bar{I} = (T_{N-2} - T_0)/(N-2) \tag{7}$$

The actual transfer characteristic given in (4), the end-point fit line defined by (6) and the end-point fit line transfer characteristic are plotted in Fig. 6.

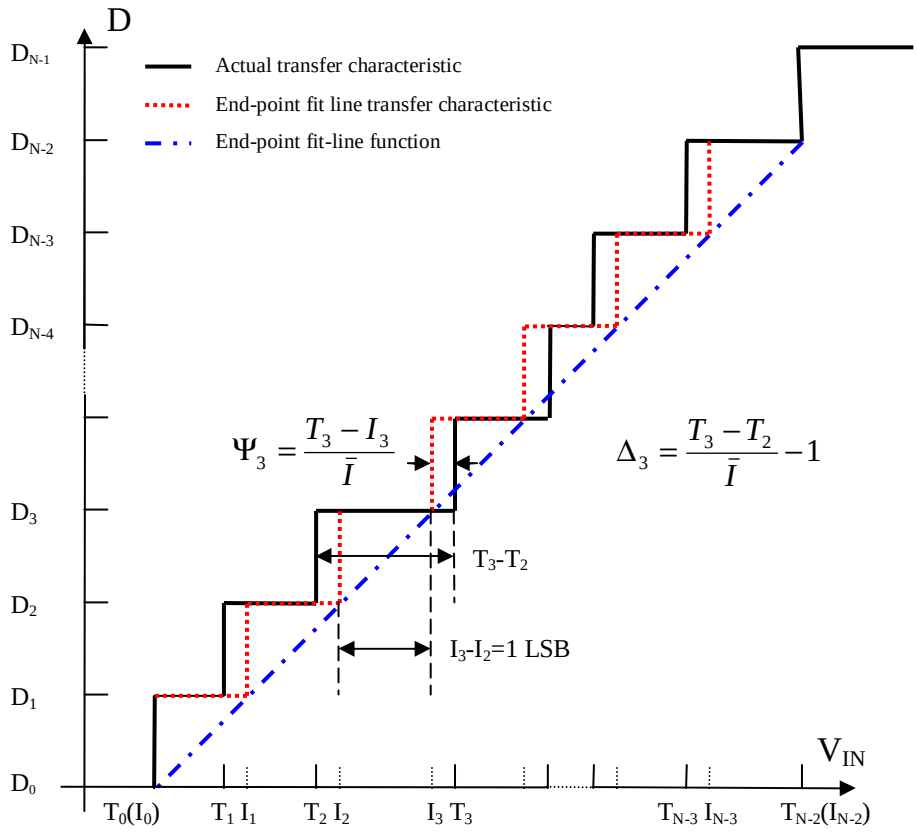


Fig. 6. Transfer Characteristics and the end-point fit line function of an ADC

The relative deviation of the code width of code k, T_k-T_{k-1}, from 1 LSB, the ideal code width for every code, is called the differential nonlinearity of code k and is defined as

$$\Delta_k = \frac{(T_k - T_{k-1}) - \bar{I}}{\bar{I}} = (N-2)\frac{T_k - T_{k-1}}{T_{N-2} - T_0} - 1, \quad k = 1, 2..., N-2 \qquad (8)$$

The difference between the actual transition point T_k and the end-point fit line transition point I_k in LSB is called the integral nonlinearity of code k and is given by

$$\Psi_k = \frac{T_k - I_k}{\bar{I}} = (N-2)\frac{T_k - T_0}{T_{N-2} - T_0} - k, \quad k = 0, 1, 2, ..., N-2 \qquad (9)$$

The INL and DNL of an ADC are defined respectively by

$$INL = \max_k |\Psi_k| \qquad (10)$$

$$DNL = \max_k |\Delta_k| \qquad (11)$$

Since the end-point fit line goes through the first and last transition points, it follows that the first and last integral nonlinearities are 0.

$$\Psi_0 = \Psi_{N-2} = 0 \tag{12}$$

Also from (8) and (9) it can be seen that

$$\Delta_k = \Psi_k - \Psi_{k-1}, \qquad k = 1, 2..., N-2 \tag{13a}$$

$$\Psi_k = \sum_{i=1}^{k} \Delta_i, \qquad k = 1, 2..., N-2 \tag{13b}$$

The relationship between these quantities is also shown in Fig. 6. In a production test environment, the purpose of ADC linearity test is to ensure that the actual INL and DNL are within the range specified by the product performance specifications. This is generally approached by identifying all the values of Ψ_k and then calculating INL and DNL from (10)-(13).

The histogram method is a widely accepted industry standard for testing the INL and DNL performance of an ADC. In this method, a linear ramp signal with accuracy much higher than the target performance of the ADC is presented as the input to the ADC under test. As the input is ramped up, samples uniformly spaced in time are taken and the output codes of the ADC are tallied into a histogram $\{C_k$, k= 0, 1, 2, …, N-1$\}$ where C_k is the number of occurrence of the output code D_k. If V_{IN} is an ideal linear ramp stimulus with slope η as assumed in standard ADC test, then the stimulus can be expressed as,

$$V_{IN} = \eta t \tag{14}$$

With this excitation, the output code will be D_k if $V_{IN} \in (T_{k-1}, T_k]$. Hence, C_k, which is the number of hits of D_k, will be equal to the number of sampling instants that $V_{IN} \in (T_{k-1}, T_k]$. Since V_{IN} is incremented by ηT_{SAMP}, we have

$$C_k \cong \frac{T_k - T_{k-1}}{\eta T_{SAMP}}, \qquad k = 1, 2..., N-2 \tag{15}$$

where T_{SAMP} is the sampling period of the ADC. This is an approximation subject to time-domain quantization errors since the right hand side of (15) need not always be an integer. The error is small if C_k is large. Furthermore, the quantization errors do not accumulate with k. The number of samples per 1 LSB will be $\overline{C} = \bar{I} / (\eta T_{SAMP})$. It can be easily verified that

$$\overline{C} = \sum_{i=1}^{N-2} C_i \Big/ (N-2) \tag{16}$$

Note that the number above is not necessarily an integer. It follows from equations (8) and (9) that the integral and differential nonlinearities of the ADC can be obtained from the histogram data as given by

$$\Delta_{k,est} = \frac{C_k}{\overline{C}} - 1 \tag{17}$$

$$\Psi_{k,est} = \sum_{i=1}^{k} \left(C_i / \overline{C} \right) - k \tag{18}$$

The INL and DNL estimated using (17) and (18) are very close to the actual value if the stimulus is perfectly linear, except for the quantization error due to the integer number of hits. If there are many samples per code on average, this error is much less than 1 LSB and can be neglected.

However, if V_{IN} is not a perfect linear ramp, the standard histogram method may lead to a wrong estimation of INL and DNL for an ADC. Assume the actual V_{IN} is a smooth, monotonically increasing but nonlinear function of time

$$V_{in} = f(t) = \eta t + F(t) \tag{19}$$

where ηt is the linear fit line connecting the first and last transition points, and $F(t)$ is the nonlinear component. The time points when V_{IN} crosses transition points T_{k-1} and T_k are $t_{k-1}=f^{-1}(T_{k-1})$ and $t_k=f^{-1}(T_k)$, respectively. When $t_{k-1} < t < t_k$, it follows that $T_{k-1} < V_{IN} < T_k$ and thus the output code will be D_k. Hence the code tally for code D_k, denoted as C'_k, can be related to the crossing time defined above and the sampling clock period by the following equation

$$C'_k = \frac{t_k - t_{k-1}}{T_{SAMP}} \tag{20}$$

By definition, ηt is the endpoint fit line, so $T_0=\eta t_0$, $T_{N-2}=\eta t_{N-2}$, and $F(t_0)=F(t_{N-2})=0$. Still using the standard histogram method (16)-(18), we have

$$\Delta'_{k,est} = \frac{C'_k}{\overline{C'}} - 1 \cong (N-2)\frac{\eta(t_k - t_{k-1})}{T_{N-2} - T_0} - 1 \tag{21}$$

$$\Psi'_{k,est} = \sum_{i=1}^{k} \left(C'_i / \overline{C'} \right) - k \cong (N-2)\frac{\eta(t_k - t_0)}{T_{N-2} - T_0} - k \tag{22}$$

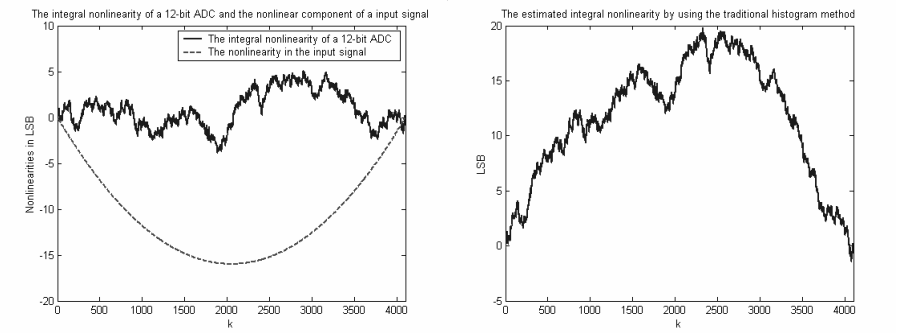
The estimated integral and differential nonlinearity above are also affected by the quantization error, so approximately equal signs are used. Comparing these estimations to

the actual value as in (8) and (9), we can see that there are errors introduced by the nonlinearity in the input signal as follows.

$$\Delta'_{k,est} = \Delta_k + (N-2)\left[\frac{\eta(t_k - t_{k-1})}{T_{N-2} - T_0} - \frac{T_k - T_{k-1}}{T_{N-2} - T_0}\right] = \Delta_k + \frac{F(t_{k-1}) - F(t_k)}{\bar{I}} \quad (23)$$

$$\Psi'_{k,est} = \Psi_k + (N-2)\left[\frac{\eta(t_k - t_0)}{T_{N-2} - T_0} - \frac{T_k - T_0}{T_{N-2} - T_0}\right] = \Psi_k - \frac{F(t_k)}{\bar{I}} \quad (24)$$

From equations (23) and (24) we can see that the nonlinearity in the input will be directly transformed into errors in the estimated integral and differential nonlinearities if the traditional method is used. Simulations are done to test a 12-bit ADC by using a nonlinear input signal. The actual integral nonlinearity of the ADC and the nonlinear component in the input signal are shown in Fig. 7 (a). The estimated integral nonlinearity by using the traditional method is plotted in Fig. 7 (b). It is exactly the summation of the actual integral nonlinearity and negative of the input nonlinearity in LSB, as predicted by (24). If the summation is plotted on Fig. 7 (b) as well, the two curves will overlap each other exactly.



(a) (b)

Fig. 7. The error of the traditional histogram method using a nonlinear input signal
(a) The integral nonlinearity of a 12-bit ADC and the nonlinearity in the input signal
(b) Estimated integral nonlinearity using the traditional histogram method

This input-introduced error will have a significant effect on the estimation of INL and DNL for a high resolution ADC. Since existing production test or BIST solution does not explicitly handle this error component, the INL and DNL estimation results will be different from the actual values if the input-introduced error is not much less than 1 LSB. Therefore, the input signal is required to be much more linear than the ADC. However, the issue of generating sufficiently linear excitation to keep the error terms in (23) and (24) at an acceptably small level for a high resolution ADC is challenging. Usually it requires longer time to generate more linear signals, resulting in an increased test cost.

Whether in a production test environment or a BIST environment, the cost of generating a sufficiently linear stimulus for INL and DNL testing of a high resolution ADC is very high. In the following section the issue of linearity testing with imprecise stimulus will be addressed.

4. ADC TESTING WITH LOW ACCURACY STIMULI

As explained in previous sections, generation of very precise ramp signal with little extra hardware is a daunting task beyond a certain limit. The concern then is whether an ADC can be accurately tested using low linearity signals. In section II the idea of characterizing an ADC with multiple imprecise inputs was introduced. In this section we propose a new ADC testing method using two input signals $V_{IN}^{(1)}$ and $V_{IN}^{(2)}$. The two signals can be highly nonlinear. The algorithm exploits the relationship between the two signals while estimating the INL and DNL of an ADC without being affected by input-introduced errors.

4.1 A new histogram based ADC testing method

In the proposed algorithm, two nonlinear ramp signals are used, with the second being a constant-shifted version of the first. The input signal is assumed to be a strictly increasing function of time and the speed at which the signal increases does not change dramatically. Furthermore, we assume that the signal generator is short-time stationary, meaning that if the same signal is regenerated within a short time period, the regenerated signal should be very close to the original signal, with the maximum difference much smaller than 1 LSB. Except for these reasonable and easy-to-satisfy conditions, the stimulus signals are allowed to be imprecise. The signal could have a significant error from what it is supposed to be, an ideal ramp in this case. Furthermore, the error is unknown to the design engineers or test engineers. It is uncertain in the sense that it is process and environment dependent. This significantly relaxes the requirement on the signal generator so that it can be easily implemented with low cost or on chip.

Fig. 8 is used to illustrate the basic idea of the proposed algorithm. The vertical axis is marked with the actual and the end-point fit-line transition points of the ADC, respectively. The two nonlinear curves represent the two ramp-like signals. Mathematically, the two nonlinear signals can be described by

$$V_{IN}^{(1)} = f(t) \tag{25}$$

$$V_{IN}^{(2)} = f(t) - \alpha \tag{26}$$

where α is the constant shift between the two signals.

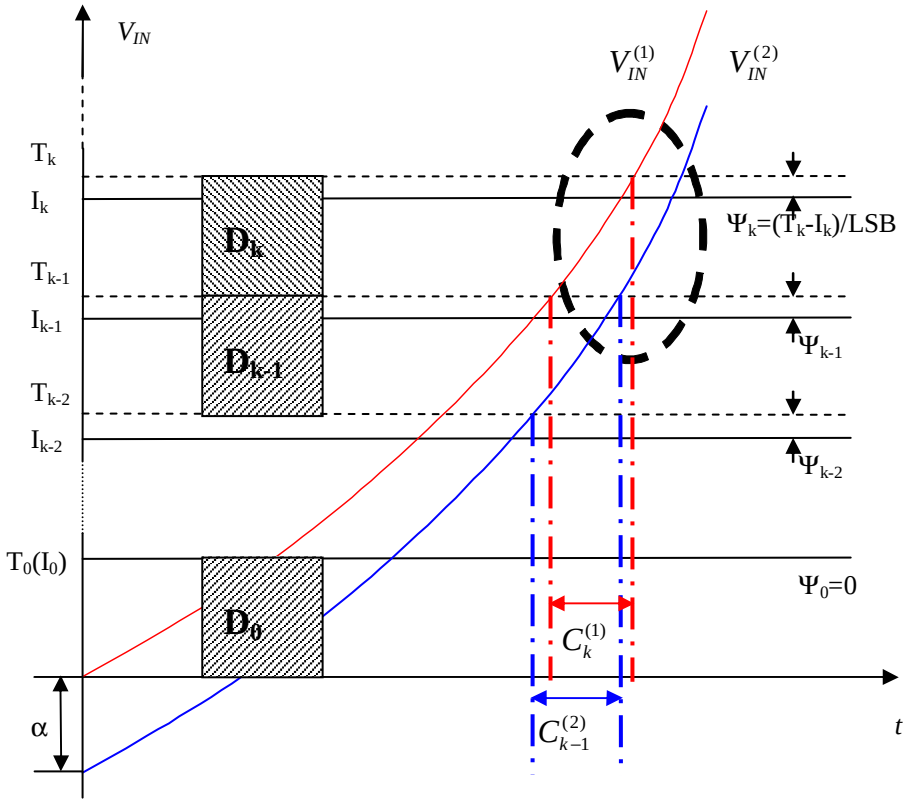


Fig. 8. Ramp testing for an ADC using two nonlinear inputs

The tallies of codes obtained when $V_{IN}^{(1)}$ and $V_{IN}^{(2)}$ are presented as the ADC input signals are $C_k^{(1)}$ and $C_k^{(2)}$, respectively. The amount of shift α between the two signals is unknown and not measurable externally and needs to be estimated as an additional variable. Assuming the signals are sampled uniformly in time with a sampling period T_{SAMP}, the time index when the value of the signal $V_{IN}^{(1)}$ (or $V_{IN}^{(2)}$) crosses transition level T_k, measured in units of sampling period T_{SAMP}, is $\sum C_k^{(1)}$ (or $\sum C_k^{(2)}$, respectively). And this relationship is subject to time quantization errors. That is

$$T_k / \bar{I} = I_k / \bar{I} + \Psi_k \cong f\left(\sum_{i=0}^{k} C_i^{(1)}\right), \qquad k = 0,1,2...,N-2 \tag{27}$$

$$T_k / \bar{I} = I_k / \bar{I} + \Psi_k \cong f\left(\sum_{i=0}^{k} C_i^{(2)}\right) - \alpha, k = 0,1,2...,N-2 \tag{28}$$

To simplify the analysis, we will consider the system to be noiseless. The effects of noise and errors will be discussed later. Subtracting the (k-1)th equation in (28) from the kth equation in (27) yields:

$$1+\Psi_k-\Psi_{k-1}=f\left(\sum_{i=0}^{k}C_i^{(1)}\right)-f\left(\sum_{i=0}^{k-1}C_i^{(2)}\right)+\alpha, \qquad k=1,2...,N-2 \qquad (29)$$

Expressions in the equation above are given in LSB. On the left hand side of (29) is the code width T_k-T_{k-1} measured in LSB corresponding to code D_k. On the right hand side is the code width expressed as a function of the summation of tallies. The difference between the first two terms on the right hand side of (29) can be written as

$$f\left(\sum_{i=0}^{k}C_i^{(1)}\right)-f\left(\sum_{i=0}^{k-1}C_i^{(2)}\right)=f'(\xi_k)\left(\sum_{i=0}^{k}C_i^{(1)}-\sum_{i=0}^{k-1}C_i^{(2)}\right), \qquad k=1,2...,N-2 \quad (30)$$

where $f'(\xi_k)$ is an unknown variable, because the exact function form of the input signal is unknown. Though we use the notation of derivative in the expression, its physical meaning is simply the slope of a section of the nonlinear function $f(t)$ between $f(t)=T_k$ and $f(t)=T_{k-1}+\alpha$. Refer to Fig. 9.

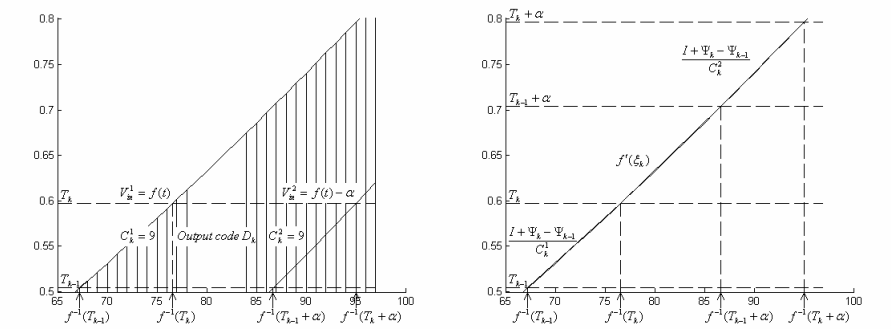


Fig. 9. Slope approximation for the nonlinear signal

There are different ways to approximate the slope. In this work, we use a simple approximation for this slope by averaging the slopes of $V_{IN}^{(1)}$ and $V_{IN}^{(2)}$ over the interval between T_{k-1} and T_k as shown in (31)

$$f'(\xi_k)\cong\frac{1}{2}\left(\frac{1+\Psi_k-\Psi_{k-1}}{C_k^{(1)}}+\frac{1+\Psi_k-\Psi_{k-1}}{C_k^{(2)}}\right),\ k=1,2,...,N-2 \qquad (31)$$

If the nonlinearity in the input has a form of a second order polynomial, the approximation in equation (31) is actually exact. The effects of the slope approximation

will be further discussed later. Substituting (30) and (31) into equation (29) and rearranging leads to

$$1 = \frac{\alpha}{1-\gamma_k} + \Psi_{k-1} - \Psi_k, k = 1,2,...,N-2 \tag{32}$$

where $\gamma_k = \frac{1}{2}\left(\frac{1}{C_k^{(1)}} + \frac{1}{C_k^{(2)}}\right)\left(\sum_{i=0}^{k} C_i^{(1)} - \sum_{i=0}^{k-1} C_i^{(2)}\right)$. Equation (32) is a set of linear equations with respect to unknown variables α and $\Psi_k, k = 1,2,...,N-3$. Many standard mathematical methods can solve this type of equation set. Some of them have a computational complexity proportional to $(N-2)^3$. For high resolution ADCs, N is very large and these methods will take a prohibitively long time to get the results. We propose a method with a computational complexity only proportional to N-2. Notice that by adding all equations in (32), the $-\Psi_k$ term of one equation will cancel the Ψ_k term of the next equation and we have $N-2 = \alpha\sum_{i=1}^{N-2}\frac{1}{1-\gamma_i} + \Psi_0 - \Psi_{N-2}$. Using the fact $\Psi_0 = \Psi_{N-2} = 0$ as described in equation (12), we get an estimation of the shift between the two stimuli

$$\alpha_{est} = (N-2)\Big/\sum_{i=1}^{N-2}\frac{1}{1-\gamma_i} \tag{33}$$

Substituting the value of α into equation (32), we can estimate the integral nonlinearity of the ADC as

$$\Psi_{k,est} = \left(\sum_{i=1}^{k}\frac{1}{1-\gamma_i}\right)\alpha_{est} - k, \quad k = 1,2...,N-3 \tag{34}$$

Based on the estimated value of integral nonlinearity, we can calculate the differential nonlinearity of the ADC and further get the INL and DNL parameters as defined in (10) and (11).

4.2 The ADC identification algorithm using low accuracy stimuli

The method discussed above can be summarized as an algorithm with the following steps.

1. Use a signal $V_{IN}^{(1)}$ to excite the ADC under test and collect the histogram $\{C_k^{(1)}, k = 0,1,...,N-1\}$.

2. Regenerate the signal $V_{IN}^{(1)}$ but shift it by a constant voltage α to obtain $V_{IN}^{(2)}$.

3. Use the signal $V_{IN}^{(2)}$ to excite the ADC under test and collect the histogram $\{C_k^{(2)}, k = 0,1,...,N-1\}$.

4. Calculate $\gamma_k = \frac{1}{2}\left(\frac{1}{C_k^{(1)}} + \frac{1}{C_k^{(2)}}\right)\left(\sum_{i=0}^{k} C_i^{(1)} - \sum_{i=0}^{k-1} C_i^{(2)}\right), k = 1,2,...,N-2$.

5. Calculate $\alpha_{est} = (N-2)\Big/\sum_{i=1}^{N-2}\frac{1}{1-\gamma_i}$.

6. Calculate $\Psi_{k,est} = \left(\sum_{i=1}^{k}\frac{1}{1-\gamma_i}\right)\alpha_{est} - k, \quad k = 1,2,...,N-3$.

7. Calculate $\Delta_{k,est} = \frac{\alpha}{1-\gamma_k} - 1, \quad k = 1,2,...,N-2$.

8. $INL_{est} = \max_k\{|\Psi_{k,est}|\}$ and $DNL_{est} = \max_k\{|\Delta_{k,est}|\}$.

The input signals can be generated very fast. It is not necessary to wait until the stimulus settles because they are not required to be linear. So test time of an ADC can be dramatically reduced. The histogram data collection in step 1 and 3 is the same as that for the traditional ADC linearity test. The voltage shift in step 2 is simply an analog addition and can be realized in hardware. Steps 4, 5 and 6 can be done by either a computer or on-chip DSP functionality. Since the partial sums in steps 4 and 6 can be generated in one run and used for each k, the total computational complexity in steps 4-8 is actually proportional to (N-2), not the seemingly $(N-2)^2$. This is the same order of computational complexity as the traditional method and therefore will not add significant processing time to the overall test time. Typically, the computational time for the traditional histogram method is less than the data acquisition time and can be pipelined in production test so that it does not contribute to the overall test time. We believe this will also be the case for the proposed algorithm.

5. PERFORMANCE ANALYSIS

The proposed algorithm has the capability to test an ADC using low accuracy input signals and estimate the integral and differential nonlinearities of the ADC to higher accuracies than that of the stimuli, which is inherently not doable for the traditional histogram method. So the proposed algorithm has wider applications for low cost

production test and mixed signal BIST, where high accuracy input signals are too expensive to build or too challenging to design.

5.1 Comparison of the proposed algorithm to the traditional histogram method

The traditional histogram method will directly transform the nonlinear error in input signals into the error in estimation of integral and differential nonlinearities as given in (23) and (24). To estimate the INL and DNL of an ADC to accuracy of 0.1 LSB, the input signal must be a decade more linear than the ADC so that the input nonlinearity is less than 0.1 LSB. This is the common knowledge that to test an n-bit ADC, the input signal should be more than (n+3)-bit linear. Furthermore, because of noise errors, even with an (n+3)-bit linear input, accuracy of 0.1 LSB is usually not achievable. Including the noise effect, a reasonable error bound for ADC production test in the industry is half LSB. The proposed algorithm significantly relaxed the requirement on input stimuli. Input signals used in the proposed algorithm can be 6-7 bits less linear than the ADC, as shown in our experimental test results. Using the traditional histogram method, there would be hundreds of LSBs error in INL estimation. The proposed algorithm can eliminate the effect of the huge input nonlinearity and estimate the INL to an error less than 0.8 LSB as we will talk about in experimental results shortly. The proposed algorithm can do the INL and DNL test for an n-bit ADC by using only (n-7)-bit linear signals and has the performance comparable to that of the traditional histogram method which requires (n+3)-bit linear input signals.

5.2 Effects of slope approximation

Two major factors contribute to the error in the proposed algorithm. The first is the error associated with the slope approximation using the average in (31). The second is the error in $C_k^{(1)}$ and $C_k^{(2)}$ measurement. We will talk about each of them as follows.

In the proposed algorithm, we were required to estimate the slope of the nonlinear input function over the interval between $\Sigma C_k^{(1)}$ and $\Sigma C_{k-1}^{(2)}$. (Refer to equation (30)). This slope strongly depends on the nature of the unknown nonlinear input signal function. There are many ways to do the estimation and without the knowledge of the input, no one method can be said to be more accurate than the other. Therefore we use the average of slopes at two end-points of the interval, $\Sigma C_k^{(1)}$ and $\Sigma C_{k-1}^{(2)}$, to approximate the required slope factor in equation (31). Although not very precise, this approximation gives us a simple calculation towards INL estimation. If the nonlinear function representing the

input is a second order polynomial, then the above estimate gives the exact value of the slope. Let's assume that the input is of the general form given by

$$f(t) = at^2 + bt \tag{35}$$

The slope of the input signal over the interval between t_1 and t_2 is given by

$$\frac{f(t_2) - f(t_1)}{t_2 - t_1} = a(t_2 + t_1) + b \tag{36}$$

On the other hand, if we use derivatives at t_1 and t_2 and obtain their average, we will have

$$\frac{f'(t_2) + f'(t_1)}{2} = \frac{2at_2 + b + 2at_1 + b}{2} = a(t_2 + t_1) + b \tag{37}$$

We can see that the slope and the average are exactly the same. This corroborates the fact that if the nonlinear input is mainly in the shape of a second order polynomial, our slope approximation will not introduce major errors in INL and DNL parameter estimation. More generally, if the nonlinear error in the input signal is dominantly of low order terms, the slope approximation of equation (31) will work well. In the unlikely case when the input signal nonlinearity has significant high frequency components, the proposed method will introduce additional error. Since low frequency smooth signals are easy to guarantee (by simple low pass filtering), such cases are of no interest to ADC testing.

5.3 Error in histogram measurement

The histogram data, $C_k^{(1)}$ and $C_k^{(2)}$, are mainly affected by the additive noise at the input of the ADC. Let us assume that the additive noise is stationary with mean 0 and variance σ^2. The noise may result in a different output code from the expected value and larger variance makes the code more likely to be different from its expected value. For instance, if we consider the accumulated histogram, $\Sigma C_k^{(1)}$, which is the number of codes less than or equal to code k. In the traditional histogram method, this number is the estimated value of the k^{th} transition point except for a constant scaling factor and an offset. Similarly in the proposed algorithm, this number gives the first order approximation of the k^{th} transition point. But any error in this number will translate into an error in the integral nonlinearity estimation and finally into an error in INL and DNL estimation. However, since there are many samples for each code, an addition or subtraction of one or two sample will not have a significant effect on the total number of samples for a code. Intuitively, the variance of $\Sigma C_k^{(1)}$ may increase as the variance of the additive noise increases. With detailed analysis, we can show that the following relationship is true.

$$\sigma_N^2\{\Sigma C_k^{(1)}\} = B_1 \frac{\sigma}{N_S} \tag{38}$$

where N_S is the averaged sample density. The subscript N signifies that the variance of $\Sigma C_k^{(1)}$ is due to additive noise. Equation (38) states that the variance of the accumulated histogram is proportional to the standard deviation of the additive noise, where B_1 is a coefficient dependent on the distribution of the noise. When the noise becomes large, the uncertainty in the accumulated histogram data will also increase, but at a speed slower than that of the noise. This implies that the error in INL and DNL estimation will not increase as fast as the noise.

The time domain quantization errors have effects on the accumulated histogram and the final INL and DNL estimation. The quantization effect is closely related to the average number of samples per code. With more samples, the quantization error will be small and the accumulated histogram can accurately characterize the transition points. Since the quantization error is distributed between 0 and 1/ N_S, we have

$$\sigma_Q^2\{\Sigma C_k^{(1)}\} = \frac{B_2}{N_S^2} \tag{39}$$

The subscript Q signifies that this part is due to the time domain quantization effect. B_2 is a coefficient dependent on the distribution of the quantization error. From the expression above we can see that increasing the number of samples can significantly reduce the quantization error in accumulated histogram and give better estimation for INL and DNL. The total estimation error will be due to the combined effect of the quantization errors and additive noise.

6. SIMULATION AND EXPERIMENTAL RESULTS

Simulations and experiments were done to verify the performance of the proposed algorithm. Simulation results show that the algorithm can estimate the integral and differential nonlinearities for a 12-bit ADC to 12-bit accuracy by using input signals of only 6-bit linearity and the performance of the algorithm is in agreement to theoretical analyses. In experiments, the integral and differential nonlinearities of 10-bit ADCs are estimated to more than 9-bit accuracy by using 2-bit linear signals.

6.1 Simulation results

Simulations were run under different combinations of parameters such as noise variance, the resolution of ADCs, the number of samples per code, etc. The nonlinear input signal used in the simulation is given by

$$f(t) = t + 0.04 \times (t^2 - t) + 0.02 \times (t^3 - 1.5t^2 + 0.5t) \qquad (40)$$

It has second order and higher order polynomial nonlinear terms with linearity less than 7 bits. Although in reality we can easily generate much better input signals, a highly nonlinear input was used in our simulations to confirm the robustness of the algorithm. Simulation results for a 12-bit ADC are plotted in Fig. 10.

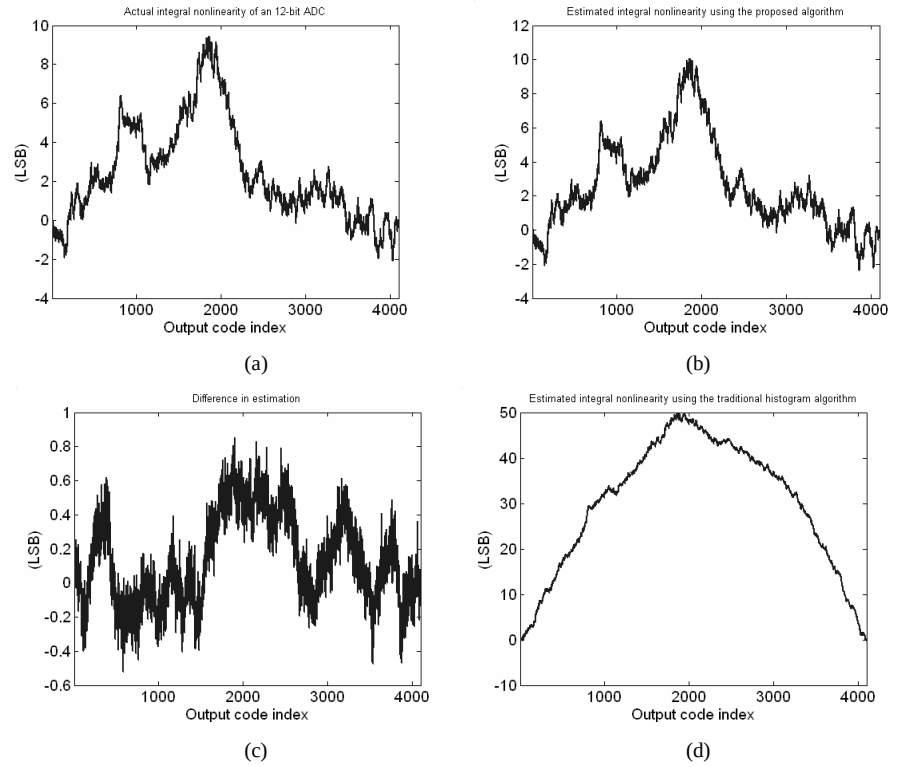


Fig. 10. Integral nonlinearity estimation for a 12-bit ADC

(a) Actual integral nonlinearity of a 12-b ADC

(b) Estimated integral nonlinearity using the proposed algorithm

(c) Difference between (a) and (b)

(d) Estimated integral nonlinearity using the traditional algorithm

The average number of samples per bin was chosen to be 32 (N_S=32) and additive noise at the ADC input has σ=0.8 LSB in simulation. Since the proposed algorithm is independent of the specific structure of the ADC, any type of ADCs can be used in the simulation. Because a flash ADC has the most number of independent error sources and therefore is believed to be more challenging to test, we choose to use a flash ADC in our simulation. The ADC has a string of 2^{12} resistors randomly generated following a uniform distribution in the range of 50% to 150% of their nominal value [11]. Once the resister values are generated, the ADC's transition points can be computed. The set of transition points are then used to represent the ADC in the simulation. As defined before,

the variation of these transition points from their corresponding end-point fit line transition points are the integral nonlinearity of the ADC. Fig. 10 (a) shows the integral nonlinearity Ψ_k of a simulated ADC at each code. It can be observed from the figure that the actual integral nonlinearity of the ADC is between +10 and -2 LSB. Fig. 10 (b) shows the nonlinearity of the device as predicted using the proposed algorithm with a 6-bit linear input signal. The difference between the actual nonlinearity values and estimated nonlinearity values is between +0.8 and -0.6 LSB, as shown in Fig. 10 (c). It can be observed that using the newly proposed algorithm, a 12-bit device can be characterized to within +/- 1LSB with an input signal which is just 7-bit accurate. To gain further insight the nonlinearity prediction using the traditional histogram algorithm with the same 7-bit linear input signal is plotted in Fig. 10 (d). We can see that the traditional algorithm identifies the device to have a 50 LSB INL. This magnitude of error is observed because the conventional histogram approach assumes that the input is a highly linear ramp, and any nonlinearity in input is wrongly interpreted as errors in the ADC. The proposed algorithm is not affected by this nonlinearity in the input.

The performance of the proposed algorithm under different noise and samples/bin were also simulated on a 10-bit ADC. The results are summarized in Table 1. The actual integral nonlinearity of the software modeled 10-bit ADC is between +3 and -2 LSB. The proposed algorithm was then used to identify the device and for each combination of noise and samples/bin, the algorithm was run 32 times to compute the variance.

Table 1. Variance of the error in INL estimation vs. σ and N_S

σ (LSB) \ N_S	16	32	64
0.2	0.2458	0.0773	0.0324
0.4	0.7265	0.2036	0.0804
0.8	1.5633	0.4806	0.1813
1.6	2.4974	0.9912	0.3505

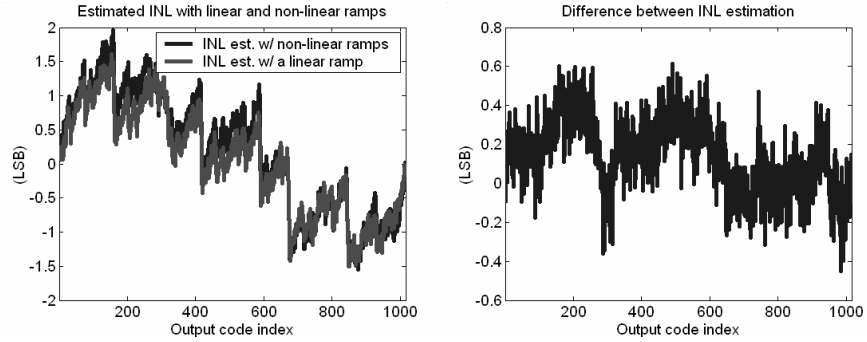
From the result we can see that the error in INL estimation is affected by both the noise effects and quantization effects as discussed in section IV. By choosing appropriate sample density, we can estimate the INL of an ADC to a reasonable accuracy, e.g., less than 0.5 LSB, even under large noise variance.

6.2 Experimental Results

In experiment, 10-bit commercial pipelined ADCs were tested to prove the effectiveness of the algorithm. Though test for 10-bit ADCs is a known art, an input of 13 bit or higher

linearity is always required. We are going to show the test result for a 10-bit ADC by using signals that are less than 3-bit linear. If the traditional method was used, it would be very unlikely to accurately identify the INL and DNL of a 10-bit ADC by using a 3-bit linear signal. There might be errors of hundreds of LSBs. By using the proposed algorithm we will see that the INL and DNL of 10-bit ADCs can be estimated to accuracy of better than 0.8 LSB in experiment. This result is as good as the result for a traditional histogram method by using a 13-bit signal.

A commercially available ADC was tested to estimate the effectiveness of the algorithm. Different ADCs and raw data were obtained. The entire testing was performed in a production test environment. As a first attempt, a commercial tester used in production test was used to generate the input signals and collect the output histograms. The tester was programmed to generate input signals with only 2-3 bit linearity (much more nonlinear than what was used in software simulations reported above). Although signals of much better linearity can be generated on-chip, to confirm the robustness of the algorithm and to consider the case of high resolution ADCs (14 bit and above) where 8-9 bit linear input signals are limiting factor, the input signals used in the test runs were intentionally limited to a low linearity. The second signal was obtained by subtracting a DC shift value of about 10 LSB from the first signal. This amount of shift and the exact nature of the input signal were unknown to the algorithm. These values were independently computed as part of the algorithm. Results of INL estimation using the proposed algorithm with the above described highly nonlinear input signals were then compared to the results calculated from using the traditional histogram algorithm with a highly linear ramp signal. The signals were sampled at 32 samples per code on average.



(a) (b)

Fig. 11. Integral nonlinearity estimation using the proposed methods

(a) Estimated INL with linear and non-linear ramps

(b) Difference between INL estimation results

To start with, the results using the highly linear signal and the traditional histogram method were considered to be the true nonlinearity of the ADC. The difference between the results using the proposed algorithm and the traditional method is then considered the residual error of the new algorithm. The results of the experimental test are given in Fig. 11. It can be seen that the algorithm is able to identify the nonlinearity of the device to within 0.7 LSB using an input signals that is just 2-3 bit linear. Fig.11 shows the result obtained using just 1 sample product. The experiments were then repeated on 20 different ADCs. The same input signal with nearly 2 bit linearity was used to test all the devices. The amount by which the second nonlinear signal was shifted with respect to the first was about 10 LSB for all devices. Fig. 12 shows the residue error in INL estimation using the proposed method, with the assumption that the linear ramp and traditional method gives the true characteristics of the ADCs.

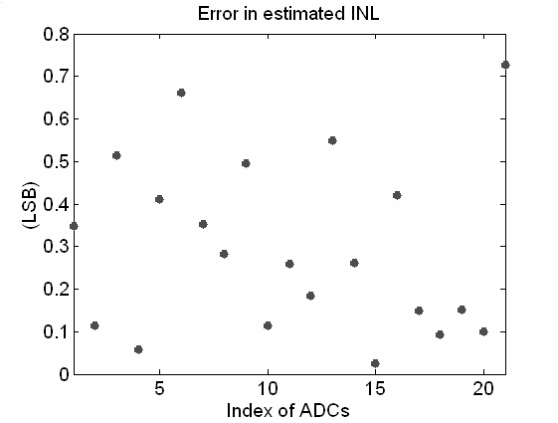


Fig. 12. Error in INL estimation – for 21 devices

It can be seen that the parts were identified to accuracy of 1 LSB using the new algorithm. Further, to see the effect of noise, one part was randomly picked again and the traditional histogram test with a highly linear ramp excitation was performed on that device for the second time. The INL measurements from the two linear ramp tests were compared. In the ideal noise free case, we would expect the INL measurements to be same, since they represent the same device. However, due to the presence measurement noise, the measurements from the two runs for the same part will be different from each other, even if a perfect linear ramp is used with the standard testing approach. In our tests, a maximum error of 0.7 LSB was found between the two runs. This indicates that the measurement noise in the testing environment is at such a level that places a bound on the INL estimation accuracy. Given this effect of noise in measurement, due to factors like temperature and time related drift, the INL estimation errors given in Figure 12 using the proposed algorithm is very reasonable.

7. CONCLUSIONS

In this paper, we first analyzed the testing flow in existing approaches to analog and mixed-signal production test and built-in self-test. It was pointed out that the use of high-precision excitation signals and high-precision measurement devices was posing daunting challenges critical to cost-effective AMS testing. We further proved mathematically (and supported by simulation) that the industry standard histogram method could not correctly test ADCs if the input excitations were not sufficiently precise, rigorously validating a common knowledge among most test engineers. These two observations together motivated us to introduce a radically new approach to AMS testing. Unlike existing approaches, the proposed approach uses multiple related imprecise excitation signals and/or multiple related imprecise measurements together with appropriate post digital signal processing to accurately characterize an AMS DUT.

As a proof of concept, we presented a histogram based algorithm that uses two nonlinear ramp signals, instead of one perfectly linear ramp, to accurately test the DC linearity of ADCs. The algorithm was described in complete mathematical details. Extensive simulation results and experimental testing results obtained in an industry production test environment demonstrated that the new algorithm is capable of accurately testing ADCs using input signals that are 6-8 bits less linear than the ADC under test. The computational complexity of the new algorithm is a little more than that of the traditional histogram method but both algorithms share the same qualitative complexity proportional to the number of transition points in the ADC under test. Even though twice the number of data points is used in the new algorithm, the overall testing time of the proposed approach could be dramatically shorter than what is needed when a high-precision signal generator is used. This is because the data acquisition time dominates the overall test time for high resolution parts and the data acquisition rate in the new approach, when no longer limited by the source settling time, can be at the ADC clock rate which could be up to thousands or tens of thousands faster than what is permitted by a slow source.

Because of the elimination of the reliance on high-precision stimulus signals and high-precision measurement devices, the new approach offers great potential for accurate but cost-effective testing of analog and mixed-signal circuits in both production test and BIST. In production test, replacing high-precision but slow signal generators with imprecise but fast excitation sources can significantly reduce the cost associated with the test of high performance AMS parts. More importantly, the new approach has the potential to offer adequate and cost-effective test solutions for certain parts whose performance requirements are comparable to or even exceed the performance of state-of-

the-art test equipment and for which there are no viable test solutions on the horizon. In the BIST environment, there are several scenarios in which the new test approach can play the key role of an enabler for cost-effective integration of BIST strategies on chip. For example, a simple signal generator can be implemented on chip to provide the excitation input for ADC testing while the converted digital data is sent off chip for digital signal processing. This scenario would be a cost-effective solution for AMS parts that do not have on chip DSP capability readily available. A catalog ADC would be an example of such a case. Merely moving the signal generator on chip can alleviate many technical problems and bring about significant benefit with minimal overhead. At the other end of the scenario, the testing of an SoC scale circuit could be mostly performed with minimal intervention of an external tester by using the already available memory and DSP capability on chip for the execution of the test algorithm. In many cases, an SoC circuit may already have multiple ADCs and DACs on chip. These un-calibrated data converters can serve as the imprecise signal generator or imprecise measurement device, further reducing the overhead associated with BIST testing circuitry. Practical issues such as sequencing of the test control, implementation of the constant shift, and so on still needs to be resolved and are topics of current research.

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