LINEARITY TESTING OF PRECISION ANALOG-TO-DIGITAL CONVERTERS USING STATIONARY NONLINEAR INPUTS

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Abstract

As the performance of Analog-to-Digital Converters continues to improve, it is becoming more challenging and costly to develop sufficiently fast and low-drift signal generators that are adequately more linear than the ADC for the purpose of linearity testing. This work relaxes the linearity requirements on the signal generators used for ADC testing by alternatively employing multiple non-linear inputs. Assuming minimal prior knowledge of the input non-linearity, a testing methodology is introduced that is based upon first identifying and computationally removing the source non-linearity and then accurately estimating the ADC linearity. Production test hardware is used for validating the performance of this testing methodology using a high performance 16-bit SAR ADC as a test vehicle. Integral linearity error readings are identified to well within the +/-2 LSB range of the device specification by using only 8-bit linear inputs. This approach provides an enabling technology for cost-effective full-code testing of high performance ADCs in production test and for a cost-effective implementation of built-in self-test (BIST).

1. Introduction

DC linearity of analog-to-digital converters (ADCs) has been historically measured using output histograms obtained from an 'ideal' ramp or sine-wave input [1-3]. As long as certain best test practices are observed, modern mixed signal automated test equipment (ATE) has made DC linearity testing a fairly straightforward production task for ADCs with 14-bit or lower resolution [4]. Certain high-precision delta-sigma ADCs are inherently linear and do not require post-production linearity testing. High-speed pipelined ADCs are usually used and correspondingly tested with high input frequencies, which reduces the importance of DC linearity testing of these devices [2], except during debug [5] or calibration [6].

DC linearity testing remains a key test challenge for the production of certain class of high performance ADCs. Such an ADC typically combines 16-bit or higher resolution, 1 MSPS or higher conversion rate, little or no output latency, and input bandwidth exceeding its Nyquist rate. Recent examples of such high performance ADCs include the 16-bit 1.25 MSPS and 18-bit 500 KSPS SAR ADCs and the 16-bit 5 MSPS multi-bit delta sigma ADC. These ADCs utilize techniques such as precision laser trimming or dynamic element matching to achieve good linearity at relatively high sampling speeds. Such expensive mixed signal building blocks are typically used in medical applications including ultrasound and computer aided tomography as well as precision industrial process control and ATEs.

To better appreciate the challenges involved with DC linearity testing of high precision ADCs, the source requirements must be well understood. A signal source generating the input to the ADC is traditionally required to be more linear than the ADC under test. Acceptable test solutions usually requires the test accuracy to remain within 10% of the device specification, so +/-0.2 LSB test accuracy is required to test an ADC with a +/-2 LSB maximum linearity error specification. One LSB of a 16-bit ADC with 5V supply corresponds to 76uV. Achieving better than 15.2uV (0.2 LSB) source linearity becomes extremely challenging. Moreover, certain critical applications demand all codes of the ADC to be tested in production, creating long test times that often run in the order of a minute on an expensive mixed signal ATE. This extensive test time is usually required to average out the effects of input noise. Requiring the source to remain stationary during this long test time creates another challenge for linearity testing. The source architectures best known for good linearity, i.e. the delta-sigma structure, are not known for good drift performance, and vice versa. In addition, linear sources tend to be very slow and the slow settling characteristic of the source usually dominates the test time. A fast source becomes critical for dramatically reducing test costs. Therefore, to enable test solutions for future high precision ADCs, methods must be developed to relax some of the performance requirements on the input source.

This work dramatically relaxes the requirement of source linearity for ADC testing. If the source is allowed to be non-linear with no stringent requirements,

as well as no need for prior knowledge, on non-linearity characteristics, the design requirement for the source will be dramatically reduced. Such sources can be designed to have better drift characteristics and to work faster, properties which are key for improving testing accuracy and reducing testing time. Furthermore, such a non-linear source can be implemented on chip with a small die area to facilitate use in a built-in self-test (BIST) environment. The non-linear effects of the source will be effectively removed by identifying the non-linearities based upon outputs observed by the ADC under test. The nonlinearity identification problem becomes a digital signal processing task which can be performed during production by the tester computer.

Recent research including non-linear excitations for ADC testing can be found in [7] and [8]. Two different algorithms using nonlinear ADC excitations are discussed in [7]. One of these algorithms is sensitive to device noise, making applications to precision ADCs difficult. The second algorithm requires a matrix inversion which is not time-effective for high resolution ADCs. Both algorithms are dependent upon an assumption of low spatial-frequency nonlinearities in the input. An application of one of these algorithms to a 10-bit ADC is discussed in [8]. 10-bits resolution appears to be a practical performance limit on the specific algorithms used in this recent previous work.

As in the previous work, the assumption is made that the nonlinearities at the input are of modestly low spatial frequency but in contrast to the previous work, the test strategy introduced here is highly insensitive to the magnitude of the nonlinear components. The test time required for implementation of the proposed testing strategy is short, making it viable for use in a production test environment. The method and algorithm presented in this paper has been verified on a high performance 16-bit ADC, a real challenge in mixed signal testing.

2. Mathematical Formulation of the Method

In this section, mathematical details of the method are given. First, the modeling of the ADC and the non-linear input signal are discussed. Second, the mathematical model of the Integral Non-Linearity (INL) test is discussed. Third, the details of the proposed algorithm that estimate and remove the input non-linearity are given.

Modeling of an ADC and the input signal

For an n-bit ADC with $N=2^n$ output codes, the static input-output characteristic can be modeled as

$$D(x)=\begin{cases}0, & x \le T_0 \\ k, & T_{k-1} < x \le T_k \\ N-1, & T_{N-2} < x \end{cases} \qquad k=1,2...,N-2 \tag{1}$$

where D is the output code, x is the input voltage, and T_k, k=0, 1 …, N-2, are transition points of the ADC. Each transition point T_k is a threshold voltage. If the input voltage is less than T_k, the output code will be less than or equal to k. If the input voltage is larger then T_k, the output code will be bigger than k. Further, in equation (1), it is assumed that the ADC is monotonic and has no missing codes. This is a good assumption for high performance ADCs.

Linearity test of an ADC corresponds to investigating how linearly transition points of an ADC, T_k, k=0, 1…, N-2, are distributed. An ideal linear ADC with the first and last transition points denoted by T_0 and T_{N-2} has transition points uniformly spaced between T_0 and T_{N-2} with a constant voltage increment of $(T_0-T_{N-2})/(N-2)$. This increment is called 1 LSB. Transition points of the ideal linear ADC are usually called endpoint-fit line transition points and notated as I_k. They can be expressed as

$$I_k = T_0 + \frac{T_{N-2}-T_0}{N-2}k, \quad k=0,1...N-2 \tag{2}$$

Equation (2) is called an endpoint-fit line, since it is a straight line connecting the first and last transition points of the ADC. For linearity testing, actual transition points of an ADC will be compared to corresponding fit line transition points. The difference between the actual transition points and the fit line transition points is defined as transition point INL. Expressing INL in LSBs, we get

$$INL_k = \frac{T_k - I_k}{1LSB} = \frac{T_k - T_0}{T_{N-2}-T_0}(N-2)-k, k=1...N-3 \tag{3}$$

A larger INL indicates an ADC has higher non-linearity.

An ideal ramp signal as assumed in traditional linearity testing can be visualized as a signal that increases linearly with time t, whereas a more realistic ramp signal always has some non-linearity that makes it deviate from a straight line. A real ramp signal can be modeled as:

$$x(t) = x_{os} + \eta t + F(t) \quad (4)$$

where x_{os} is a DC offset, η is the slope of the linear component and *F(t)* is the nonlinear component. Let us define transition time t_k to be the time at which the value of the ramp signal is equal to the kth transition point of the ADC.

$$T_k = x(t_k), k = 0,1..., N-2 \quad (5)$$

Monotonicity of the source is assumed in this work, and hence the output codes before t_k will be always less than or equal to k. To simplify derivation, we perform some linear operations on equation (4), which will not affect the final test results. First, we choose the first transition time to be the origin of time, i.e. t_0=0. Second, we make the last transition time to be unit time, i.e., t_{N-2}=1. Furthermore, we define the non-linearity in input signal to be 0 at *t*=0 and 1. In other words,

$$F(0) = F(1) = 0 \quad (6)$$

These operations are equivalent to choosing

$$x_{os} = T_0, \eta = T_{N-2} - T_0 \quad (7)$$

Substituting equation (7) into (4), we get

$$x(t) = T_o + (T_{N-2} - T_0)t + F(t), 0 \le t \le 1 \quad (8)$$

Equation (8) represents a signal whose magnitude is equivalent to the first and last transition points of the ADC at normalized time 0 and 1, respectively. The non-linearity of the input signal is totally characterized by *F(t)*. The above equation basically relates the time variable to the input waveform, with the ADC's transition points being the parameters.

Because we do not have prior knowledge about the general form of *F(t)*, we will use a set of complete and orthonormal basis functions $\{F_j(t), j = 1,2,3...\}$ to express the input non-linearity. As an example, we first choose familiar and widely-used trigonometric functions on [-1, 1] to be the basis functions, though there are other alternative basis functions. We will show that using only a part of the basis functions we can obtain a simple parameterization for *F(t)*. Let us apply odd extension to *F(t)* to cover the interval [-1, 1],

$$\hat{F}(t) = \begin{cases} F(t), & 0 \le t \le 1 \\ -F(-t), & -1 \le t < 0 \end{cases} \quad (9)$$

This function can be expanded as:

$$\hat{F}(t) = \sum_{j=1,2...} a_j \sin(j\pi t) + \sum_{j=0,1...} b_j \cos(j\pi t), \quad -1 \le t \le 1 \quad (10)$$

where a_j, j=1, 2…, and b_j, j=0, 1, 2…, are associated coefficients. Since the extended function is odd, coefficients of cosine functions are all 0 and only sine functions are necessary for expressing the non-linearity. On [0, 1], *F(t)* can then be parameterized by the sinusoidal functions as

$$F(t) = \sum_{j=1}^{M} a_j \sin(j\pi t) + e(t) \quad (11')$$

In general, the parameterization of *F(t)* can be done with any set of basis functions $\{F_j(t), j = 1,2,3...\}$ which have the same property as *F(t)* such that they are equal to 0 when evaluated at t = 0 and 1.

$$F(t) = \sum_{j=1}^{M} a_j F_j(t) + e(t), 0 \le t \le 1$$
$$F_j(0) = F_j(1) = 0, \qquad j = 1,2...,M \quad (11)$$

An example of an alternative set of basis functions are polynomial functions
$\{F_1(t) = t(t-1), F_2(t) = t(t-1)(t-1/2)...\}$.

Since we can only handle finite number of parameters, first M basis functions are used in (11), and *e(t)* represents the combined effect of the residual terms that cannot be expressed by the M basis functions. However, by the completeness of basis functions, M can be appropriately chosen such that this residue is arbitrarily small. We will not carry the term *e(t)* in the following derivation and analyze its effect later. *F(t)* is said to be identified if we can determine the value of a_j, j=1, 2…, M. Figure 1 depicts the relationships between actual and fit line transition points, the input and output of an ADC, and the ideal and real ramp signals. The horizontal axis corresponds to time with transition time labeled. The vertical axis corresponds to the input voltage with transition points labeled. The region corresponding to different output codes are marked as dotted areas.

Modeling of the INL test of an ADC

The goal of ADC linearity test is to identify transition points and INL of an ADC. Transition points of an ADC cannot be measured directly. However, we can calculate the value of transition points by using equation (5), if the shape of the input signal and transition time is known to us. Substituting equation (8) into (3) and parameterizing the nonlinearity as described earlier, we get

$$INL_k = (N-2)t_k + \sum_{j=1}^{M} a_j F_j(t_k) - k, \quad k = 1,2...,N-3 \quad (12)$$

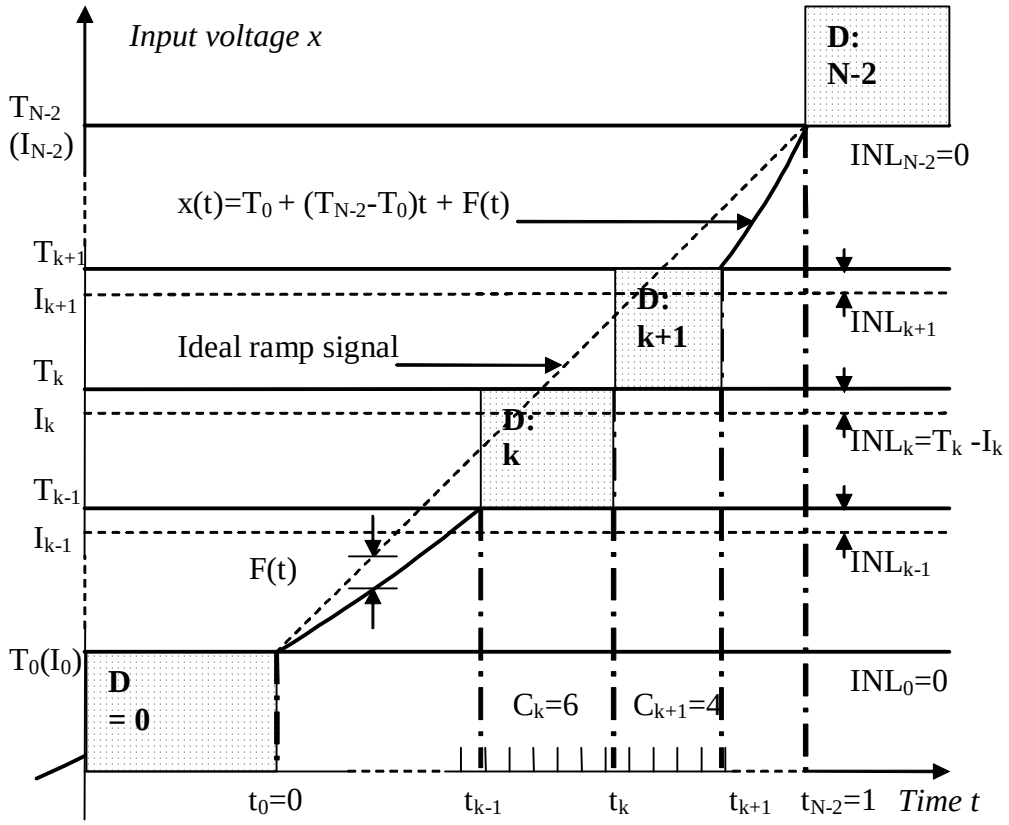

Figure 1. Basic relationships in ADC linearity testing

Coefficients a_j, j=1, 2…, M, are in LSB in the equation above.

Let us assume the output of an ADC is sampled at a constant rate. The number of samples obtained for each code can be represented as C_k, k=0, 1, 2…, N-2. If the conversion time of the ADC is constant, the time when a sample is taken is linearly proportional to the number of samples that has been taken before. So, the number of samples can be viewed as a measure of time. For example, C_0 samples are captured when the last sample of code 0 is taken; C_0+C_1 samples are captured when the last sample of code 1 is taken. In general, C_0+ C_1+…+C_k samples have been captured when the last sample of code k is taken, which can then be expressed as

$$\hat{t}_k = T_c \sum_{i=0}^{k} C_i \tag{13}$$

where T_c is the sampling clock period. If a particular sampled output code is k+1 while the previous code is k, the input voltage must change from less than T_k to larger than T_k during the previous clock period, and it is equal to T_k at a time between the two concerned samples, which is by definition t_k. That is

$$\hat{t}_k \le t_k < \hat{t}_k + T_c \tag{14}$$

There is an uncertainty of one clock period between the two samples. But when enough samples are taken, it's safe to assume the quantization error is insignificant and

$$t_k \cong \hat{t}_k = T_c \sum_{i=0}^{k} C_i \tag{15}$$

To be in agreement with equation (8), we shift and normalize the estimated transition time as in (16) so that the estimate of the first transition time 0 and the last transition time is 1.

$$\hat{t}_k = \sum_{i=1}^{k} C_i \Big/ \sum_{i=1}^{N-2} C_i \tag{16}$$

(16) is a key equation to be used while relating ADC transition time to histogram counts for each code. Substituting equation (16) in (12), we get an estimate for INL as:

$$\hat{INL}_k = (N-2)\hat{t}_k + \sum_{j=1}^{M} a_j F_j(\hat{t}_k) - k, \quad k = 1, 2..., N-3 \tag{17}$$

Equation (17) carries some significance. If the input non-linearity were known, equation (17) would relate the histogram counts to INL of the ADC. However, typically input non-linearity is not known before hand. Also (17) comprises of a set of N-3 linear equations with (N-3) INL values and M non-linearity values, amounting to a total of N+M-3 unknowns. The set of equations are thus insufficient to solve for all the N+M-3 unknowns. It can be observed that if assume the input signal is ideally linear such that all a_j=0, we get the traditional histogram method

$$\hat{INL}_k = (N-2)\hat{t}_k - k, k = 1,2...,N-3 \qquad (18)$$

This estimation is good when the input non-linearity is much smaller than 1 LSB. However, if the non-linearity is comparable to or larger than 1 LSB, it will give us significant error. The error in INL estimation can be obtained by subtracting equation (18) from (12)

$$INL_k - \hat{INL}_k = \sum_{j=1}^{M} a_j F_j(\hat{t}_k) + d(\hat{t}_k - t_k) \qquad (19)$$

The first term of INL estimation error is the input non-linearity. We see that the input non-linearity gets included in the estimated values of INL. This will result in misinterpretation of the actual linearity performance of an ADC. For example, if we use an input source with 10-bit linearity to test a 16 bit ADC with true 1 LSB INL, equation (18) will estimate the ADC to have an INL of about 64 LSB. In (19), $d(\hat{t}_k - t_k)$ is the quantization error in transition time. However, with a reasonable number of samples per code, it's usually a fractional of 1 LSB and much less than the term coming from the input non-linearity. We will neglect it presently and the effect of the quantization error will be dealt with later.

A new method for ADC linearity test

In equation (17), nonlinearities from different sources are coupled to each other and cannot be identified at the same time. In the proposed algorithm, two analog input signals will be used, and the input non-linearity and INL of an ADC will be separated and identified independently. The first signal is of the general form given in (4) and the second is simply a shifted replica of the first input signal with a shift voltage α. Such a shift could easily be obtained in hardware by an analog summing circuit.

$$x_1(t) = T_0 + (T_{N-2} - T_0)t + F(t) \qquad (20)$$

$$x_2(t) = T_0 + (T_{N-2} - T_0)t + F(t) - \alpha \qquad (21)$$

Transition time for the two signals is defined by following equations

$$T_k = x_1(t_k^{(1)}) \qquad (22)$$

$$T_k = x_2(t_k^{(2)}) \qquad (23)$$

Equations (22) and (23) are key to understand the logic behind the proposed method. Any non-linear (or linear) input maps the transition points of the ADC onto the time axis represented by histogram counts. The same ADC transition points can be mapped onto the time axis with different histogram counts using different input signals. If $C_k^{(1)}$ and $C_k^{(2)}, k = 0,1...,N-1$ are histogram data collected by using x_1 and x_2, estimates of transition time can be expressed in following equation by using the same argument for equation (16).

$$\hat{t}_i^{(1)} = \sum_{i=1}^{k} C_i^{(1)} \Big/ \sum_{i=1}^{N-2} C_i^{(1)} \qquad (24)$$

$$\hat{t}_i^{(2)} = \left(\sum_{i=0}^{k} C_i^{(2)} - C_0^{(1)} \right) \Big/ \sum_{i=1}^{N-2} C_i^{(1)} \qquad (25)$$

where transition time is shifted and scaled with respect to the first signal, with origin at $C_0^{(1)}$ and unit time at $C_{N-2}^{(1)}$. Similar to equation (17), we can have the estimate of INL formulated using each input signal and corresponding histogram counts.

$$\hat{INL}_k^{(1)} = (N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(1)}) - k, \quad k = 1,2...,N-3 \qquad (26)$$

$$\hat{INL}_k^{(2)} = (N-2)\hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(2)}) - \alpha - k, \quad k = 1,2...,N-3, \quad \hat{t}_k^{(2)} \le 1 \qquad (27)$$

Notice that the non-linearity is only parameterized on the interval [0, 1] by equation (11), but in (25) some transition time of the second input will be larger than 1. For that part of transition time, parameters are not well defined by (11), so those corresponding equations are excluded from (27). Roughly speaking the last α (in LSB) equations in (27) will have transition time larger than 1, so the total number of equations will be N-3-α. We will see for a reasonable shift value this reduction in number of equations will not affect the performance of the new method.

Equations (26) and (27) constitute the body of the proposed algorithm. The left hand side of the equations (ADC's trip points) will cancel when two equations are subtracted from each other and the input non-linearity will be left in a parameterized form. Moreover, there

will be more equations than parameters, so the system can be solved using a standard parameter estimation method. Regardless of the difference between two estimates of a same INL, we still have N+M-3 unknowns consisting of N-3 INL and M a_j parameters. But with two input signals and nearly doubled number of 2(N-3)-α equations, the identification of the unknowns is possible. Equating the right hand side of (26) and (27), we get

$$\begin{aligned}&(N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(1)}) = \\ &(N-2)\hat{t}_k^{(2)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(2)}) - \alpha\end{aligned} \tag{28}$$

It can be observed that the above equations contain only the parameters corresponding to the non-linearity in the input signal and have no INL parameters of the ADC. Moving the linear terms of transition time to one side of the equation and the nonlinear and shift terms to the other side, we get

$$\begin{aligned}&(N-2)\left(\hat{t}_k^{(2)} - \hat{t}_k^{(1)}\right) = \\ &\sum_{j=1}^{M} a_j \left(F_j(\hat{t}_k^{(1)}) - F_j(\hat{t}_k^{(2)})\right) + \alpha, \\ &k = 1, 2..., N-3, \qquad \hat{t}_k^{(2)} \le 1\end{aligned} \tag{29}$$

There are roughly N-3-α linear equations for M unknown parameters a_j. If the number of codes is much larger than the number of basis functions and the shift magnitude, the various unknowns are over constrained by (29) and can be estimated by using the Least Squares (LS) method. The LS method has an attractive property of partially or totally averaging out any noise or errors in equation (29). Denoting the estimated values of the parameters to be $\hat{a}_j, j = 1, 2..., M$ and substituting them into either equation (26) or (27) or their combination, we can estimate INL of the ADC. Using (26) for example, we get

$$\begin{aligned}&\hat{INL}_k = (N-2)\hat{t}_k^{(1)} + \sum_{j=1}^{M} \hat{a}_j F_j(\hat{t}_k^{(1)}) - k, \\ &k = 1, 2..., N-3\end{aligned} \tag{30}$$

3. A first attempt of error analysis

There are several sources of errors that will affect the performance of the algorithm. Among them the additive noise in the signal, the non-parameterized error of the signal as given in equation (11), and the quantization error of transition time as shown in equation (19) may have the most significant effects on the INL test results obtained by our method. Using the first signal as an example, and adding the effects of noise and errors, the relationship between transition points and the estimated transition time can be written as

$$\begin{aligned}T_k = T_o + (T_{N-2} - T_0)\hat{t}_k^{(1)} + \sum_{j=1}^{M} a_j F_j(\hat{t}_k^{(1)}) \\ + e(\hat{t}_k^{(1)}) + n(\hat{t}_k^{(1)}) + d(\hat{t}_k^{(1)} - t_k^{(1)})\end{aligned} \tag{31}$$

where $e(\hat{t}_k^{(1)})$ is the non-parameterized error, $n(\hat{t}_k^{(1)})$ is effect of the additive noise, and $d(\hat{t}_k^{(1)} - t_k^{(1)})$ is the quantization error. We further assume these noise and errors will not affect the LMS estimation of $\hat{a}_j, j = 1, 2..., M$ so that they can be assumed to be the same as $a_j, j = 1, 2..., M$. This is a fair assumption based on following reasons. First, the non-parameterized error is orthogonal to the first M sinusoidal functions by definition. Second, the additive noise and quantization error are usually changing very fast as a function of time and hence have little components correlated to low frequency basis functions. Third, the LS method will also average out the effect of fast changing components in noise and errors. Therefore the difference between the INL calculated in equation (30) and the actual INL is

$$INL_k - \hat{INL}_k = e(\hat{t}_k^{(1)}) + n(\hat{t}_k^{(1)}) + d(\hat{t}_k^{(1)} - t_k^{(1)}) \tag{32}$$

We will discuss these terms separately.

Effects of the non-modeled error in input signals

The magnitude of $e(\hat{t}_k^{(1)})$ is dependent on the number of basis functions used in parameterization, M, and the non-linearity of the input signal itself. As mentioned earlier, $e(\hat{t}_k^{(1)})$ can be reduced to arbitrarily small by increasing M. In reality, we require the input signal to be changing slowly. The non-linearity in the input can be large, but it doesn't change too fast so that we can parameterize it with reasonable number of basis functions to get a small residue error. Higher spatial-frequency nonlinearities can be handled by increasing the number of basis functions.

Effects of the additive noise in input signal

Let us assume the additive noise at the input to an ADC to be stationary and Gaussian with variance σ^2. The noise may make the output code different from its expected value, thereby changing the bin counts. Larger variance of the noise makes the code more likely to be different from its expected value. However, with a reasonably large number of samples per code, a change by one or two samples' value will not have a significant

effect on the total number of samples for a code. Intuitively, the variance of $n(\hat{t}_k^{(1)})$ may be positively correlated to the variance of the additive noise and negative correlated to the average number of samples per code. With more detailed statistical analysis, we can show that the following relationship is true.

$$\sigma\{n(\hat{t}_k^{(1)})\} = \sqrt{A\frac{\sigma}{N_s}} \quad (LSB) \tag{33}$$

where N_s is the average number of samples per code. A is a constant dependent on the distribution of the noise. For Gaussian noise, A=0.5642. This sensitivity to noise is also a fundamental problem in conventional histogram based ADC test algorithm.

Effects of the quantization error in transition time
The quantization error of transition time is bounded by equation (14). A smaller clock period T_c will produce more samples in total and a larger average number of samples per code N_s and the quantization error will become smaller. The standard deviation of the quantization error can be expressed in terms of N_s as

$$\sigma\{d(\hat{t}_k^{(1)} - t_k^{(1)})\} = \sqrt{\frac{1}{12N_s^2}} \quad (LSB) \tag{34}$$

In equation (34) we assume the quantization error is uniformly distributed.

Typically, in an all codes production testing environment, N_s is between 20 to 100 samples per code. The magnitude of the additive noise determines which term of (33) and (34) is more important to the test result. If the standard deviation of the additive noise is comparable to 1 LSB, the quantization error is much smaller than the effect of the noise. For high resolution ADCs, up to 1 LSB RMS noise is typical. This was the rationale behind neglecting the effect of quantization earlier. The same quantization error is also an issue in traditional histogram based testing.

Effects of the shift between two signals and others
The value of voltage shift α between two input signals also affects the final INL estimation results. If the shift is too small, the difference between the non-linearity of the two input signals at the same code level will be very small and noise in equation (31) will have significant effects on the LS method. The assumption that estimated parameters $\hat{a}_j, j = 1, 2..., M$ are close to the actual value doesn't hold any more and the numerical behavior of the LS method is no longer reliable under that situation. The shift can not be too large as well. As mentioned before, the last α equations in (29) will not be used to estimate the parameters, so the LS result is only optimal for part of the input non-linearity and not necessary to be optimal for the non-linearity on the whole interval of [0, 1]. Analysis shows that 0.1 to 1 % shift is appropriate for the proposed method. Both simulation and experimental results support this conclusion. The method estimates the amount of shift, so, no prior knowledge on the amount of shift is assumed.

We assume the two input signals are identical but with a constant shift. This is not true in reality. We always have time varying effects in the test, e.g. the drift of reference voltage. The signal source may change from the first to second run, which will introduce gain error and/or different non-linearity between two signals. These non-stationary effects can be eliminated by well designed time interleaving measurement. Two signals are interleaved in time to excite the ADC and collect histogram data. By using "common-centroid" sequence to interchange between the two signals, most of the non-stationary effects are cancelled in experiment.

4. Simulation results

Simulation were done in Matlab, using different combinations of ADC resolution, the average number of samples per code, the non-linearity of the input, the additive noise, and the voltage shift between two input signals. Simulation results show that the algorithm can accurately identify INL of an ADC of different resolution by using nonlinear excitations under various situations. Results from simulations of 14-bit simulated ADCs under different noise level and average number of samples are summarized as follows. The actual INL of the simulated ADC is shown in Figure 2.

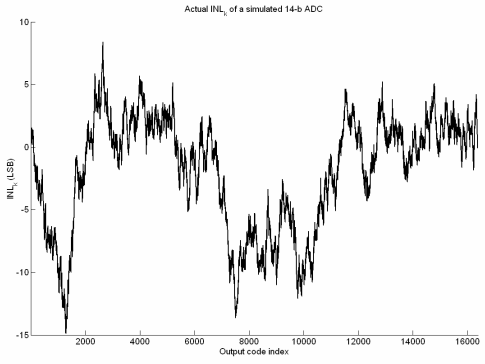

Figure 2. INL of a simulated 14-bit ADC

The first nonlinear input signal is modeled as

$$x_1(t) = t + 0.04 * (t^2 - t) + noise \tag{35}$$

The maximum non-linearity specified in (35) is 1% of the total input range. The input signal is 6-7 bit linear. The shift between the first and second signals is 128

LSB. However this data is not used in the algorithm and is considered as an unknown and calculated independently. 11 sinusoidal basis functions are used in parameterization of the nonlinear term in the input. If the additive noise has a standard deviation of 1 LSB and 32 samples are taken for each code on average, INL estimated by the proposed algorithm is shown in Figure 3. The difference between the actual and estimated INL is plotted in Figure 4, which shows that the error in INL estimation is less than .6 LSB. Using the proposed method the test results are nearly 14 bit accurate with just a 7 bit linear input signal.

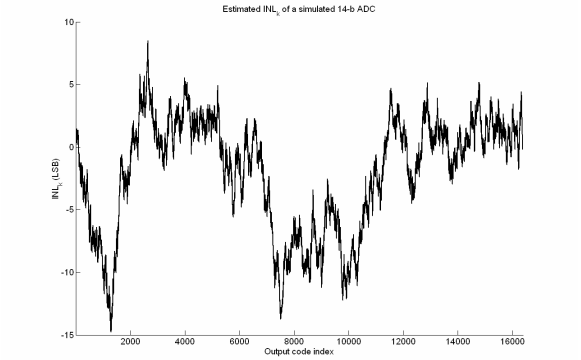

Figure 3. Estimated INL of the simulated ADC by using nonlinear inputs

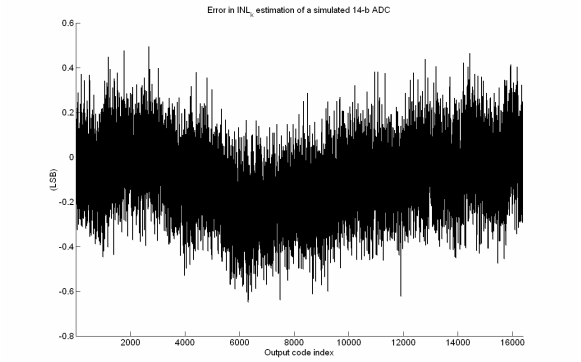

Figure 4. Difference between actual and estimated INL for the simulated ADC

Other results for different combinations of the average number of samples per code and noise are summarized in Table 1.

Table 1. Max INL estimation error of different N_s and σ

Shift = 128 LSB, 11 sinusoidal basis functions					
N_s	Σ (LSB)	Error (LSB)	N_s	σ (LSB)	Error (LSB)
16	0.8	0.78	16	0.2	0.46
32	0.8	0.54	16	0.4	0.60
64	0.8	0.40	16	0.8	0.78
128	0.8	0.32	16	1.6	1.22

For each of the INL error data in Table 1, 4 tests are simulated for each set of the same N_s and σ, and an average value of the maximum errors are calculated and listed. This allows us to statistically analyze the performance of the proposed algorithm. From Table 1, we can see that if N_s is increased by 4 times, the error in INL estimation is reduced by about 50%; if the standard deviation of the additive noise is increased by 4 times, the error in INL estimation is increased by 2 times. This is in agreement with equation (33).

5. Test Results from a 16-bit SAR ADC

Commercially available 16-bit ADC was also tested to verify the performance of the new method. The sample that was used as device-under-test (DUT) were laser trimmed 16-bit ADC with excellent linearity performance (typically +-1.5LSBs) making it a real test challenge. The test hardware used for the verification of our method is the same hardware used in the production testing of the device.

Test Setup

Verification of the full performance of this ADC requires extreme attention to test hardware design. A 12-layer handler interface board is used with extensive ground, supply and reference coverage. Extreme care is given to reduce ground loops and also to obtain proper bypassing. High performance contactors, high precision resistors, high performance capacitors and precision op-amps are used throughout the board. Latching relays are used to reduce temperature gradients generating metal to metal contact noise effects. The digital outputs are damped and buffered properly to avoid current surges. The test platform is Teradyne A580 Advanced Mixed Signal tester. The source generating both the linear and the synthetic nonlinear excitations is a 20-bit multi-bit delta-sigma DAC with 2ppm typical linearity error, 100uV/minute typical drift characteristics, and 2 KHz bandwidth (This source is a typical example demonstrating that an expensive signal generator is not always good enough to provide low drift, high speed and good linearity all at the same time). DC shift of the nonlinear excitation is given through an analog summing circuit. In the experiment, the testing of histogram data using nonlinear signals and identification of INL using the proposed method are done in different platforms. The tester setup, including the shape of the non-linearity in the input and shift between two signals are not known to the identification algorithm at all. Only two sets of histogram bin counts are fed into the analysis program.

Test Data Collection and Analysis

The INL of the ADC was first obtained by using the histogram from an ideal ramp excitation. This method

is the traditional method used during the production testing of the ADC. The INL plot is given in Figure 5. 32 samples per code are used to keep the test time reasonable.

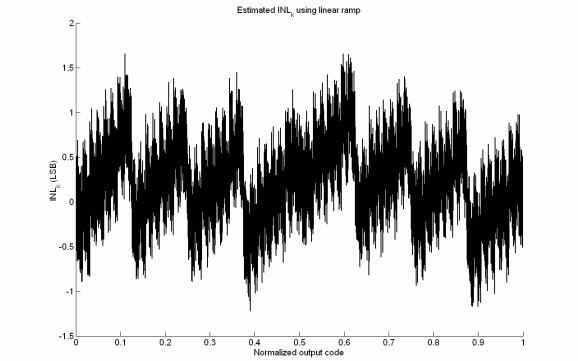

Figure 5. INL of a 16-bit ADC measured with a linear ramp

Figure 5 will be used as the actual INL of the ADC to compare the results of the proposed algorithm. We would like to mention here that actual INL of an ADC is actually not known to us. The INL measured with a linear signal is only an estimate of the actual INL. It is only *assumed* that INL measured with the conventional method is a good estimate of the true INL of the device.

The two nonlinear signals are synthetically generated by programming the source memory with a nonlinear digital waveform. The DC shift is generated by an analog summing circuit. The INL of the ADC measured with one of the two nonlinear signals and (incorrectly) calculated by the traditional histogram method using equation (18) are plotted in Figure 6.

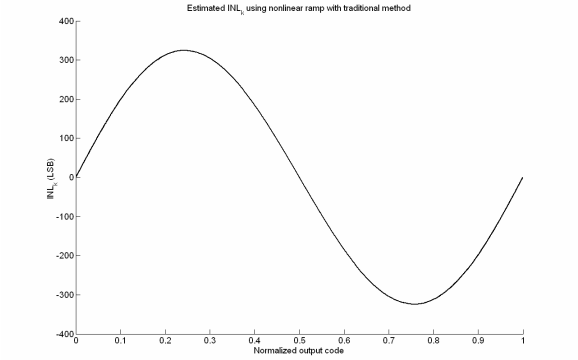

Figure 6. INL of the ADC measured with nonlinear input and calculated with the traditional histogram method. In the traditional method, any input non-linearity appears as ADC non-linearity.

The non-linearity is simply one period of a sine wave with some slight phase shift. These two nonlinear signals have only 8-bit linearity. They are fairly linear for the real world, but for our 16-bit, precision ADC, the amount of non-linearity at the input is simply excessive. Needless to say, these inputs are synthetically generated to be a representative of real world quasi-linear analog ramp generators such as simple integrators. When the method proposed in this paper is applied to the measured bin count data, we get an estimate of the INL as plotted in Figure 7.

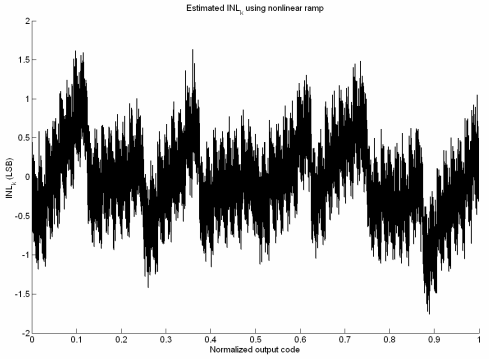

Figure 7. INL of the ADC measured with nonlinear input and calculated with the proposed method

INL measured in Figure 7 follows Figure 5 really closely. The difference between them is shown in Figure 8. This difference is promising and can be acceptable as far as 16 bit converters are concerned. Up to 0.5 LSB variation is inherent in histogram testing with 32 samples per code. In a previous study on this device, the performance of all-codes histogram testing was compared to the performance of reduced code testing with a servo-loop. At each code, differences up to 0.7LSB was found during the comparison, giving further proof that at 16-bit level, discrepancies indicating poor test capability do occur.

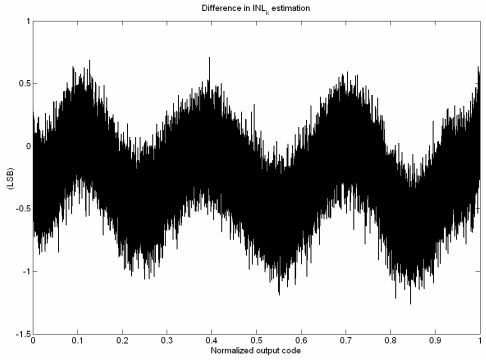

Figure 8. Difference between the INL estimation by using linear and nonlinear signals

The results in figure 7 and 8 are calculated by using the first 14 polynomial basis functions. Sinusoidal basis functions are also used and they estimate the INL with the same performance. This means that the proposed method doesn't rely on the selection of basis functions. Figure 8 shows that INL measured with linear and

nonlinear signals are in agreement with each other with an absolute difference less than 1.2 LSB, across all 65536 codes. This difference may be due to noise effect or due to the drift error in input signals. But by comparing figure 5 and 7, we can see that the proposed method accurately identifies the INL of an ADC using a low accuracy 8 bit linear input signal.

The test time penalty of this algorithm is insignificant. The actual test time for this 16-bit ADC is about 50 seconds, and the post-processing of the algorithm takes 1.2 seconds in Matlab to calculate the INL from the collected bin counts. Once coded in the tester workstation, the algorithm is expected to complete well within 100 milliseconds. If a fast nonlinear source were used, the test time would actually improve.

6. Conclusion

This paper solves the mathematics behind linearity testing of ADCs using non-linear signals. A nonlinear stationary excitation and its shifted replica are needed for a complete mathematical solution. No assumptions on the shape or the frequency of the non-linearity are made. No prior knowledge about the shift or non-linearity is required. Using actual production test hardware, the method was shown to test a high performance 16-bit ADC to well within its +- 2 LSB specifications, using only 8-bit linear inputs. The algorithm has insignificant negative impact to test time. With the introduction of this method and similar future methods, the test hardware development paradigm could easily shift from linear source development, to low drift and high-speed source development. The nonlinear low-drift input waveform and its shifted replica can even be generated on chip as a built-in self-test feature. The algorithm directly applies to DAC testing as well, since it cancels the ADC non-linearity totally while estimating the source (DAC) non-linearity.

7. References

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