Analog Integrated Circuits and Signal Processing, 37, 123–132, 2003


# Area Allocation Strategies for Enhancing Yield of *R*-2*R* Ladders

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*Received August 12, 2002; Revised October 4, 2002; Accepted March 20, 2003*

**Abstract.** A new strategy for allocating area, at layout, for enhancing the soft yield of *R*-2*R* ladders is introduced. In contrast to the conventional and convenient approach of allocating equal area to each R/2R bit-slice, the new strategy allocates progressively larger areas to higher-order bits. With this strategy, the INL yield for a fixed total resistor area as determined by local random variations in the sheet resistance is optimized. Simulation results show that the new area allocation strategy provides significant improvements in INL yield compared to what is achievable with the conventional area allocation strategy.

**Key Words:** *R*-2*R* ladder, yield, soft yield, standard deviation, sigma, INL, resistors, layout, ratio, LSB, MSB

## 1. Introduction

It is well recognized that different layout approaches of a given circuit may result in significantly different soft yields. Because of the importance of layout, considerable effort has been focused on optimizing the layout of matching-critical circuits. However, most of this work has been concentrated on the matching of two nominally identical devices or on arrays of nominally identical devices. Invariably, reported results are based upon using a standard cell and are concerned about placement and segmentation strategies for reducing yield loss due to random gradient variations. Little attention has been paid to circuits which require ratio matching where the ratio is not equal to one and essentially no consideration has been given to the issue of area allocation between components when the precise value of some components in a circuit is more critical than the value of others. In this work, the issue of optimal area allocation between the resistors in *R*-2*R* ladders is addressed.

Gradients and local random variations in the sheet resistance are the two major factors that contribute to ratio-matching errors in resistors. The effects of first or higher-order gradient effects on ratio matching can be minimized by appropriate placement, segmentation and common-centroiding of the layout [1–3]. If the types of gradient effects present can be accurately modeled, these techniques can be used to drive the gradient effects to arbitrarily low levels. If gradient effects have been taken care of, local random sheet resistance variations become the dominant contributor to ratio errors. Several researchers have reported that the standard deviation of the resistance or capacitance in integrated devices due to local random variations [4, 5] is inversely proportional to the square root of the area used for the components. Thus, the conventional strategy for minimizing the effects of random local variations in the sheet resistance is to allocate sufficient area to the matching-critical components to achieve acceptable matching performance. Unfortunately, there is little in the literature to suggest how area relates to yield when the ideal component ratios are not unity. As a result, many engineers either allocate excessive area to achieve an acceptable yield or suffer a yield penalty if inadequate area is allocated. Unfortunately, too, is the observation that many engineers do not know whether they have allocated too much or too little area for a given yield target until after test results have been obtained and, if the yield is inadequate, they often do not know whether the yield loss is due to inadequate area allocation or other factors. Although it might appear that allocating excessive area is a viable design strategy, aside from the increased die costs and hard yield loss associated with the excessive area allocation, the increased parasitic capacitances associated with the extra area will invariable limit high-frequency performance of the circuit.

Beyond the issue of area allocation is the issue of area partitioning and this has received little, if any, attention in the literature. Invariably, if an n:1 component ratio is required, it is assumed that this will require an n:1 area ratio as well. Thus, the conventional area partitioning strategy can be termed a component-ratio strategy. Whether the component-ratio area partitioning strategy is optimal deserves consideration. As a consequence, *the problem of soft-yield management in ratio-critical circuits becomes one of determining how to optimally allocate and partition area between the matching-critical components*.

One partial solution to this problem is to develop better tools or analytical procedures for area allocation so that area can be judiciously allocated for achieving a desired yield. It was recently shown that for some applications requiring two or more ratio-matched components the yield can be significantly improved [6] by using an area partitioning strategy different from the standard component-ratio strategy. Thus, a second part of a solution to this problem is to develop better area partitioning strategies for ratio-critical circuits.

In the following, we will concentrate on the linearity of $R$-$2R$ ladders by studying specifically the INL of these structures. We will develop an analytical procedure for predicting the soft yield based upon the areas allocated to the individual resistors in the structure. We will also introduce a new area partitioning strategy that will improve yield for a given total area. In these discussions, it will be assumed that appropriate segmentation and placement is used to render gradient effects non-dominant.

A simple example shows the important role that the area partitioning plays in these structures. Consider the case of the $n$-bit $R$-$2R$ ladder DAC of Fig. 1 where the resistors without a subscript are nominally of value $R$ and those with the '2' subscript are nominally of value $2R$. It will be shown that by using the new area partitioning strategy for resistor layout, the standard deviation of the INL for a 16-bit DAC will be reduced by 48% when compared to that attained with the standard component-ratio area partitioning strategy. This same example can be viewed in a different way. If the standard area partitioning strategy was used along with the area needed to obtain a yield of 81.5%, it will be shown that the new area partitioning strategy will improve the yield to 99% for the same total area.

## 2. Area-Partitioning

If the gradient effects are neglected, it is well-known that the standard deviation of the normalized resistance of any rectangular resistors of length L and width W due to local random variations in the sheet resistance can be expressed as [6]:

$$\sigma_{\frac{R_{ran}}{R_N}} = \frac{A_\rho}{\rho_N\sqrt{WL}} = \frac{A_\rho}{\rho_N\sqrt{A_R}} = \frac{K_\rho}{\rho_N\sqrt{A_R}} \qquad (1)$$

where $A_\rho$ is a process parameter that characterizes the random local sheet resistance variation, $\rho_N$ is the nominal value of the sheet resistance, and $A_R$ is the area of the resistor. For convenience, the ratio of $A_\rho$ to $\rho_N$ is denoted as $K_\rho$.

The two standard area partitioning approaches depicted in Fig. 2 for implementing an $R$-$2R$ ladder can be both termed component-ratio partitioning strategies. In this figure, the switches $d_1, \ldots d_n$ are not shown. We term the strategy of Fig. 2(a) the "conventional series" strategy. In the conventional series strategy, the "$R$"

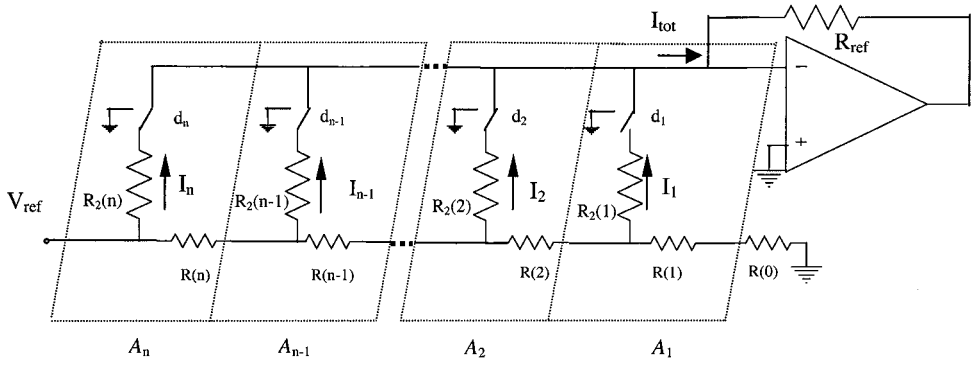


*Fig. 1.* A basic $n$-bit $R$-$2R$ DAC.

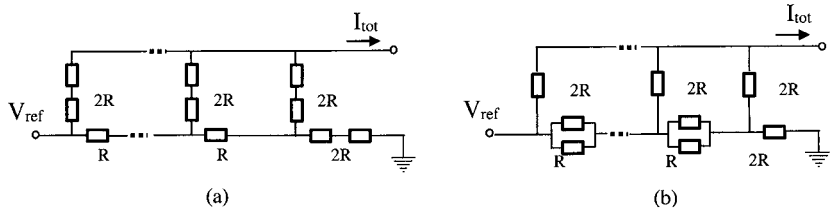


*Fig. 2.* Area distribution of standard $R$-2$R$ ladders (a) conventional series and (b) conventional parallel configurations.

resistors are all implemented with a unit resistor cell and the "2$R$" resistors are implemented with two of the unit resistor cells connected in series. The second, depicted in Fig. 2(b) is termed the "conventional parallel" strategy. In the latter, the "2$R$" resistors are all implemented with the standard resistor cell and the "$R$" resistors are implemented with two standard resistor cells placed in parallel.

For the $n$-bit $R$-2$R$ DAC depicted in Fig. 1, we will assume the amplifier and the feedback resistor are ideal. This DAC has $N = 2^n$ output levels and from the definition of the endpoint INL [7], it can be readily shown that the INL at the $k$th output is given by:

$$\mathrm{INL}_k = \left( \sum_{i=1}^{n} d_i I_i - \frac{k}{N-1} \sum_{i=1}^{n} I_i \right) \Big/ I_{\mathrm{NOM}} \qquad 0 \le k \le N-1 \quad (2)$$

where the sequence $\langle d_i \rangle$ is the digital input, $k$ is the decimal equivalent of $\langle d_i \rangle$, $I_i$ is the current flowing in the corresponding bit resistors and the $I_{\mathrm{NOM}}$ is the nominal current of one LSB. The INL is defined to be the maximum of the absolute values of the $\mathrm{INL}_k$ and is formally expressed as:

$$\mathrm{INL} = \max_{0 \le k \le N-1} \{|\mathrm{INL}_k|\} \quad (3)$$

The standard deviation of the INL is denoted by $\sigma_{\mathrm{INL}}$. The INL is a random variable and is the $N$th order statistic of the $N$ correlated random variables, $|\mathrm{INL}_k|$ $0, \le k \le N-1$. Analytical expressions for statistics of the INL such as $\sigma_{\mathrm{INL}}$ are not mathematically tractable. This information is, however, essential for soft yield prediction and computer simulations can be used for characterizing the INL.

A comparison of the standard deviation of the INL for the conventional $n$-bit series and the conventional $n$-bit parallel area partitioning strategies for the $R$-2$R$ ladder will now be made. For this comparison, it will be assumed that the total area for the $R$-2$R$ ladders is fixed for all $n$ and that the standard deviation of a resistor with this total area is 0.1% of the nominal value. A C-program was used for a statistical analysis of the resultant $R$-2$R$ ladders and the results are shown in Fig. 3. From this plot, it is apparent that for a fixed total resistor area, the conventional series layout will give a substantial improvement in yield when compared with the conventional parallel layout. It can be deduced that to enhance yield, it is better to allocate more area to the "2$R$" resistors than to the "$R$" resistors. From this example, it is apparent that area allocation plays an important role in yield. This example naturally raises two questions: What is the optimal area allocation between the "$R$" and "2$R$" resistors and how should the area be allocated between more significant and less significant bit slices for a given total area? In what follows we will attempt to answer these two questions and develop insight into what resistors play the most important role in the overall INL.

With reference to Fig. 1, it can be shown analytically that the standard deviation of the $\mathrm{INL}_k$, $\sigma_{\mathrm{INL}k}$, is a maximum at $k = 2^{n-1}$ and at $k = 2^{n-1} - 1$. This can be

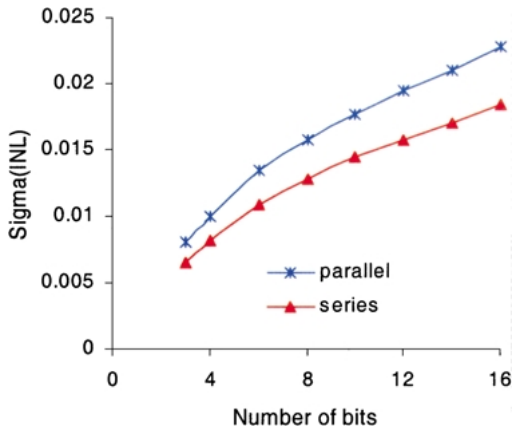


*Fig. 3.* Sigma INL vs. resolution level.

expressed as:

$$\max(\sigma_{\mathrm{INL}k}) = \sigma_{\mathrm{INL}(2^{n-1})} = \sigma_{\mathrm{INL}(2^{n-1}-1)} \tag{4}$$

It is instructive to identify the major contributors to $\max(\sigma_{\mathrm{INL}k})$. Although a formal expression of $\sigma_{\mathrm{INL}(2^{n-1})}$ for any $n$ is possible, the expression for the case where $n = 3$ does provide the desired insight. If we assume each resistor can be expressed as the sum of a nominal value and a random component, $R = R_{\mathrm{NOM}} + R_r$, it follows from a tedious but straightforward derivation for a 3-bit $R$-$2R$ ladder that

$$\begin{aligned}\max(\sigma_{\mathrm{INL}k}) = \sigma \Bigg\{ \frac{4}{7} \Bigg( & \frac{3}{16} \frac{R(0)_r}{R_{\mathrm{NOM}}} + \frac{3}{16} \frac{R(1)_r}{R_{\mathrm{NOM}}} \\ & - \frac{5}{16} \frac{R_2(1)_r}{R_{\mathrm{NOM}}} - \frac{1}{4} \frac{R(2)_r}{R_{\mathrm{NOM}}} - \frac{3}{4} \frac{R_2(2)_r}{R_{\mathrm{NOM}}} \\ & - \frac{R(3)_r}{R_{\mathrm{NOM}}} + \frac{3}{2} \frac{R_2(3)_r}{R_{\mathrm{NOM}}} \Bigg) \Bigg\}\end{aligned} \tag{5}$$

From this expression, it is apparent that the MSB resistors $R(3)$ and $R_2(3)$ provide the largest contributions to the standard deviation. These two resistors comprise the MSB bit slice of the $R$-$2R$ ladder. Further, within the bit slice, the resistor $R_2(3)$ is a bigger contributor to the overall standard deviation than the resistor $R(3)$. This indicates the "$2R$" resistor is a larger contributor to $\sigma_{\mathrm{INL}(2^{n-1})}$ than the "$R$" resistor in the bit-slice supporting the earlier observation that the "standard series" configuration which allocates more area to the "$2R$" resistors should have a lower $\sigma_{\mathrm{INL}(2^{n-1})}$ than the "standard parallel" configuration. This can be generalized to suggest that the MSB resistors make a larger contribution to the standard deviation of the $\max(\sigma_{\mathrm{INL}k})$ than the LSB resistors and the "$2R$" resistors make a larger contribution than the "$R$" resistors in arbitrary $R$-$2R$ ladder networks. Although $\max(\sigma_{\mathrm{INL}k})$ is not the standard deviation of the INL, this expression gives insight into the roles that different resistors play in determining the overall INL. Intuitively, the overall INL should be reduced if the standard deviation of those resistors that make the individual $\mathrm{INL}_k$s large can be reduced. This can be achieved if more area is allocated to the MSB resistors and less area is allocated to the LSB resistors while keeping the total area constant and even further improvements can be made if more area is allocated to the "$2R$" resistors than to the "$R$" resistors. Of course, if too much area were removed from the LSB resistors, the contributions of these resistors to the overall INL would again dominate thus deteriorating the INL. Although this qualitative discussion provides guidance into how the area should be allocated, a more rigorous investigation is needed to determining how the area should be optimally allocated between resistors in the $R$-$2R$ structure. An $n$-bit $R$-$2R$ structure is comprised of $2n + 1$ resistors and thus the key question is how to allocate area between these $2n + 1$ elements. This $2n + 1$ variable optimization problem itself is quite involved. It can be argued, however, that a near optimal solution can be obtained by considering how to distribute area between bit slices and how to allocate area within a bit slice. This facilitates a major reduction in the order of the optimization problem. In what follows, we will first consider a two-parameter optimization [7] and then extend it to a three-parameter optimization.

### *2.1. Two-Parameter Optimization*

We will consider an 8-bit $R$-$2R$ ladder but the results extend to $R$-$2R$ ladders of any order. Referring again to Fig. 1, observe each bit slice has an "$R$" resistor and a "$2R$" resistor allocated to the slice. The area allocated to these two resistors will be designated as the area associated with that slice (bit). The area allocated to the $p$th bit will be denoted as $A_p$. Therefore, the first slice area is $A_1$, the second is $A_2$, and the MSB slice area is $A_n$ for an $n$-bit ladder. For convenience, we will allocate the termination resistor, $R(0)$ in Fig. 1, to the LSB slice. In each slice, the allocation of area between the "$R$" resistor and the "$2R$" resistor must also be determined. Denote the ratio of the area allocated to the "$2R$" resistor and the "$R$" resistor in the $p$th bit as $k_{\mathrm{p}}$. An optimal area assignment strategy involves determining the optimal values of $A_1, \ldots A_n$ and $k_1, \ldots k_n$. With $2n$ variables and only one constraint, the total area, an analytical formulation of the optimal area allocation algorithm appears unwieldy.

To reduce the order, we will assume that the area ratio of the neighboring slices is $m$, i.e. $A_2 = mA_1$, $A_3 = mA_2, \ldots A_n = mA_{n-1}$ and the area ratio of the $2R$ and $R$ resistor inside each slice is $k$ as depicted in Fig. 4. We have thus reduced a $2n-1$ variable optimization problem to the 2-variable optimization problem of finding optimal values for $m$ and $k$. With this order reduction, for a given fixed $A_{\mathrm{total}}$, the standard deviation of the INL of the ladder is only a function of $k, m$. For relative comparisons, the value of $A_{\mathrm{total}}$ is arbitrary.

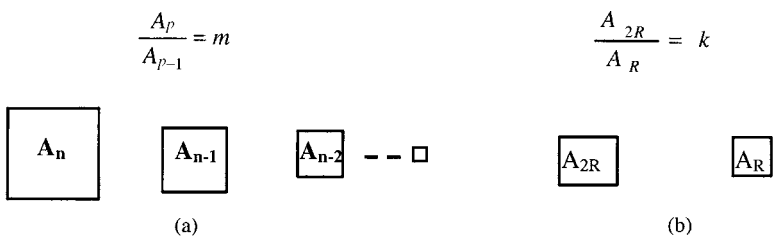


*Fig. 4.* Area allocation of $R$-2$R$ ladder cells (a) inter-slice allocation and (b) intra-slice allocation.

For an 8-bit $R$-2$R$ ladder, we first assumed $k = 2$ (this corresponds to the "conventional series" strategy discussed earlier) and then varied $m$ by computer simulations to find a minimum in the standard deviation of the INL. We found a shallow one-dimensional local minimum in the INL around $m = 1.7$ as depicted in Fig. 5. Then $m$ was fixed at 1.7 and $k$ was varied to obtain an optimal value of $k$ and the optimal value of $k$ around $k = 2.2$ as depicted in Fig. 6 was obtained. This one-dimensional local minimum was even shallower. We then repeated this procedure, fixing first $k$ and then $m$ but saw little further movement in either $k$ or $m$. It can thus be concluded that the two-dimensional local minimum is shallow and approximately given by

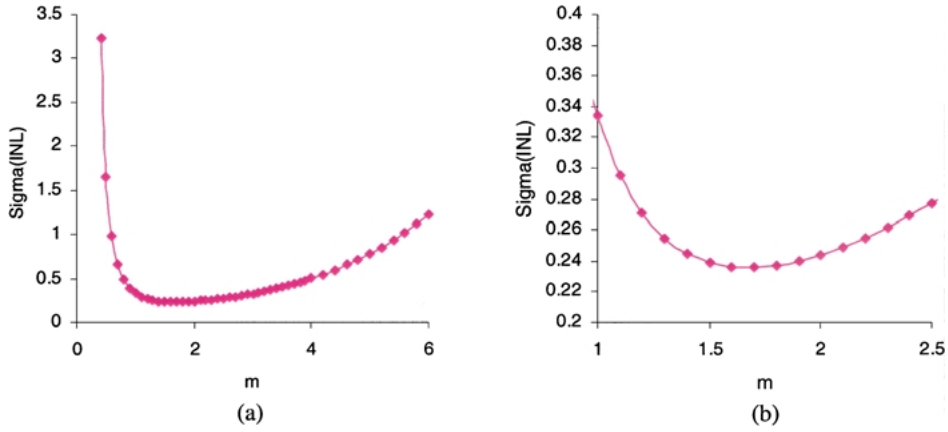


*Fig. 5.* Standard deviation of INL vs. $m$ for an 8-bit $R$-2$R$ ladder with $k = 2$ (a) coarse view (b) expanded view.

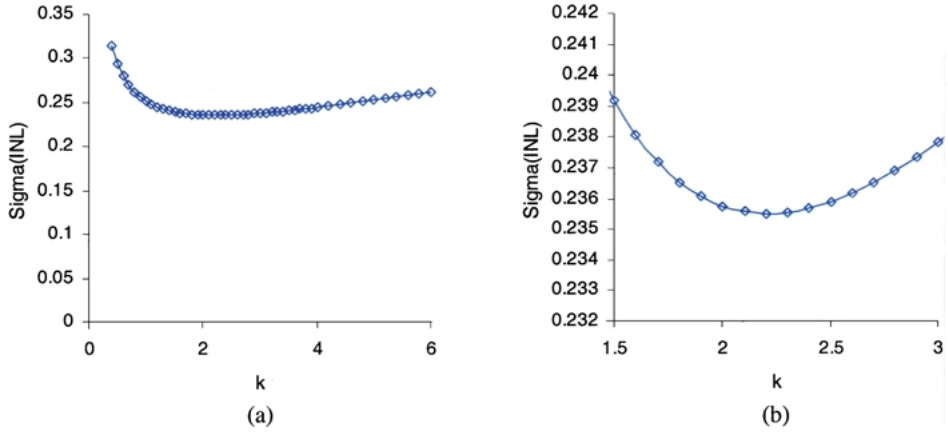


*Fig. 6.* Standard deviation of INL vs. $k$ for an 8-bit $R$-2$R$ ladder with $m = 1.7$ (a) coarse view (b) expanded view.

$m = 1.7$ and $k = 2.2$. From these simulations, it is apparent that the standard deviation is somewhat more sensitive to $m$ than to $k$ for $n = 8$. Simulations were undertaken for values of $n$ larger and smaller than $n = 8$. The local minima did not change much from the values of $m = 1.7$ and $k = 2.2$.

Although the local minimum is quite shallow, it should be observed that the value of $m = 1.7$ is far from the value of $m = 1$ that would correspond to one of the standard component-ratio area partitioning strategies thus indicating much more area should be allocated to the higher-order bit slices than to the lower-order bit slices.

### 2.2. *Three-Parameter Optimization*

In the two parameter optimization procedure, we allocated the area for the extra termination resistor to the LSB slice and did not allow the area partitioning within a bit slice to change with slice location. These restrictions can be altered by considering a three parameter optimization which is still quite manageable. The parameters $m_1$, $m_2$ and $k_1$ are defined respectively as the area ratio of the adjacent "$2R$" resistors, the area ratio of the adjacent "$R$" resistors and the area ratio of all of the "$2R$" resistors to that of all of the "$R$" resistors. For convenience, the LSB terminating resistor that is in series with the LSB "$R$" resistor is treated as the final "$2R$" resistor and is designated as $R_2(0)$. Formally,

$$m_1 = \frac{A_{R2(k)}}{A_{R2(k-1)}} \quad \text{for } n \le k \le 1$$

$$m_2 = \frac{A_{R(k)}}{A_{R(k-1)}} \quad \text{for } n \le k \le 3$$

$$k_1 = \frac{\sum_{i=0}^{n} A_{R2(i)}}{\sum_{i=2}^{n} A_{R(i)}}$$

This area partitioning is depicted in Fig. 7. Following a simulation strategy similar to that used in the two-parameter case, the optimal values of $m_1 = 1.7$, $m_2 = 1.7$ and $k_1 = 2.2$ were obtained. With the exception of the area associated with the termination resistor, these results are essentially the same as obtained in the two-parameter optimization and these results are essentially independent of $n$.

Although the two-parameter and the three-parameter optimizations do not necessarily provide the same local minimum as the completely general $2n - 1$ parameter optimization, they do suggest that a substantially higher percentage of the total area needs to be allocated to the higher-order bits than to the lower-order bits. As such, it is unlikely that the more general $2n - 1$ parameter optimization would result in substantive improvements over what was obtained with the much simpler two-parameter optimization.

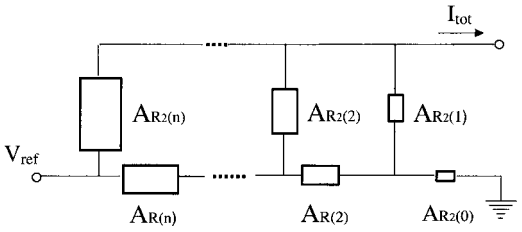


*Fig. 7.* The area distribution of three-parameter approach.

### 2.3. *Simplified Area Allocation Strategy*

Since the local minimums obtained above are quite shallow, near optimal INL performance can be obtained even if the area allocations differ modestly from the optimal. This will make the layout more practical. However, maintaining the area ratios for the lower order bits will become increasingly challenging since the areas for the lower-order slices are becoming quite small. Since the area for the lower-order slices is quite small and comprises only a few percent of the total area for large $n$, the question naturally arises: Can the LSB slices have the same area to reduce the layout efforts? Since this non-optimal area assignment will cause degradation in the standard deviation of the INL, the increase in INL will be considered.

Table 1 gives the increase in the standard deviation of the INL for selected resolution $R$-$2R$ ladders over what would be obtained if the same total area were used with optimal area partitioning. In this table, $s$ is the number of LSB stages with the same area. The first $n - s + 1$ stages were designed with the $m = 1.7$ and $k = 2.2$ area allocation strategy and the area in the last $s$ stages were all equal to the area in stage $s$. The

*Table 1.* The standard deviation of $R$-$2R$ ladder.

| $n$ | $s$ | $\sigma_{INCR}$ (%) |
|---|---|---|
| 8 | 3 | 0.5445 |
| 10 | 4 | 0.6819 |
| 12 | 5 | 0.6445 |
| 14 | 6 | 0.5302 |
| 16 | 8 | 0.9915 |

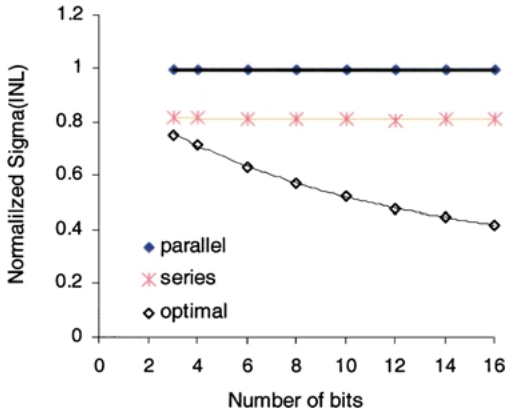


*Fig. 8.* The normalized sigma INL of $R$-2$R$ ladder vs. resolutions.

increase in the standard deviation of the INL, $\sigma_{\mathrm{INC}R}$, is less than 1% for the cases considered. For example, if the last 8 stages of a 16-bit $R$-2$R$ network all have the same area, the penalty in $\sigma_{\mathrm{INL}}$ over what would be obtained with optimal area allocation is less than 1%.

### *2.4. Comparison with Existing Strategies*

The new area allocation performance based upon $m = 1.7$ and $k = 2.2$ is compared with that of the conventional series and the conventional parallel approaches in Fig. 8 for different optimization values of $n$. In this plot, the standard deviation of the INL was normalized to that of the standard parallel layout to facilitate the comparison. From this plot, it is apparent that the standard deviation is reduced more with higher ladder resolution. For a 3-bit $R$-2$R$ ladder, the decrease in the standard deviation is 25% and for a 16-bit $R$-2$R$ ladder it is about 60% relative to what is attainable with the conventional parallel layout that allocated equal area to each bit.

The normalized sigma INLs for the three different approaches discussed above are compared in Fig. 9. The data of the simplified approach is based upon the area assignments given in Table 1. From these simulation results, it is apparent that the three different approaches give almost the same $\sigma_{\mathrm{INL}}$ and consequently the same yield.

## 3. Yield Enhancement with Optimal Area Allocation

The improvement in the standard deviation of the INL over what is achievable with a standard equal area/slice area allocation strategy was presented in the previous section. What is of bigger concern is how much improvement in yield can be obtained with the optimal

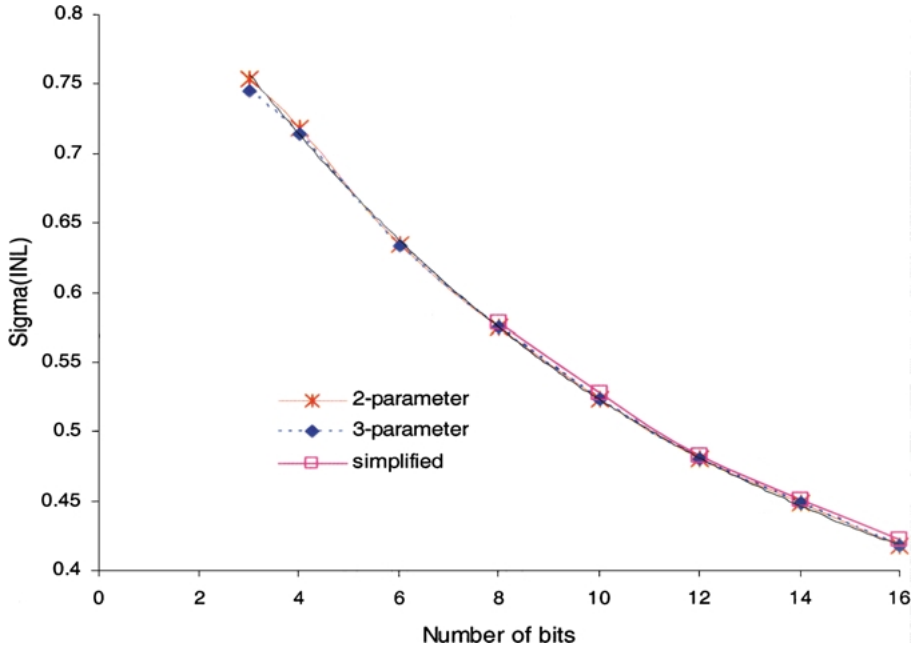


*Fig. 9.* The normalized sigma INL of $R$-2$R$ ladder vs. resolutions of three different optimal approaches.

area allocation strategy. The yield improvement will be discussed in this section.

The soft yield [6] of a device that has a single random error mechanism that is normally distributed can be expressed as:

$$Y = \text{erf}\left(\frac{\varepsilon}{\sigma\sqrt{2}}\right) \tag{6}$$

where, $\varepsilon$ is the tolerable error in a parameter of interest, $\sigma$ is the standard deviation of the same parameter, and $\text{erf}(x)$ is the standard error function. If $Y_1$ is the yield for a standard deviation $\sigma_1$, it is easy to show that the yield $Y_2$ if the standard deviation is changed to $\sigma_2$ relates to $Y_1$ by the relationship

$$Y_2 = \text{erf}\left(\frac{\sigma_1}{\sigma_2}\text{erf}^{-1}(Y_1)\right) \tag{7}$$

From (7), if $\sigma_1$ is the optimal standard deviation ($\sigma_{\min}$) and $Y_1$ is the corresponding optimal yield ($Y_{\text{opt}}$), it follows that the yield for a non-optimal sigma, $Y$, is given by

$$Y = \text{erf}\left(\frac{\sigma_{\min}}{\sigma}\text{erf}^{-1}(Y_{\text{opt}})\right) \tag{8}$$

It follows from (8) that a comparison of the optimal yield with a conventional series and a conventional parallel area assignment can be made from the data in Fig. 8. This comparison is made in Fig. 10. In this comparison, the total area for the optimal area assignment for each $n$ was selected to obtain a yield of 99% with the optimal area assignment. From this comparison, it is apparent that a substantial yield penalty will be paid if the optimal area allocation strategy is not used. For example, if the area is determined so that the optimal yield of a 16-bit $R$-2$R$ ladder is 99%, then the conventional series area allocation approach would result in a yield of only 81.5%. Stated alternately, if a conventional series area allocation had a soft yield due to random variations in the sheet resistance of 81.5%, then the new area allocation strategy would provide a yield of 99% with the same total area allocated to the $R$-2$R$ ladder.

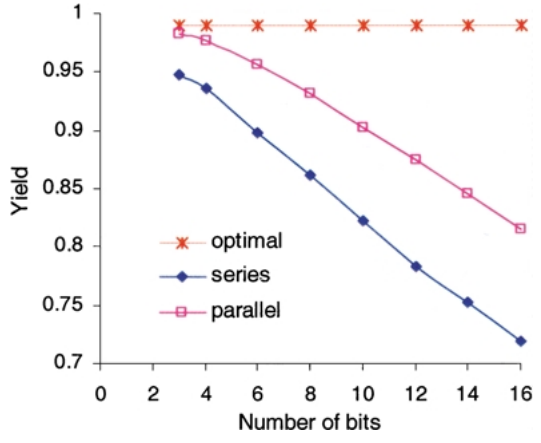


*Fig. 10.* The yield of different area configuration of $R$-2$R$ ladder vs. resolutions with same total resistor area.

The concepts presented here can be extended to the optimal allocation of area in capacitors and transistors in related applications.

## 4. Layout of Standard Cells

It is still important to use a standard cell and, if gradients are a problem, common centroid layouts of the $R$-2$R$ array. With the required scaling of area between slices, the issue of how the ratios of $m = 1.7$ and $k = 2.2$ can be achieved deserves attention. Since the local minimums are reasonably shallow, there is considerable flexibility in the layout. One possible standard cell layout that involves rationing in the first 6 stages and that then maintains a constant area per slice will now be described. Assume the "2$R$" resistor of the MSB block is comprised of 288 unit cells arranged 12 wide and 24 long. The MSB "$R$" resistor would then be 12 wide and 12 long. The next MSB block would have a "2$R$" resistor that is 9 wide and 18 long and the corresponding "$R$" resistor would be 9 wide and 9 long. The third MSB block would have the "2$R$" resistors 7 wide by 14 long and the corresponding "$R$" resistor would be 7 wide by 7 long. The fourth "2$R$" resistor would be 5 wide by 10 long and the corresponding "$R$" resistor would be 5 wide by 5 long. The next "2$R$" resistor would be 4 wide by 8 long and the corresponding "$R$" resistor would be 4 wide by 4 long. All remaining slices would have "2$R$" resistors that are 3 wide by 6 long and all "$R$" resistors that are 3 wide by 3 long. In this case, the sequence of $m$ values is 1.78, 1.65, 1.96, 1.56, 1.78, 1, 1, . . . , 0.75 and the sequence of $k$ values are all 2. Applying this approach to an 8-bit $R$-2$R$ ladder, the increase in the standard deviation of the INL, $\sigma_{\text{INC}R}$, is only 0.9% of the INL achievable with the optimal approach. Therefore, a modest deviation from the optimal $k$ and $m$ values will still give a near-optimal yield.

Other layout strategies that use the standard cell and which may provide closer agreement to the $m = 1.7$ and $k = 2.2$ area allocation strategy exist as well.

In the formulation presented in this paper, the issues of contact resistance and edge definition were not addressed. The random component of the contact resistance does play a significant role in yield prediction of $R$-$2R$ networks but it can be shown that the contact resistance does not alter the area allocation results developed in this paper. The randomness of the edges of the resistors will play a role as well when a large number of unit cells are used to realize the resistors in the $R$-$2R$ network. A formulation for the optimization of area allocation when both sheet resistance variations and edge variations are contributors to yield loss is straightforward but quite tedious and is not included in this work.

## 5. Conclusions

An assessment of the INL yield associated with random variations in the sheet resistance for the standard series and standard parallel equal bit/slice area layouts of an $R$-$2R$ ladder was made. This assessment shows that the yield of the standard series layout was somewhat better than the yield for the standard parallel layout. A new method for distributing area between the resistors of different bit slices has been introduced that provides near optimal yield for a given total resistor area. This area allocation strategy results in placing a higher percentage of the total area in the higher-order bit slices than in the lower-order bit slices. The optimal area allocation strategy provides a substantial improvement in soft yield when compared to what is achievable with the standard equal area allocation strategies.

## Acknowledgment

This work is supported in part by National Semiconductor, the Semiconductor Research Corporation (SRC) and the National Science Foundation (NSF).

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