PARAMETER OPTIMIZATION OF DETERMINISTIC DYNAMIC ELEMENT MATCHING DACS FOR ACCURATE AND COST-EFFECTIVE ADC TESTING

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ABSTRACT

Deterministic dynamic element matching (DDEM) is applied to low accuracy DACs for high resolution ADC test. The testing accuracy is impressive while the test cost is relatively low. This work tries to further optimize the DDEM parameters based on improving the testing accuracy and reducing the test hardware and computation cost. The optimization is accomplished by theoretical analysis and numerical simulation. Some typical parameter values are suggested by this work.

1. INTRODUCTION

Analog and mixed-signal (AMS) ICs often utilize analog-to-digital and digital-to-analog converters (ADCs and DACs). Test of high speed high resolution ADCs is viewed as one of the most challenging parts of AMS circuit test. [1] Conventionally, ADC linearity test requires a stimulus signal at least one decade more accurate than the ADC under test. Realizing such high accuracy stimuli is hardware consuming and very expensive. Furthermore, when considering build-in-self-test (BIST), it is very difficult to build such high accuracy signal generators with affordable chip area. [2]

To make the ADC linearity test more cost-effective and capable of BIST, researchers are working toward test approaches using relaxed stimuli. DDEM is one of the candidate approaches. In this method, DDEM is applied to a low accuracy current steering DAC and the output of the DAC serves as the stimulus to the ADC under test. The original DAC can be implemented with minimum-sized devices, and the DDEM control logic is very simple. Simulation results reported in ISCAS 2003 showed that this method is very promising. [3]

The DDEM method controls the current elements of the original DAC with a special switching sequence. For each DAC input code, the DAC generates many output samples with different combinations of the current elements. The DAC overall output is statistically linear. Key parameters affecting ADC test accuracy include the number of bit of the original DAC, the mismatch characteristics of current elements in the DAC, and the number of output samples for per DAC input code. Furthermore, the hardware cost and computational complexity are also greatly affected by these parameters. Optimizing the DDEM DAC parameters can help achieve the required ADC test accuracy with minimum cost.

This work focuses on optimal selection of DDEM DAC parameters for achieving accurate but cost-effective ADC linearity testing. Following this introduction, the general requirement of the stimulus for histogram based ADC test is presented in section 2. The DDEM method is briefly described in section 3. In section 4, we will discuss how the DDEM parameters affect the ADC test accuracy theoretically. Simulation results will be shown in section 5. Finally we summarize this work in section 6.

2. STIMULUS REQUIREMENT FOR ADC TESTING

An ADC can be characterized using a series of transition points which divide the whole input range into a series of decision intervals that are then mapped into digital codes. Suppose there is an n-bit ADC under test characterized by input range $[T_0, T_N]$ and transition points T_1~ T_{N-1}, where $N=2^n$. The N intervals: $[T_0, T_1]$, $[T_1, T_2]$, …, $[T_{N-1}, T_N]$ are mapped into N output codes C_0~C_{N-1}. An end-point fit line that connects the first transition point T_1 and the last transition point T_{N-1} is defined for the transfer curve as shown in Fig. 1. INL and DNL are defined to evaluate ADC static linearity performance. INL[k] is defined as the difference between C_k and the value on the fit line at the transition point T_k. DNL[k] is defined as the difference between the code width T_{k+1}-T_k for code C_k and the averaged code width. The overall INL and DNL are the maximum values of INL[k] and DNL[k] respectively.

$$DNL[k] = \frac{T_{k+1} - T_k}{(T_{N-1} - T_1)/(C_{N-1} - C_1)} - 1 \qquad (1)$$

$$INL[k] = C_k - \left(\frac{T_k - T_1}{T_{N-1} - T_1}(C_{N-1} - C_1) + C_1 \right) \qquad (2)$$

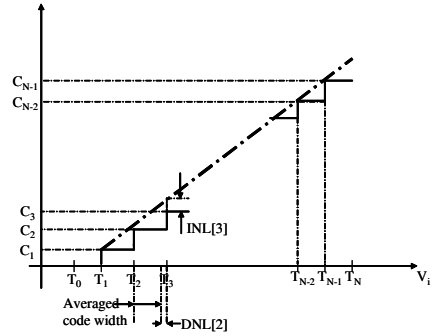

Figure 1: ADC fit line and DNL[k] and INL[k]

Histogram method is the most widely used method in ADC linearity test. The input to the device under test (DUT) can be any waveform. Once the input histogram $H_i(x)$ and output

histogram $H_o[k]$ are obtained, the ADC conversion errors can be identified. Here $H_i(x)$ can be defined as a combination of impulse functions positioned at the input analog voltages, and $H_o[k]$ counts the number of code C_k received at the DUT output end. Formula (3) relates the $H_i(x)$, $H_o[k]$ and the transition points. Here, '≈' is used due to the limit number of samples.

$$H_o[k] \approx \frac{\int_{T_k}^{T_{k+1}} H_i(x)dx}{\int_{T_1}^{T_{N-1}} H_i(x)dx} \cdot \sum_{i=1}^{N-2} H_o(i) \quad k = 1,...,N-2 \tag{3}$$

If the input samples are uniformly distributed over $[T_1, T_{N-1}]$, then we can calculate DNL[k] and INL[k] from (1), (2) and (3).

$$\hat{DNL}[k] = (C_{N-1} - C_1)\frac{H_o[k]}{\sum_{i=1}^{N-2} H_o(i)} - 1 \tag{4}$$

$$\hat{INL}[k] = C_k - C_1 - \frac{C_{N-1} - C_1}{\sum_{i=1}^{N-2} H_o[i]} \sum_{i=1}^{k-1} H_o[i] \tag{5}$$

To make (4) and (5) valid, the input histogram should be uniform. If the actual input histogram is not uniform, then estimation error is introduced. The estimation error mainly depends on how uniform the histogram is.

To generate the uniform input histogram, the conventional method uses a highly linear analog ramp generator or a high resolution DAC with high linearity. However, such high linearity is mathematically unnecessary for accurate ADC linearity test. [4] We can achieve such uniform histogram without caring about either the time-related linearity or the control code related linearity. There are various ways to generate statistically uniform histogram. Among them, the DDEM approach is one candidate that will be described in the following section.

3. DDEM DAC DESCRIPTION

DACs are often used to generate the stimulus for ADC linearity test. Conventionally, the DAC needs to have linearity at least 2-3 bits more than the ADC resolution under test. However, if we choose a low accuracy DAC and apply the DDEM to it, we can get the statistically uniform output histogram which is sufficient for ADC test.

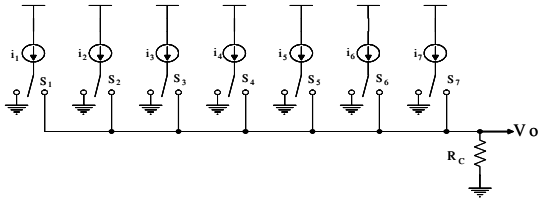

Figure 2: Basic structure of current steering DAC

We choose the thermometer coded current steering DAC and apply the DDEM method to it. To illustrate the basic idea, a 3-bit DAC structure is depicted in Fig. 2. Without DDEM control, the switches in Fig. 2 will be switched on one by one with sequential input codes. The DDEM method picks the current sources to be switched on in a way that all sources are used almost uniformly. To perform the DEM method, a n bit DAC has totally 2^n current sources. Let $N = 2^n$. We use $i_j \quad (j = 1,...,N)$ to denote the j^{th} current source element out of the total N elements. To understand the switch pattern, we can assume that all the current sources are arranged in a circular manner. For each input code k, the DAC has P samples of output. The first sample is obtained by switching k current sources started from i_1 in the clock-wise direction around the circle. The d^{th} $(1 \le d \le P)$ sample is obtained by switching k consecutive current sources started from $i_{(d-1)q+1}$ in the clock-wise direction, where q=N/P. The output analog signal is obtained by forcing the summation of the selected current sources to drive a resistor R_C. Since the resistor value can be viewed as a normalization factor, we can view the current through it as the DAC output to evaluate the DAC performance.

For each input code k, the DAC outputs P samples. Each output is the summation of the selected k current elements. The d^{th} current summation is denoted by $I_d(k)$. We have

$$I_d[k] = \sum_{j=1}^{k} i_{(d-1)q+j} \qquad d = 1,...,P \tag{6}$$

The average of P samples is denoted by $\bar{I}(k)$

$$\bar{I}[k] = \frac{1}{P}\sum_{d=1}^{P}\sum_{j=1}^{k} i_{(d-1)q+j} \tag{7}$$

The statistical performance of the DAC output will be evaluated based on $I_d[k]$ and $\bar{I}[k]$ in section 4.

4. DDEM DAC PARAMETERS AND OUTOUT DISTRIBUTION

Section 3 suggests that we only need to look at the current element combination for each code k. Suppose that the designed value of all current elements is i_0. Due to process and other variations, the actual value of each current source is given by:

$$i_j = i_0(1 + \varepsilon_j) \quad (j = 1,...,N) \tag{8}$$

We assume $\varepsilon_j \ \ i.i.d. \sim N(0, \sigma^2)$ where σ^2 is determined by design and process variations.

The overall output range is determined by $I[N] = N \cdot i_0 + i_0 \sum_{j=1}^{N} \varepsilon_j$.

The nominal output range is $N*i_0$. However, due to variations, the actual output range may not reach the nominal value. To make sure that DAC output range covers the DUT input range, we must make the DAC nominal output range to be larger than the ADC input range.

We will first inspect the average of the P output samples for each DAC input code k. To evaluate the linearity of the averaged output, we define an end-point fit line which connects (0, I(0)) and (N,I[N]). When k=t*q+s (s=1,…,q, t=0,…,P-1), it can be shown that the expected values of all the averaged output current $\bar{I}[k]$'s are on the fit line, and the standard deviation is given by

$$\sqrt{\frac{q(q-s)}{4Pq}}\sigma \cdot i_0 \tag{9}$$

If n=16, P=64 and σ=0.1, the maximum normalized standard deviation of the $\bar{I}[k]$'s is only 0.2, which shows that averaged output is almost uniformly distributed.

All the P output samples for code k center at $\bar{I}[k]$, and approximately obey the Gaussian distribution

$$N\left(\bar{I}[k], \frac{(N-k)k}{N}\sigma^2 \cdot i_0^2\right) \qquad (10)$$

With proper approximation, when P is large, all the output samples of the DDEM DAC obey a distribution with the following PDF.

$$f(x) = \sum_{k=1}^{N} f(x|k) \cdot P(k) \qquad (11)$$

Here, f(x|k) is the PDF corresponding to (10) and P(k) is the probability of each input code k. P(k)=1/N. For a DAC with given number of bit, P and σ are the two key parameters to determine equation (11). Though equation (11) is too complicated to simplify mathematically, we can draw the overall PDF as a combination of Gaussian PDF's with the aid of MATLAB. Fig 4 depicts the output PDF of a 10bit DDEM DAC. For this example, σ is chosen to be 0.1 and P is set to 64. From this figure, the output PDF is very flat except near the end points. Actually, near the end points, due to the small variances that can be calculated from (10), the PDF is discontinuous and fluctuates. The histogram of a DAC is a realization of such PDF, and should also be very uniform except near the end points.

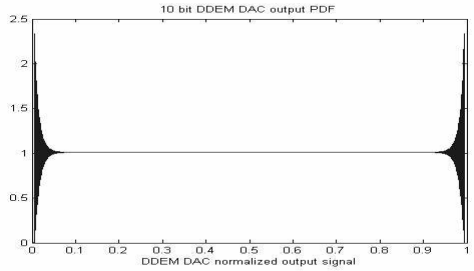

Figure 4: Output PDF of 10 bit DDEM DAC

The flatness of the PDF comes from two essential bases: 1) the averaged value $\bar{I}[k]$ which is the center of the individual distribution for each code D is almost uniformly distributed; 2) all the individual distributions for each code k have proper variances such that the combined distribution is continuous and flat. To inspect how P and σ affect the output PDF/histogram flatness, we can just look at how P and σ affect the two bases.

1) From equation (9), we can see that larger P leads to smaller variances for $\bar{I}[k]$'s and hence makes the distribution of $\bar{I}[k]$'s more uniform. Furthermore, increasing P means increasing the number of total output samples. Larger sample number will definitely make the shape of histogram closer to the flat shape of PDF statistically. In a word, large P helps to achieve uniform histogram.

2) Small σ brings small variances for $\bar{I}[k]$'s and also small variances for the individual distribution of each code k. Though small variances benefit the first base, extremely small variances hurt the second one. Actually if the variances for the individual distributions are too small, the whole combined distribution will fluctuate as near the end-points. On the other hand, large σ also hurts the flatness of the PDF since large σ makes the distribution of $\bar{I}[k]$'s worse. So σ needs to be set properly.

Though we can predict the DAC output PDF and therefore the output histogram use equation (11), such prediction is not adequate. To obtain the optimal DDEM DAC parameters, more simulation needs to be done.

5. SIMULATION OF DDEM DAC PARAMETER OPTIMIZATION

To validate the previous analysis and obtain the optimal DDEM DAC parameters for ADC test, simulation in MATLAB is carried out. In this simulation, a 14-bit ADC is under test. As an initialization, a 14bit thermometer coded current steering DAC is simulated to send stimulus to the ADC. The standard deviation of the current element mismatches is set to be σ=0.1. For each input code, the DAC sends P=64 analog samples to the ADC. To make sure that DAC output with uniform histogram that covers ADC input range, the DAC nominal output range is set to be larger than the ADC input range by 2%. The ADC INL[k] is estimated based on the ADC output histogram.

To evaluate the INL estimation accuracy, two error parameters E1 and E2 are defined. E1 is used to justify the error in INL[k] estimation, and E2 to determine the error in overall INL estimation.

$$E1 = \max_k \left| INL_{true}[k] - INL_{est}[k] \right| \qquad (12)$$

$$E2 = \left| \max_k \left| INL_{true}[k] \right| - \max_k \left| INL_{cal}[k] \right| \right| \qquad (13)$$

One simulation result including the true INL[k], estimated INL[k] and their difference is depicted in Fig 5. For this result, E1=0.2694 and E2=0.0714. The estimation errors are very low.

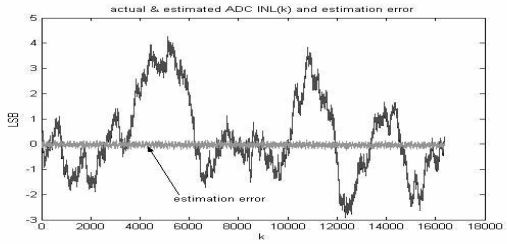

Figure 5: True INL[k], estimated INL[k] and estimation error

Now we will try to optimize the DDEM parameters with both test performance and test cost in mind. In the simulation, we vary the parameters and find those optimal parameter values that minimize E1 and E2.

1) DAC output range expansion

We must make the DAC nominal output expanded to exceed the ADC input range by a certain percentage. Denote this percentage as EXP. EXP cannot be too large; otherwise the effective resolution to the DUT is reduced. In simulation, EXP is varied and E1 and E2 are observed as shown in Fig 6. Though not displayed, E1 and E2 are 14 and 10 LSBs respectively when EXP=0. We can see that either when EXP is larger than 10% or less than 0.1%, E1 and E2 get large. It is safe to select EXP=2%.

2) DAC output sample number

Fix all the other parameters and change P. The simulation results are shown in Fig 7. It is obvious that increasing P can reduce the

estimation error. On the other hand, increasing P also means increasing the test time and computation complexity. Normally, P=64 is an acceptable value for both accuracy and cost. When P=64, the INL estimation error is only about 0.1LSB.

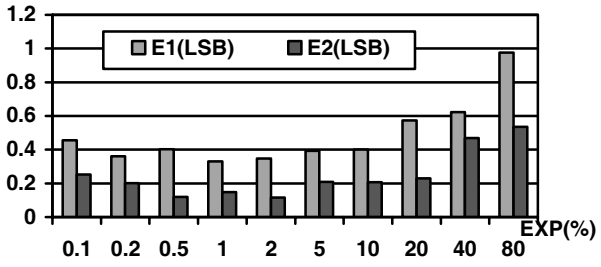

Figure 6: Estimation errors versus output range expansion

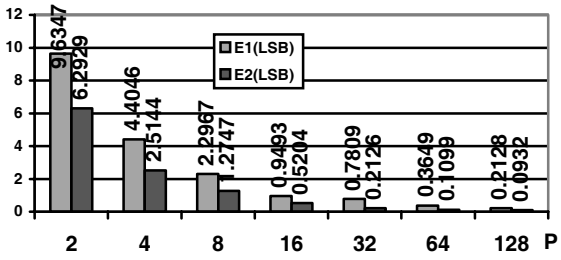

Figure 7: Estimation errors versus P

3) DAC current element mismatches

As discussed in section 4, the DAC current element mismatch affects the estimation accuracy greatly. Fig 8 shows the estimation errors as the current element stand deviation σ varies. The small estimation errors are achieved when σ is 0.03 to 0.1, implying 3σ current source mismatches in the 10% to 30% range. Such current sources are some of the easiest to achieve with minimum hardware overhead.

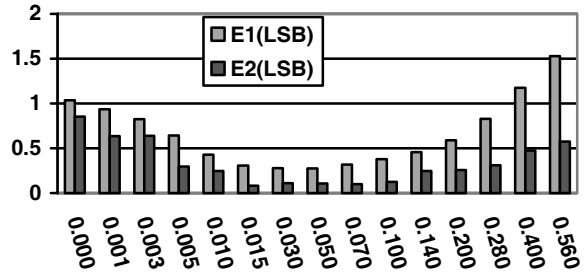

Figure 8: Estimation errors versus σ

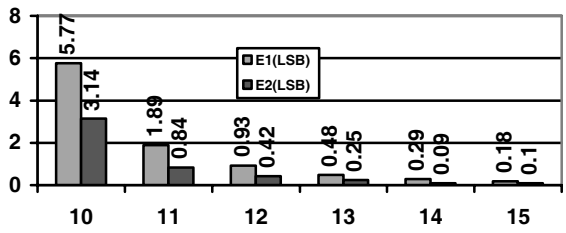

Figure 9: Estimation errors versus DAC NOB

4) DAC number of bit (NOB)

Increasing DAC number NOB while maintaining other conditions will increase the DAC accuracy and therefore increase the test accuracy. This is verified in simulation by changing DAC NOB while keeping other parameters (σ=0.05, P=64). The result is shown in Fig 9. We can also see that using a 13 bit DDEM DAC to test a 14 bit ADC, the INL estimation error is about 0.25LSB with hardware reduction by half.

5) Robustness of the DDEM approach

The previous discussion suggests that to test a 14-bit ADC with 14-bit DAC using DDEM, the following parameter values can be chosen: EXP=2% P=64 & σ=0.05. 6 ADCs with large INL variation are simulated and the DDEM approach with these selected parameters is applied. Results given in Fig 10 show that the INL estimation error is maintained at a low level no matter how the true INL of the DUT varies. The DDEM approach is robust.

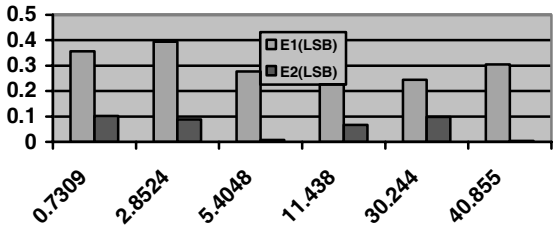

Figure 10: Estimation errors for ADC with large INL variation

6. SUMMARY

This work focuses on the parameter optimization of the DDEM approach for histogram based ADC linearity test. Theoretical analysis shows that two key DDEM parameters are essential to guarantee the output histogram flatness. These two parameters are the number of ADC output samples P for every input code and the normalized current element standard deviation σ. Analysis also predicts how these parameters affect the test accuracy. Simulation was carried out for testing 14 bit ADCs. The simulation results verify the theoretical analysis and suggest the optimal values for P, σ and the DAC output range expansion percentage based on the consideration of both test cost and test accuracy. The simulation result also shows that a 13 bit DAC with DDEM can be used to test a 14 bit ADC with acceptable accuracy with half hardware reduction. The DDEM approach is robust for ADCs with various linearity errors.

7. REFERENCES

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