AN SOC COMPATIBLE LINEARITY TEST APPROACH FOR PRECISION ADCS USING EASY-TO-GENERATE SINUSOIDAL STIMULI

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ABSTRACT

Analog and mixed-signal test is identified as one of the most daunting challenges for system-on-a-chip design. The bottleneck of mixed-signal test is the instrumentation of high precision signal generators and response measurement devices. This paper provides a cost-effective solution to the mixed-signal test problem by using low-accuracy but easy-to-generate stimuli instead of accurate signals generated by very expensive testers. We take the ADC linearity test as a vehicle to study the performance of the proposed approach. A low-linearity sine wave and an attenuated copy of the sine wave are used in the histogram test for an ADC. A stimulus error identification and removal algorithm is derived such that the ADC's linearity can be accurately determined without being affected by the sine wave's non-linearity. Simulation results show that 16-bit test accuracy can be achieved by using sine waves with a 38-dB SFDR, corresponding to a 6-bit linearity. This approach is applicable to test fully differential ADCs and extendable to other mixed-signal functions of IC products.

1. INTRODUCTION

System-on-a-chip (SOC) is a design style that integrates various functions into a high-complexity high-value product [1]. It is a promising trend for future IC design, since there are ever-growing demands for more powerful ICs from markets of automobiles, audio and video players, wireless communications, etc. Furthermore, current state-of-the-art technologies with a continuously shrinking feature size allow high level integration on a small piece of silicon.

An SOC system may include analog and mixed-signal (AMS), digital, and radio frequency (RF) functions on a single chip. Some functional blocks are deeply embedded in the circuits without any external node for test. This lack of accessibility makes the test of these blocks a challenging task. The testing procedure should provide an interference-free environment for the block under test and not affect other blocks [2]. The cost of AMS test is a challenge in SOC design as well. Although the price of IC products has a downward trend, the testing cost for AMS functions continues to increase along with the development of new high performance circuits [3].

Extensive efforts from the industry and the academia have been spent on the test problem for more than a decade. Linear modeling approaches were proposed to reduce the test complexity and shorten the test time [4, 5]. On chip test functions were designed to eliminate the need for external testers [6]. Recently statistical analysis was incorporated into AMS test to improve the test accuracy [7]. Only a limited number of examples are listed above, but all these works corroborate the importance of the test problem and the necessity for further works on it. *The International Technology Roadmap for Semiconductors* identified AMS test as one of the four "most daunting SOC challenges" and indicated that the problem of "Manufacturing test for AMS circuits is essentially unsolved" [1].

The bottleneck of AMS test is the instrumentation of high precision signal generators and response measurement devices. The common wisdom of test is "garbage in, garbage out." Only if a highly accurate signal is fed into a device under test (DUT), the measured response will represent the true performance of the DUT. Conventional production test takes a "platinum in, gold out" approach. The signal generation and measurement functions of commercial testers usually have a much better performance than the specification of DUTs so that the test errors could be controlled at an acceptably low level. These testers are more expensive and challenging to design than most DUTs and unable to test DUTs with comparable performance. Most of the existing solutions to AMS test adopt a "gold in, gold out" approach. They are looking for methods to design on-chip precision instruments that require minimal time and efforts and use them in test. However, implementation of these solutions for testing high-performance IC products is still a non-trivial challenge.

This paper provides an essentially different approach for high-precision AMS test which uses cost-effective signal generators as stimuli. The proposed approach will be presented in Section 2. A linearity test algorithm for high precision ADCs will be studied as an application of the proposed approach in Section 3. Section 4 will discuss

the simulation results of the ADC test algorithm. Section 5 will conclude the paper.

2. A COST-EFFECTIVE HIGH-ACCURACY TEST APPROACH FOR AMS CIRCUITS

Instead of following the "gold in, gold out" style, we propose an AMS test approach using low-accuracy but easy-to-generate test signals and computation-efficient identification algorithms. We call it a "garbage in, gold out" approach as illustrated in Figure 1.

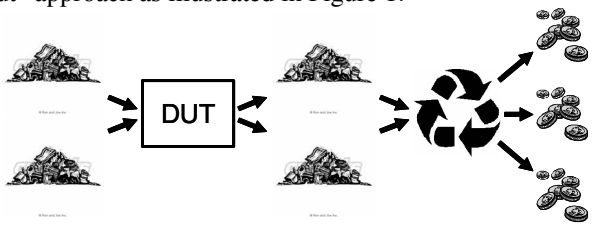

Figure 1 AMS test using organized "garbage" stimuli.

The common wisdom of "garbage in, garbage out" is true in the sense that the captured response of a DUT is contaminated by errors in test signals and does not accurately represent the performance of the DUT [8]. However, the captured response is not useless. It contains the DUT's characteristic information masked by stimulus errors. Feeding a set of organized low-accuracy signals into a DUT, we will get a set of organized low-accuracy responses. By appropriately manipulating the organized outputs, we can recover the masked DUT characteristics.

Since low-accuracy signals can be easily and fast generated, the cost and complexity of AMS test can be dramatically reduced by using the proposed approach. Furthermore, the low-accuracy signal source can be integrated on the same chip as the functional block under test with little area overhead, which makes the proposed approach a promising solution to SOC design and BIST problems.

Selection of the type and number of organized low-accuracy test signals are strongly dependent on the nature of the DUT, but authors' previous works demonstrated the feasibility of the proposed approach. A linearity test approach for precision ADCs was introduced in [9]. Experimental results showed ADC performance can be accurately tested by using two easy-to-generate signals. The computational efficiency of the algorithm in [9] is very attractive. The whole algorithm implemented on a PC adds a little data processing time to the data capture time which is dramatically less than the data capture time of conventional approaches. Short test time is another contributor of the proposed approach towards saving the cost of AMS test. The achievements of high-accuracy ADC test in [9] indicated that the proposed approach can do the job of collecting the "gold" from the "garbage." Next section will introduce another algorithm for testing a more general class of ADCs by using the proposed approach.

3. A STIMULUS ERROR IDENTIFICATON AND REMOVAL ALGORITHM FOR ADC TEST

We first give the symbols and acronyms used throughout.

k: ADC output code
N: Number of distinct output codes of an ADC
T_k: Transition point between code k-1 and k
W_k: Code bin width of code k
INL_k: Integral nonlinearity at code k
INL: Integral nonlinearity, maximum of $|INL_k|$
$x(t)$: Equivalent input signal
H_k: Bin count for code k
t_k: Transition time associated with T_k
a_j: Coefficient of j^{th} harmonic in the test signal
β: Attenuation factor

Sine waves have been used in ADC linearity test for more than 20 years because of its low distortion [10]. However, it becomes more and more challenging to generate pure enough sine waves for high-resolution ADC test. The stimulus error identification and removal (SEIR) algorithm introduced in this section allows engineers to use low-linearity easy-to-generate sine waves for testing ADCs. The SEIR algorithm will first identify and remove the effects of the distortions in a sine wave on the captured data and then accurately characterize ADC's linearity.

An ADC's linearity is defined by its transition point T_k's [9]. ADC's linearity test focuses on determining the values of T_k's. This test is usually done in the time domain using the following relationship

$$T_k = x(t_k). \tag{1}$$

$x(t)$ is an equivalent signal determined by the shape of the actual test stimulus. It is an increasing ramp for a saw tooth or triangular wave actual test signal. It is an increasing half period of a cosine wave if the actual test signal is sinusoidal. Transition time t_k is defined to be the time at which $x(t)$ is equal to T_k. If $x(t)$ is known and t_k's are measured, T_k's can be determined by using Eq. (1). By using a pure sinusoidal test signal, the transition point of an ADC can be estimated as [10]

$$\hat{T}_k = -\cos(\pi \hat{t}_k), \tag{2}$$

where the estimated value of the transition time is

$$\hat{t}_k = \sum_{j=0}^{k} H_j \Big/ \sum_{j=0}^{N-1} H_j. \tag{3}$$

H_k's in Eq. (3) are bin count data collected by using the pure sine wave test signal. If the input signal has harmonic distortions, Eq. (2) no longer holds and needs to be modified. Because of the distortions, we have to use different equivalent signals for the rising and falling segments of a sine wave. If we include only the bin counts from the rising (or falling, but not both) segments of a sine wave in Eq. (3) and consider the harmonic distortions, an

equation relating the transition point and transition time can be written as

$$\hat{T}_k = -\cos(\pi \hat{t}_k) + \sum_{j=2}^{M} a_j \cos(j\pi \hat{t}_k), \quad (4)$$

where a_j's are coefficients of the harmonics in the sine wave. Usually Eq. (4) is not sufficient to estimate T_k's since a_j's are unknown and they may mask the true value of transition points.

The SEIR algorithm uses two sine waves to test an ADC, one sine wave being an attenuated version of the other. The attenuation factor is unknown and will be estimated by the SEIR algorithm. Using these two signals, we can collect two sets of histogram data $H_{k,1}$ and $H_{k,2}$ and get two sets of estimated transition time $\hat{t}_{k,1}$ and $\hat{t}_{k,2}$ using Eq. (3). Substituting these estimated values into Eq. (4), we get two estimates of transition point T_k as

$$\hat{T}_{k,1} = -\cos(\pi \hat{t}_{k,1}) + \sum_{j=2}^{M} a_j \cos(j\pi \hat{t}_{k,1}) \quad (5)$$

and

$$\hat{T}_{k,2} = \beta\left[-\cos(\pi \hat{t}_{k,2}) + \sum_{j=2}^{M} a_j \cos(j\pi \hat{t}_{k,2})\right] + d, \quad (6)$$

where β is the unknown attenuation factor. The term d models a possible offset between the two sine waves. Since the two histograms are from a same ADC, the two estimates in Eq. (5) and (6) have to be the same. By equating the two estimates, we get an equation involving only the sine wave parameters as

$$\begin{aligned} &\beta\cos(\pi \hat{t}_{k,2}) - \cos(\pi \hat{t}_{k,1}) \\ &= \sum_{j=2}^{M} a_j\left[\beta\cos(j\pi \hat{t}_{k,2}) - \cos(j\pi \hat{t}_{k,1})\right] + d. \end{aligned} \quad (7)$$

Eq. (7) is linear in a_j's. If β is known, a_j's can be estimated from the huge number of Eq. (7) for k=1, 2… N-3, using the standard least squares (LS) method. We will show β can be estimated together with a_j's. Let β' be a tentative value of β with an error $\Delta\beta$ such that

$$\beta = \beta' + \Delta\beta. \quad (8)$$

Substituting Eq. (8) into Eq. (7) gives

$$\begin{aligned} &\beta'\cos(\pi \hat{t}_{k,2}) - \cos(\pi \hat{t}_{k,1}) \\ &\approx \sum_{j=2}^{M} a_j\left[\beta'\cos(j\pi \hat{t}_{k,2}) - \cos(j\pi \hat{t}_{k,1})\right] - \Delta\beta\cos(\pi \hat{t}_{k,2}) + d, \end{aligned} \quad (9)$$

with the product term of $\Delta\beta$ and sine wave harmonic errors neglected because they are small numbers. The values of $\Delta\beta$ and a_j's, and d which is of no interest, can be estimated from Eq. (9) using the LS method. It can be shown that the true value of β minimizes $|\Delta\beta|$. So by scanning a possible range of β, the $\hat{\beta}$ that gives the smallest $|\Delta\beta|$ is the optimal estimate of β, and the associated $\hat{a}_j$'s give an optimal estimate of the harmonic errors in the test signal. Simulation shows that this calculation takes very short time. By substituting $\hat{a}_j$'s into Eq. (5), transition points of the ADC can be estimated as

$$\hat{T}_k = -\cos(\pi \hat{t}_{k,1}) + \sum_{j=2}^{M} \hat{a}_j \cos(j\pi \hat{t}_{k,1}). \quad (10)$$

Thus INL_k's and INL of the ADC can be estimated by their definitions

$$\hat{INL}_k = \frac{\hat{T}_k - \hat{T}_0}{\hat{T}_{N-2} - \hat{T}_0}(N-2) - k \quad (11)$$

and $$\hat{INL} = \max_k\{|\hat{INL}_k|\}. \quad (12)$$

Since the SEIR algorithm has no specific requirement on the DC component of the two test signals, it can be used to test fully differential ADCs with stimuli AC coupled to the input nodes, for which a DC offset algorithm does not work.

4. SIMULATION RESULTS

Extensive simulations have been done in Matlab on personal computers to validate the performance of the SEIR algorithm. The simulation was set up for testing 16-bit pipelined ADCs using sine waves. The harmonic errors in a sine wave were randomly generated. The spectrum of a sine wave used in simulations is plotted in Fig. 2. It has a 38-dB SFDR with the largest distortion at the 3rd harmonic. Harmonic distortions in simulations were purposely set at a high level to test the algorithm. Much better sine waves can be practically generated using simple band-pass filters. Sub-sampling together with coherent sampling was employed in simulations, since it is an industry standard for sine wave test using high frequency stimuli [11]. The attenuation factor was nominally 1.05 with a random error which was unknown to the algorithm. The attenuation can be practically implemented by a simple voltage dividing network. An additive noise of 1-LSB standard deviation was added to sine waves for modeling the ADC's input referred noise.

Common error sources, such as gain errors, offset errors and reference voltage errors, were modeled for pipelined ADCs in simulations. The simulated INL_k of a 16-bit ADC is given in black on the top of Fig. 3. This ADC has a 2.5-LSB INL. Then we fed the low-purity sine wave shown in Fig. 2 and an attenuated version of it to the ADC and collected two sets of bin counts. By applying the SEIR algorithm, we identified the INL_k of the ADC as plotted in red on the top of Fig. 3. The true and estimated INL_k plots are very close to each other. The difference between them is plotted on the bottom of Fig. 3. The maximum error in INL_k estimation is 0.6 LSB. From Fig. 2 and 3 we can see that 16-bit accuracy was achieved in ADC test by using sine waves of a 38-dB SFDR, which is corresponding to about 6-bit linearity.

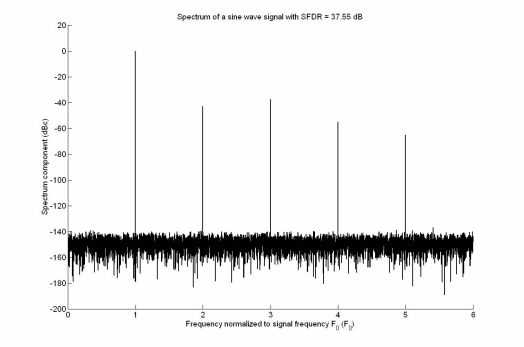

Figure 2 Spectrum of a simulated sine wave testing signal.

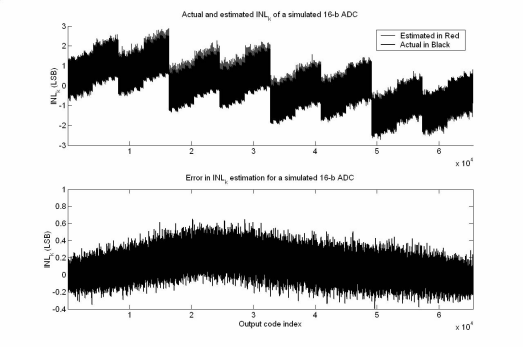

Figure 3 INL testing for a simulated 16-bit ADC.

The simulation was repeated for sine waves with various harmonic distortions. The maximum errors in INL_k estimation for different runs are plotted with respect to the SFDR of sine waves in Fig. 4. From the figure we can see the errors for more than 90% of the runs are less than 1 LSB, and those few larger ones are under 1.1 LSB. 16-bit test performance is achieved regardless of the SFDR of sine waves from 35 dB to 65 dB.

5. CONCLUSION

The SEIR algorithm can test ADCs to 16-bit accuracy using sine wave signals with only 6-bit linearity performance. This algorithm does not require expensive signal generators and is applicable to high-precision and high-speed ADCs. The achievement of the SEIR algorithm strongly suggests the potential of the proposed "garbage in, gold our" approach for testing high-precision AMS systems. Cost-effective test methods using easy-to-design and manufacture circuits and computationally efficient error removal algorithms can be developed based on the proposed approach for other AMS circuits such as DACs and filters. These test functions can be easily incorporated into SOC design and BIST because of the low overhead of the silicon area and test time.

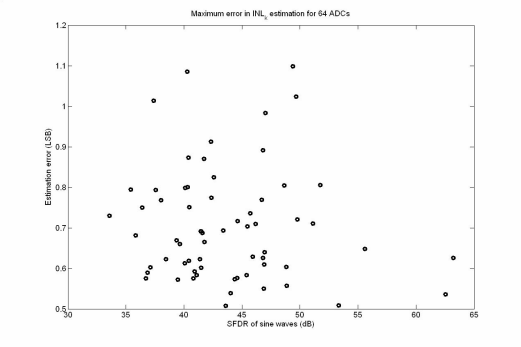

Figure 4 Maximum error in INL_k estimation for 64 ADCs.

6. REFERENCES

[1] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 2001 Edition and 2002 Update*, available online at http://public.itrs.net/.

[2] Y. Zorian, E.J. Marinissen, and S. Dey, "Testing Embedded-Core Based System Chips," *Proc. 1998 International Test Conference*, pp. 130-143, Oct. 1998.

[3] G.W. Roberts, "Improving the testability of mixed-signal integrated circuits," *Proc. IEEE 1997 Custom Integrated Circuits Conference*, pp. 214-221, May 1997.

[4] T.M. Souders and G.N. Stenbakken, "A comprehensive approach for modeling and testing analog and mixed-signal devices," *Proc. 1990 International Test Conference*, pp. 169-176, Sept. 1990.

[5] P.D. Capofreddi and B.A. Wooley, "The use of linear models for the efficient and accurate testing of A/D converters." *Proc. 1995 International Test Conference*, pp. 54-60, Oct. 1995.

[6] M. Hafed, N. Abaskharoun, and G.W. Roberts, "A stand-alone integrated test core for time and frequency domain measurements," *Proc. 2000 International Test Conference*, pp. 1031-1040, Oct. 2000.

[7] S. Max, "Ramp testing of ADC transition levels using finite resolution ramps," *Proc. 2001 International Test Conference*, pp. 495-501, Oct. 2001.

[8] K. Parthasarathy, T. Kuyel, D. Price, L. Jin, D. Chen, and R. Geiger, "BIST and Production Testing of ADCs Using Imprecise Stimulus," *ACM Trans. Design Automation of Electronic Systems*, Vol. 8, No. 4, pp. 522-545, Oct 2003

[9] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. L. Geiger, "Linearity Testing of Precision Analog-to-Digital Converters Using Stationary Nonlinear Inputs," *Proc. 2003 International Test Conference*, pp. 218-227, Oct 2003.

[10] J. Doernberg, H.-S. Lee, and D.A. Hodges, "Full-Speed Testing of A/D Converters," *IEEE J. Solid-State Circuits*, Vol. Sc-19, No. 6, pp. 820-827, Dec. 1984.

[11] T. Kuyel, "Linearity Testing Issues of Analog to Digital Converters," *Proc. 1999 International Test Conference*, pp. 747-756, Oct. 1999.