The SRE/SRM Approach for Spectral Testing of AMS Circuits

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ABSTRACT

Cost effective testing of analog and mixed-signal components is considered by the ITRS as one of four most daunting SoC challenges. Spectral testing is of critical importance to a large class of integrated circuits and is particularly challenging for high speed and/or high resolution circuits. This paper presents a new spectral testing methodology, termed the SRE/SRM approach, which uses low-cost Spectrally Related Excitations (SRE) and/or Spectrally Related Measurements (SRM) to accurately determine the spectral performance of AMS circuits. This approach can be used in both production test and built-in-self-test (BIST) environments. Simulation results show that sources or measurement devices with 9-10 bit accuracy can be used to accurately test high resolution CUTs with actual spectral performance as high as over 104 dB SFDR.

1. INTRODUCTION

Mixed-signal ICs and systems on a chip (SoC) are emerging as major technology drivers for the future of the semiconductor industry. The International Technology Roadmap for Semiconductors (ITRS) [1] identifies systems on-a-chip (SoC) and analog and mixed-signal (AMS) as two of the three system drivers for future semiconductor technology. In fact, analog components such as ADCs and DACs have become an integral part of the chip industry mainstream products. The increased complexity, increased performance, and reduced access to internal circuit nodes make testing these devices a major challenge [2]. The high-precision excitation signals and high-precision measurement devices required in existing approaches for accurate parametric testing of AMS functionalities are great challenges to obtain in a production test environment and are impossible in a built-in self-test (BIST) environment. The ITRS authors state "Developing cost-effective test methodologies and techniques for analog and mixed-signal components is therefore an essential part of devising a complete solution for testing of heterogeneous SoCs". The ITRS also identifies "Development of SoC test methodology" as one of the four "most daunting SoC challenges."

Many attempts have been made to provide BIST solutions to AMS testing to reduce costs associated with using testers and to enable testing of deeply embedded SoCs. Excellent examples include the work of Roberts, Sunter, Azais, Arabi, Sanchez, and many others [3-8]. Invariably, their approaches have been aimed at replicating a standard tester on a chip but unfortunately have found little industrial adoption. A fundamental difficulty in implementing such approaches is the need for a highly accurate signal to stimulate the circuit under test (CUT). Requirements for this stimulus input are typically substantially more precise than those of the CUT making the signal generator more challenging to design than the CUT itself and raising the question of whether a test circuit is also needed for the signal generator! Despite the extensive research effort from both industry and academia, the ITRS concludes that "manufacturing test for AMS circuits is essentially unsolved."

Abandoning the "accurate excitation and measurement" paradigm, the authors' group recently developed a drastically different approach for ADC static linearity testing, in which the highly precise input signal is replaced by two functionally related easy-to-generate signals. System identification and signal processing techniques are used to isolate input nonlinearities from device nonlinearities and to test the ADC accurately. Several algorithms have been developed for ADC linearity testing. One such algorithm was validated at Texas Instruments in which 7 bit linear signals were used to test a 16 bit ADC achieving 16 bit level testing performance [9].

In high-speed applications, spectral measures such as SFDR, SINAD, THD, IMD, SNR, etc. are of critical importance. For accurate spectral testing, input sine wave signals ideally should have spectral purity far exceeding the targeted performance of the CUT. However, in bench or production tests, practical sine waves generated by test equipment and practical measurement devices are not necessarily distortion-free. To ensure accurate testing, the IEEE standard as well as state of the art industry testing technologies requires that distortion in the input signal and in the measurement device must be significantly lower than the tolerable nonlinearity errors in the CUT. For example, a circuit with targeted 18-bit SFDR performance can tolerate distortions at or below the –110 dB level. The input sine wave signal and the measurement device should then have distortion components at the –130 dB level or lower. Such requirements are extremely difficult to satisfy, especially at very low or very high frequencies. In a BIST environment, they are even more difficult.

In this paper, we introduce a new spectral performance testing technology, termed the SRE/SRM approach, which uses two or more low-cost Spectrally Related Excitations, instead of distortion-free excitations, and/or two or more Spectrally Related Measurements using low-cost measurement devices, instead of distortion-free measurements, to accurately determine the spectral performance of the CUT. The SRE/SRM approach uses the spectral relationship between two or more input sinusoids or between measurement devices to separate or isolate the distortion inherent in the CUT from that in the test equipment. Computationally efficient DSP algorithms will be used to determine the true spectral performance of the CUT from SRM data. This approach eliminates the need for bulky and expensive signal generation and filtering circuitry and highly accurate measurement devices, and can be used in both production test and BIST environments. Simulation results show that sources or measurement devices with 9-10 bit accuracy can be used to accurately test high resolution CUTs with actual spectral performance as high as over 104 dB SFDR.

2. Spectral Testing of AMS Circuits

Consider the testing set up shown in Figure 1. The CUT represents an analog and mixed-signal circuit whose spectral

performance needs to be tested. The dynamic behavior of the CUT can be in general described by a set of differential and algebraic equations (DAEs) in the form:

$$\dot{x} = f(x,z,p,u);\ g(x,z,p,u) = 0;\ y = h(x,z,p,u) \quad (1)$$

where u is the input and y is the output of the CUT, x is the vector of state variables, z is a vector of network variables, p is a vector of circuit parameters, and all variables lie in their respective compact sets. The functions f, g, h are piecewise continuously differentiable with respect to all of their arguments. When p is at its nominal value p_0, the CUT is an exponentially stable linear time-invariant (LTI) causal system. When p differs from p_0, the CUT becomes a nonlinear dynamical system. If the variation is small, which is the case for high performance systems, the CUT will remain exponentially stable.

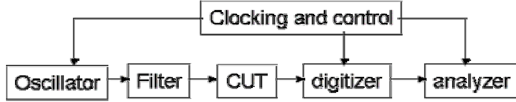

Figure 1 Spectral testing set up

Under the above conditions, when the input is a bounded periodic signal, a dynamical systems theorem states that all variables in the CUT will settle into a periodic solution with the same period as the input. In particular, if $u(t)=u_0(t)=\sin 2\pi f_i t$, the CUT output y has the Fourier Series form (base normalized)

$$y_c(t) = \sin 2\pi f_i t + \sum_{k=2}^{\infty} (h_{ck} e^{2\pi k f_i t} + \bar{h}_{ck} e^{-2\pi k f_i t}) \quad (2)$$

Then the h_{ck}'s are called the distortion spectrum of the CUT. In particular, the spurious free dynamic range (SFDR) and total harmonic distortion (THD) of the CUT are defined by

$$THD = 10\log_{10}\left(\sum_{k=2}^{\infty} |2h_{ck}|^2\right) \quad (3)$$

$$SFDR = -20\log_{10}\left(\max_{k\geq 2} |2h_{ck}|\right) \quad (4)$$

According to the SFDR and THD definition, the input signal to the CUT should be a pure sine wave and the output of the CUT should be directly used in the Fourier analysis, meaning that the digitizer should not introduce noticable errors. Because of this, the IEEE standard and industry practice require that the spectral distortions in the excitation sinusoidal and in the output digitizer should be at least 10 times or 3 bits better than the targeted spectral performance of the CUT. For medium to high performance CUTs, this requirement imposes challenges on the test environment. In particular, very high performance digitizers are required to capture the CUT output waveform and very pure input sine waves are needed to excite the CUTs. When the targeted spectral performance of the CUT is high, such requirements become very challenging and the test equipment becomes very expensive, leading to long test time and high testing costs. For some of the very high end products, testing equipment meeting the desired requirements are not readily available from ATE venders. For example, if a CUT has a targeted spectral performance of 17 bits or more, its SFDR would be 104 dB or more, and the test equipment should have distortions of -124 dB or less. This is very challenging, if possible at all. For deeply embedded AMS functionalities in SoC scale circuits, providing such high performance signal sources and measurement devices on chip with limited die area for BIST solutions is significantly more challenging.

3. The SRE/SRM Approach for AMS Spectral Testing

Contrast to the standard testing paradigm described above, we propose the SRE/SRM (spectrally related excitation/spectrally related measurement) approach to spectral testing of AMS circuits. In this approach, two or more spectrally related low-accuracy sinusoidal signals that can be easily generated will be used as the stimulus input to the CUT, instead of the traditional high-precision sinusoidal signals. This is shown in Figure 2. The SRE signal generator can use a simple DAC or a cheap oscillator, with much poorer spectral performance than the CUT, to generate the first low-accuracy signal. That signal can be passed through a simple filter, such as a first order low-pass RC filter, to generate a second low-accuracy signal that is spectrally related to the first signal. If necessary, additional spectrally related low-accuracy signals can be easily generated with different simple filters. For capturing the output of the CUT, two or more spectrally related measurements will be taken using inexpensive measurement devices, instead of using high-performance waveform digitizers as in the traditional approach. The SRM digitizer in Figure 2 is used to take spectrally related measurements m_1 and m_2. The measurement device could be a really inexpensive ADC, say a pipeline ADC with many stages built within a small die area, with much poorer spectral performance than the CUT. The output of the CUT can be directly digitized by the inexpensive ADC to obtain the first measurement, and then passed through a simple (could be first order RC) filter before digitization to obtain the second measurement that is spectrally related to the first measurement. The spectral relationship among the SRE signals and among the SRM measurements will be used together with digital signal processing algorithms to separate the distortion components of the CUT from those from the signal source and from the measurement device. Once the spectral components from the CUT are separated from those of the testing environment, the spectral performance of the CUT can be accurately computed without being affected by the errors from the inexpensive signal source or from the low-accuracy measurement device.

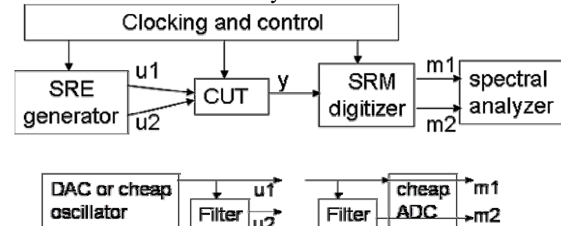

Figure 2 SRE/SRM testing set up

Specifically, let $u_1(t) = u_0(t) + \Delta u_1 = \sin 2\pi f_i t + \sum_{k=2}^{\infty} (h_{u1k} e^{2\pi k f_i t} + \bar{h}_{u1k} e^{-2\pi k f_i t})$. Since 9~10 bit pure sine waves are easy to generate, we assume Δu to be at the 0.1% to 0.2% level. Since u_1 is periodic, from the same dynamical systems theorem all variables in the CUT will be periodic in steady state. Furthermore, the difference between the new solution and the previous solution can be obtained through a linear sensitivity system in the form

$$\Delta\dot{x}_1 = A\Delta x_1 + B\Delta u_1;\quad \Delta y_1 = C\Delta x_1 + D\Delta u_1 \quad (5)$$

where A, B, C, D are sensitivity matrices evaluated along the nominal solutions when Δu is zero. In general this linear system will be time varying. However, under the assumption the CUT is a LTI system when p is at it nominal value, the linear sensitivity system will be LTI. In this case, (5) yields $\Delta y_1 = H(s)\Delta u_1$, where H(s) is the transfer function of the sensitivity system. The CUT's

output y_1 due to u_1 will be, in the first order approximation,

$$y_1(t) = y_c(t) + \Delta y_1 = \sin 2\pi f_i t + \sum_{k=2}^{\infty}(h_{ck}e^{2\pi k f_i t} + \bar{h}_{ck}e^{-2\pi k f_i t})$$
$$+ \sum_{k=2}^{\infty}(H(j2\pi k f_i)h_{u1k}e^{2\pi k f_i t} + \bar{H}(j2\pi k f_i)\bar{h}_{u1k}e^{-2\pi k f_i t}) \quad (6)$$

Following the same steps, we can arrive at a similar expression for $y_2(t)$, the output due to u_2, with h_{u1k} replaced by h_{u2k}.

In the SRE approach, u_2 is related to u_1 through simple filtering. Suppose the filter is adjusted so that u_1 and u_2 will have the same magnitude. Furthermore, assume that the measurement is synchronized so that when measuring y_2 the time origin is also at a positive zero crossing of the sine wave. These are assumptions that are typically maintained when taking a measurement. Under these conditions, the spectral components of u_2 are related to the spectral components of u_1 through the filter relationship and we can write $u_2(t) = u_0(t) + \Delta u_2 = \sin 2\pi f_i t + \sum_{k=2}^{\infty}(F_1(j2\pi k f_i)h_{u1k}e^{2\pi k f_i t} + \bar{F}_1(j2\pi k f_i)\bar{h}_{u1k}e^{-2\pi k f_i t})$ and $h_{u2k}=F_1(j2\pi k f_i)h_{u1k}$. We can then have,

$$y_2(t) = y_c(t) + \Delta y_2 = \sin 2\pi f_i t + \sum_{k=2}^{\infty}(h_{ck}e^{2\pi k f_i t} + \bar{h}_{ck}e^{-2\pi k f_i t})$$
$$+ \sum_{k=2}^{\infty}(H(j2\pi k f_i)F_1(j2\pi k f_i)h_{u1k}e^{2\pi k f_i t} + \bar{H}(j2\pi k f_i)\bar{F}_1(j2\pi k f_i)\bar{h}_{u1k}e^{-2\pi k f_i t}) \quad (7)$$

Subtracting (7) from (6), we have

$$y_1 - y_2 = \sum_{k=2}^{\infty}(H(j2\pi k f_i)(1 - F_1(j2\pi k f_i))h_{u1k}e^{2\pi k f_i t}$$
$$+ \bar{H}(j2\pi k f_i)(1 - \bar{F}_1(j2\pi k f_i))\bar{h}_{u1k}e^{-2\pi k f_i t})$$

Notice that in this equation, the spectral distortion components h_{ck} due to the CUT nonlinearity do not appear. This is a set of equations involving the source nonlinearities and the CUT output data. Taking the spectrum difference between the two measurements, we will have,

$$h_{y1k} - h_{y2k} = (1 - F_1(j2\pi k f_i))H(j2\pi k f_i)h_{u1k}$$

which can be used to solve for the distortion components in y_1 that is contributed by the source error Δu_1 as follows:

$$H(j2\pi k f_i)h_{u1k} = (1 - F_1(j2\pi k f_i))^{-1}(h_{y1k} - h_{y2k})$$

Once this has been computed, it can be substituted back in the spectrum of y_1 to compute the CUT's spectral distortion components as follows:

$$h_{ck} = h_{y1k} - H(j2\pi k f_i)h_{u1k}$$

Therefore we have derived a method for separating the spectral distortion components due to the signal source from those due to the CUT and computing them separately based on the SRE approach. Similarly, let $y(t)$ be any output signal from the CUT (y_c, or y_1 or y_2) and m_1 and m_2 be the two SRM measurements for $y(t)$ with filter $F_2(s)$, then we can derive the following formula (details neglected due to space limitations):

$$h_{yk} = (1 - F_2(j2\pi k f_i))^{-1}(h_{m1k} - h_{m2k})$$

4. Simulation Results

To evaluate the SRE/SRM approach to spectral testing of AMS circuits, it suffices to evaluate the SRE approach for ADC testing (no measurement device is needed since the ADC output is digital) and the SRM approach for DAC testing (no signal generator is needed since a DAC takes digital input codes). For ADC testing, we considered a high-resolution flash structure because it has more independent error sources and is more challenging to fully characterize than other structures. Specifically, an imperfect 16-bit flash ADC is generated assuming random resistor mismatch in the R-string. Using an ideal sinusoid and FFT, the true spectral performance of the ADC is determined through simulation.

To evaluate the SRE approach, simulated low-purity sine waves were used as the input signals to test the ADC's spectral performance. To do this, harmonic distortion components were added to a pure sine wave to form our first input signal $x_1(t)$ whose spectrum is shown in Figure 3.

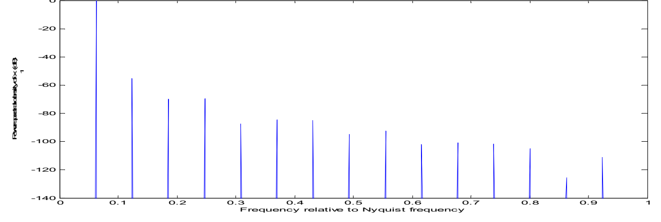

Figure 3. Spectrum of imprecise sinusoidal input signal

As can be seen, this $x_1(t)$ has its second harmonic power at –55 dB relative to the full-scale signal power. That means the purity of $x_1(t)$ is only 55 dB, or about 9-bit pure. The corresponding steady state ADC output signal $y_1(t)$ was recorded and coherent samples were taken for use in FFT. The spectrum of $y_1(t)$ is displayed in Figure 4. If standard procedures for ADC spectral testing were to be followed with this data record, an incorrect conclusion would be drawn that the ADC under test had an SFDR equal to 55 dB. The true SFDR of the ADC is 104.0 dB as verified by ideal sinusoidal testing. The computed SFDR is basically the SFDR of the input signal itself. Hence we have verified that in the standard testing method, a low purity sine wave signal cannot be used as an excitation signal to test the spectral performance of the ADC.

In our algorithm, we use a second imprecise sine wave input. The second input is obtained by filtering the first imprecise sine wave through a simple low pass filter. By doing so, the spectra, or the harmonic distortions, of the two imprecise sine waves are related to each other through the filter transfer function. This known relationship will be used to correctly estimate the ADC's true spectral performance.

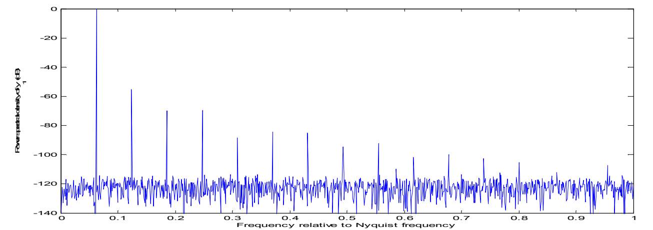

Figure 4. ADC output spectrum with $x_1(t)$ as input

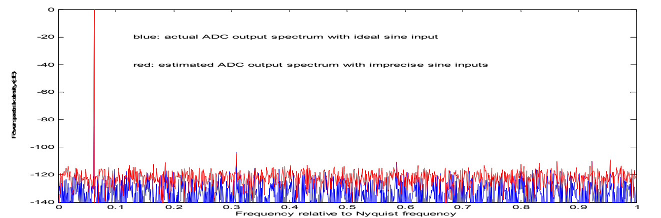

Figure 5. True and SRE estimated ADC spectrum

After we obtained the spectra of both $Y_1(f)$ and $Y_2(f)$, the SRE algorithm was used to calculate the SFDR of the CUT. Figure 5 plots both the true ADC spectrum, indicating 104.0 dB SFDR, and the estimated ADC spectrum from the SRE method, indicating 104.8 dB SFDR. It must be reminded that the accurate SFDR

result was obtained with input signals with only 9-bit purity. This compares with the industry standard which will require an input signal whose purity is 124 dB or 21-bit pure.

For SRM based DAC testing, we considered a 15-bit thermometer coded current steering DAC. A digitizer with sufficient resolution but low linearity was used as the measurement device. The true spectrum of the digitizer is depicted in Figure 6. It can be seen the measurement device has 65.68 dB or 10.5-bit SFDR performance. It was also verified that the digitizer has 9.5-bit INL static linearity. When a digital sine wave sequence is input to the DAC under test, the DAC output is digitized. The straightforwardly computed spectrum of the digitized data is shown in Figure 7. It incorrectly shows an SFDR of only 65.33 dB. This low SFDR reading is mainly due to corruption by the distortion in the measurement device.

In the SRM approach, the DAC output is filtered and digitized by the same digitizer again. The combined data from both SRM measurements are processed by the SRM testing algorithm. The estimated DAC spectrum, after removing the error of the nonlinear measurement device, is illustrated in Figure 8. Also plotted in Figure 8 is the DAC spectrum computed based on data collected with an ideal digitizer. It can be seen that both spectra suggest similar high readings of SFDR. In fact, the printed out data show that the true SFDR of the DAC is 93.54 dB and the SRM estimated DAC SFDR is 93.43 dB. Again, we emphasize that the accurately estimated SFDR results were obtained with a measurement device that has only 9-10 bit linearity. In comparison, standard industry practice would require a waveform digitizer with a minimum of 114 dB or 19-bit linearity.

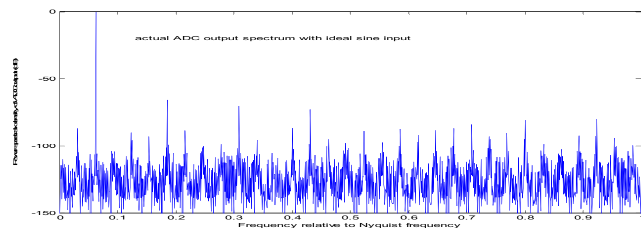

Figure 6. True spectrum of the measurement device ADC

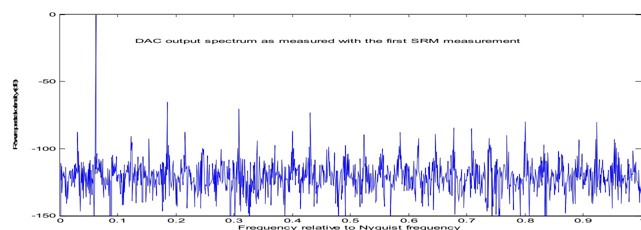

Figure 7. DAC spectrum corresponding to the first SRM

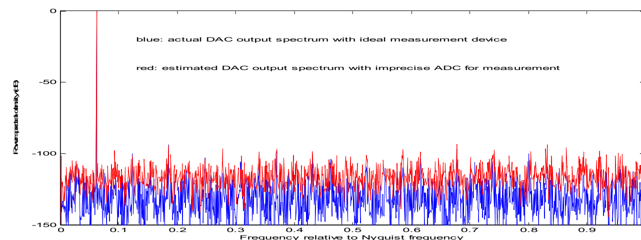

Figure 8. True and SRE estimated DAC spectra

5. Conclusion

We have presented the SRE/SRM approach to accurate spectral testing of high performance AMS circuits using inexpensive signal generators and measurement devices. Simulation results demonstrate that 9-10 bit accurate sinusoidal sources, which are readily realizable with a small die area, can be used in a SRE algorithm to accurately test the spectral performance of 16 bit ADCs, and 9-10 bit linear ADCs can be used in a SRM framework to accurately test the spectral performance of DACs with 15 bit or higher resolutions. Because of the dramatically relaxed requirement on the signal generators and the measurement devices, the SRE/SRM approach can significantly reduce the testing cost associated with the high-precision testing equipment as well as the cost associated with running and maintaining a high precision testing environment. The SRE/SRM testing approach can offer immediate solutions to production test needs with substantially lower cost without sacrificing testing accuracy. It also offers a testing solution to certain high performance parts for which there exist no viable spectral testing solutions currently. More significantly, the relaxed sources and measurement devices can be easily implemented on chip and the signal processing tasks can be carried out using on-chip DSP capabilities available in a SoC scale circuit. Therefore, the proposed algorithms offer the potential to be fully integrated in to a BIST solution to reduce or eliminated the need for standard production tests.

6. References

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