Testing High Resolution ADCs with Low Resolution/Accuracy Deterministic Dynamic Element Matched DACs[†]

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Abstract

This paper presents a Deterministic Dynamic Element Matching (DDEM) approach which is applied to low precision DACs to generate stimulus signals for ADC testing. Both simulation results and experimental results from a fabricated DDEM DAC are presented to verify the performance. The ADC testing performance of an 8-bit DDEM DAC (linearity less than 5 bits without DDEM) is comparable to or better than the best results reported in the literature using on-chip linear ramp generators. The DDEM technique offers great potential for use in both production test and built-in-self-test(BIST) environments.

1. Introduction

The most common and widely use mixed-signal circuits are digital to analog converters (DACs) and analog to digital converters (ADCs) [1]. Data converters are widely used because they serve as the interface between digital logic and the analog or physical world. Due to increasing resolution and conversion rates, the challenge and cost of testing analog to digital converters (ADCs) is growing. Testing techniques that facilitate a reduction in the cost of test or that support Built-in-Self-Test (BIST) will have a significant impact in the final product costs [2].

BIST structures for analog and mixed-signal circuits offer the potential to reduce cost while also providing a capability to test deeply embedded systems on a chip (SOCs). BIST schemes can also be used for self-calibration [3] and hence improve circuit performance. Most existing BIST approaches have been aimed at replicating a standard tester on chip [4-11], which leads to the requirement of on chip generation of a highly accurate and linear stimulus. However, prior arts have not demonstrated linearity adequate for testing moderately high resolution ADCs in a BIST setup.

A different approach was introduced recently [3] [12-14], where the linearity requirements on the signal generator are relaxed by orders of magnitudes through the use of multiple inputs and appropriate DSP techniques to accurately characterize the DUT. In this paper an alternative approach is described that uses DDEM on low linearity DACs to generate a statistically linear source for testing highly-linear ADCs. No special signal processing is needed and the standard code-density test techniques can be directly used.

DACs are commonly used to generate input signals for ADC testing. The performance of most DAC architectures is dependant on the matching properties of critical elements. Due to process variations, element matching errors are inevitable. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases and are difficult to use in a BIST environment. The DEM technique, first introduced by Van De Plassche in 1976 [15], accepts matching errors as inevitable and dynamically rearranges interconnections among mismatched elements so that on the average all element values are nearly equal. The DEM method was used by Jensen and Galton [17, 18] to improve the effective linearity specifications of DACs. It has been demonstrated that DEM can be used to appreciably improve the SFDR performance of moderately low-linearity DACs [17] by spreading the errors in the DAC over a wide frequency spectrum. This behavior is a direct consequence of the randomizing effect provided by DEM.

Other researchers [19-24] have used DEM in Delta-Sigma Converters and the high over-sampling ratio inherent in these structures can either partially or totally remove the limitations associated with the time-local errors. Leung and Sutarja presented three different approaches to DEM in [19]: Conventional Random Averaging, Clocked Averaging and Individual Level Averaging. The DEM was applied on a 3-bit DAC in a Delta-Sigma ADC. Baird and Fiez introduced and analyzed in [20] the Data Weighted Averaging (DWA) algorithm. Different

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modifications to the DWA are made in [21-23] to improve its performance. Adams and his colleagues present a Data-Directed Scrambler for multi-bit noise shaping D/A converters in [24]. Most of these DEM algorithms are input data dependent and are variants of the Data Dependant First use-Next use (DDFN) algorithm. None of these algorithms have been used for testing purpose and many known problems with these algorithms remain to be solved, such as the spectral spurious components generated by DEM, the large sampling window required and the time-local non-stationarity. In this paper we present a DDEM algorithm which is applied to ADC testing, where such problems do not affect the testing performance.

Our application of DDEM allows the signal generator to be realized with a low-linearity DAC, eliminating the need for large silicon area and greatly relaxing the design requirements of the stimulus signal generator. A preliminary study investigated the use of random DEM with a highly-nonlinear DAC to test low-resolution ADCs [25]. The idea behind DEM testing is to generate the ADC stimulus with more than one DAC output samples for a given DAC input digital word, each sample generated using different elements following the DEM philosophy. Since DEM is used in the input signal generator we do not have to worry about of the time-local nonstationarity caused by DEM in the signal path. DDEM was introduced, compared to the random DEM testing and theoretically analyzed in [26-28]. It was shown that DDEM significantly outperformed random DEM (RDEM) for a given number of samples per DAC code.

The rest of this paper is organized as follows. Basic notation on ADC integral nonlinearity (INL) characterization is given in Section 2. Section 3 presents details about the DDEM DAC structure, DDEM algorithm description and theoretical performance evaluation. Section 4 presents simulation results of testing 11-bit and 12-bit resolution ADCs using an 8 bit DDEM DAC. An 8-bit DDEM DAC design is described and experimental results are presented in Section 5.

2. INL Characterization

There are several alternative but similar definitions of the INL of an ADC. Some authors [29] define an INL function as a continuous function of the ADC input voltage, INL(Vin). Some other authors define an INL function from a discrete sequence denoted as INL_k determined by the transition points of the ADC. It is also common to define an INL function from a discrete sequence of output code densities obtained by exciting the ADC with a known test signal such as a ramp or sinusoid. In all cases, the total INL is defined to be the maximum magnitude of either the continuous or discrete INL functions and there is usually negligible difference in the INL obtained from any of the three definitions. In this paper, we follow what is the most common INL definition used by test engineers in industry. Specifically, the transition point, T_k, will be first estimated from code density outputs of the DUT generated from a characterized input signal. The INL_k of an ADC is defined as the error between a fit line and the actual transfer characteristics curve of the ADC at code *k*. The fit line is usually the end point fit line. Let n be the resolution of the ADC and $N=2^n$. If there are no missing codes in the ADC output, the ADC will have transition points at T_1, T_2, … T_{N-1}. The end-point fit line is then defined as the straight line connecting the first and the last transition points and is given by the expression:

$$y = 1 + \frac{(N-1)-1}{T_{N-1} - T_1}(x - T_1) \tag{1}$$

where x is the input voltage and y is the corresponding (fractional) output code. At code k transition point, $x = T_k$ and the definition of INL_k given above leads to

$$INL_k = 1 + \frac{N-2}{T_{N-1} - T_1}(T_k - T_1) - k = \frac{T_k - T_1}{T_{N-1} - T_1}(N-2) - (k-1) \tag{2}$$

Notice that with the end-point fit line, $INL_1 = INL_{N-1} = 0$.

A linear ramp is widely used in industry as the input signal to the ADC under test and the numbers of occurrences of each ADC output are tallied into corresponding code bins. Let H_k be the number of occurrences of code k. Since V_{in} is proportional to time and the sampling intervals are constant, the total number of accumulated samples for a linear ramp input is linearly proportional to V_{in}. Thus, a transition voltage is proportional to the accumulated code bin counts up to this transition and can be estimated from the corresponding code densities. From these estimates, an estimate of INL_k as given in (2) can be expressed as

$$INL_k \cong \overleftrightarrow{INL_k} = \frac{(\sum_{i=1}^{k} H_i) - H_1}{(\sum_{i=1}^{N-1} H_i) - H_1}(N-2) - (k-1), \; k = 1,2 \ldots N-1 \tag{3}$$

Tests using $\overleftrightarrow{INL_k}$ as the measured value of INL_k are often termed histogram based tests and the histogram-based method is widely used to test ADCs.

3. Deterministic Dynamic Element Matching

In this section, we will first briefly review the DAC structure that DDEM is applied to. Then the Cyclic DDEM sequence approach is described and its performance when applied to a DAC is evaluated.

The proposed DDEM approach will be explained using a 3-bit current steering thermometer-coded DAC as shown in Figure 1.

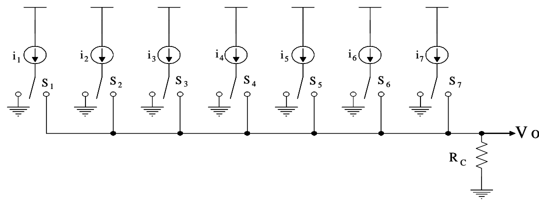


Figure 1 A 3-bit Current Mode Thermometer-Coded DAC

In this case, when all switches are connected to ground, the output corresponds to the digital word zero. To generate the output voltage for the digital 1, one switch needs to be connected to the output node. For a digital "k", any k of the switches needs to be connected to the output node. The resistor R_C is picked so that when all of the current sources are on, the voltage output is at the desired maximum.

The conventional random dynamic element matching idea for generating an output for a digital word "k" is to randomly pick k switches to be turned on each time an output corresponding to word k is desired. Multiple outputs are generated for each digital word 'k' with different randomly selected current sources.

The DDEM method deterministically picks the k current sources to be switched on. The deterministic pattern used attempts to distribute the sources to be switched on in such a way that all sources are used almost statically uniformly. For simplicity, one extra current source element has been added to the DAC in Figure 1 so that the DAC has a total of $N = 2^n$ current sources. An integer q is defined by the expression q = N/p where it is assumed p, the number of samples per DAC input code, is selected such that q is an integer.

Both the RDEM and DDEM approaches take advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static viewpoint, where the output of a DAC is used as the input to the ADC. The DAC's output for the same input digital word, using different randomly or deterministically chosen current sources, will be input to the ADC p times. The ADC's outputs corresponding to each one of the p input samples are then stored for calculating the ADC INL later. In this way, the real-time limitations are eliminated, and a statistically linear input signal can be generated as shown in the following sections.

The DDEM approach will be described and its performance will be evaluated theoretically and verified by both simulation results and experimental results in the following sections. It will be also shown that DDEM outperforms RDEM in two aspects. One is that DDEM requires much simpler control logic than RDEM for implementation. The other is that ADC test based on DDEM is generally much more accurate than that based on RDEM for a given number of samples.

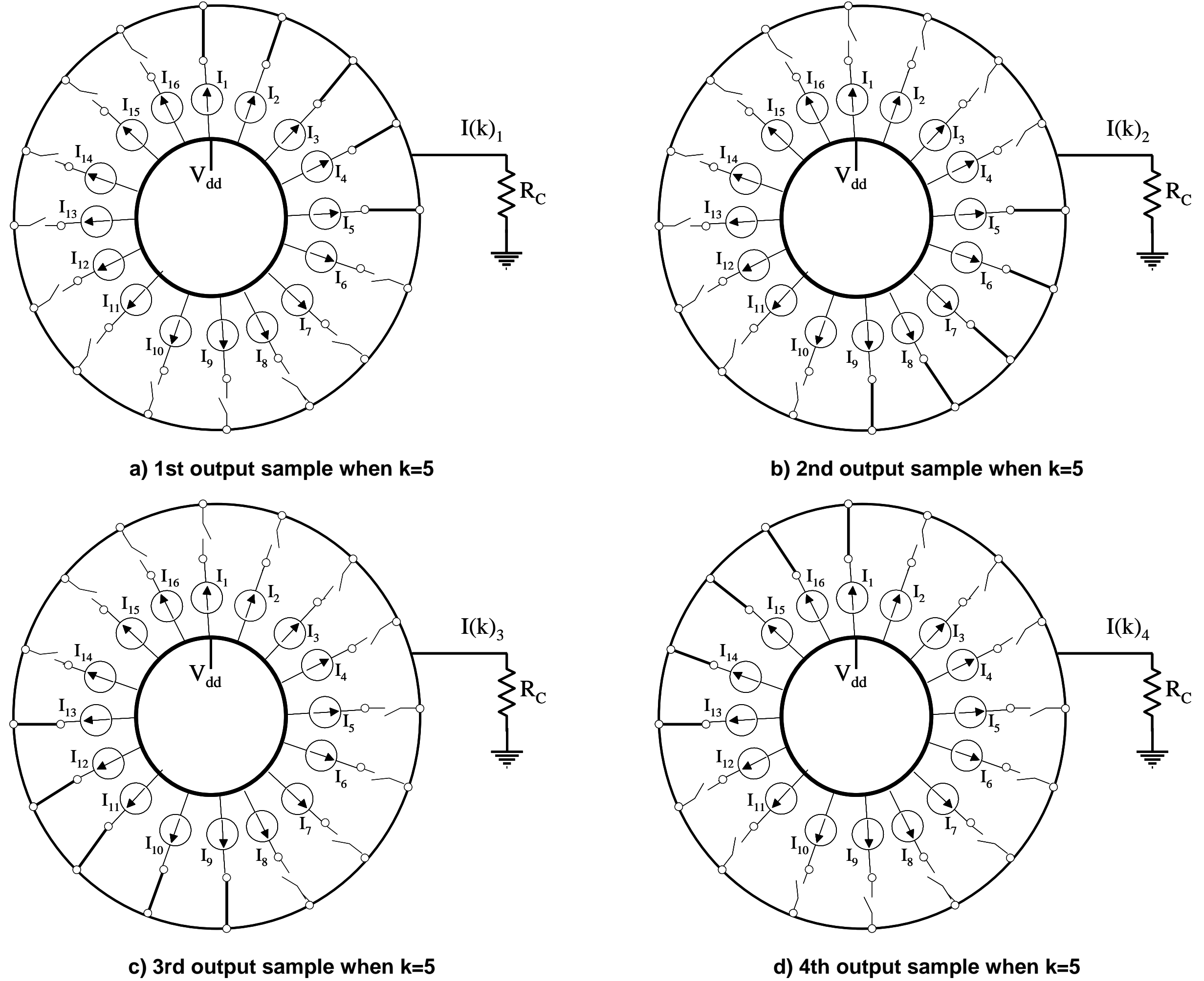
3.1 Cyclic DDEM Switching Sequence

In this subsection, we will describe a Cyclic DDEM Sequence that is very easy to implement but gives excellent performance. The current sources are arranged conceptually and sequentially around a circle, as seen in Figure 2, to visualize a wrapping effect whereby the Nth current source is adjacent to the first current source. In the example shown in Figure 2, k = 5, n = 4, N = 16, p = 4, and q = 4. The physical layout of the current sources need not have any geometric association with this cyclic visualization.

We will denote p current sources as index current sources by the sequence I_1, I_{1+q}, I_{1+2q},..$I_{1+(p-1)q}$. These index current sources are uniformly spaced around the circle. For each input code k, $1 \le k \le N$, the DAC generates p output voltages. Each output voltage is obtained by switching on k current sources consecutively starting with one of the p index current sources. Thus, the dth sample ($1 \le d \le p$) is obtained by switching on k current sources consecutively starting with $I_{1+(d-1)q}$ and continuing around the circle in the clock-wise direction.

We will term this the Cyclic DDEM Switching Sequence. It may appear to be similar to some of the DDFN approaches that are in use but, in contrast to the DDFN approaches, the Cyclic DDEM Switching Sequence is not data dependent and is completely deterministic.

At this point, a comparison between the Cyclic DDEM Switching Sequence and the random DEM switching sequence can be made from a hardware implementation viewpoint. It can be shown that the logic needed to implement the Cyclic DDEM approach is much simpler than that needed for a completely random DEM switching sequence. No scrambler is needed in the Cyclic DDEM approach and since the index current source values are shifted by a fixed amount, a shift register can be used to drive the switches that select the current sources.



a) 1st output sample when k=5

b) 2nd output sample when k=5

c) 3rd output sample when k=5

d) 4th output sample when k=5

Figure 2 Cyclic DDEM Switching of a 4-bit DAC

3.2 Performance evaluation of the deterministic DEM switched DAC

For each input code k, the DAC outputs p samples. Each output is the summation of the selected k current elements (scaled by Rc). The dth current summation is given by

$$I_d(k)=\sum_{j=1}^{k} I_{(d-1)q+j} \qquad d=1,...,p \tag{4}$$

The average of the p samples for code k is given by $\bar{I}(k)=\frac{1}{p}\sum_{d=1}^{p} I_d(k)=\frac{1}{p}\sum_{d=1}^{p}\sum_{j=1}^{k} I_{(d-1)q+j}$ (5)

The statistical performance of the DAC output will be evaluated based on $I_d(k)$ and $\bar{I}(k)$. Suppose the expected value of all current elements in this die is I_0 (which is unknown and may be different from batch to batch, wafer to wafer, or die to die). Due to random variations, the actual value of each current source is given by:

$$I_j = I_0(1+\varepsilon_j) \quad (j=1,...,N) \tag{6}$$

We assume the variations follow a Gaussian distribution and ε_j *i.i.d.* $\sim N(0,\sigma^2)$ where σ^2 is determined by design and process variations. The overall output range is determined by $I(N)=N\cdot I_0 + I_0\sum_{j=1}^{N}\varepsilon_j$. Due to uncertainties in I(N), the actual output range may not reach the desired level. To make sure that DAC output range covers the DUT input range, we must guarantee the DAC nominal output range to be larger than the ADC input range.

We will first inspect the average of the p output samples for each DAC input code k. To evaluate the linearity of the averaged output, we define an end-point fit line which connects (0, I(0)) and (N,I(N)). For any k, write k=t*q+s (s=1,…,q, t=0,…,p-1). It can be shown that the expected values of all the averaged output current $\bar{I}(k)$'s are on the

fit line exactly, and the standard deviation of $\bar{I}(k)$ is given by

$$\sqrt{\frac{q(q-s)}{4pq}}\sigma \cdot I_0 \quad (7)$$

As an example, if n = 16, p = 64 and σ = 0.1, the maximum normalized standard deviation of the $\bar{I}(k)$'s is only 0.2, which shows that every averaged output always stays very close to the fit-line and hence all the $\bar{I}(k)$'s are almost uniformly distributed.

Since all the p output samples for code k are the summation of k elements from the same Gaussian distribution, they also have Gaussian distribution with center at $\bar{I}(k)$. The distribution is described as following:

$$N\left(\bar{I}(k), \frac{(N-k)k}{N}\sigma^2 \cdot I_0^2\right) \quad (8)$$

With proper approximation, when p is large, all the output samples of the DDEM DAC obey a distribution with the following PDF.

$$f(x) = \sum_{k=1}^{N} f(x \mid k) \cdot P(k) \quad (9)$$

Here, f(x|k) is the PDF corresponding to (8) and P(k) is the probability of each input code k. P(k)=1/N. For a DAC with given number of bits n, p and σ are the two key parameters to determine the distribution in equation (9). Though equation (9) is too complicated to simplify analytically, we can draw the overall PDF as a combination of Gaussian PDF's with the aid of MATLAB. Figure 3 depicts the output PDF of a 10-bit DDEM DAC. For this example, σ is chosen to be 0.1 and p is set to 64. From this figure, the output PDF is very flat except near the end points. Actually, near the end points, due to the small variances which can be calculated from (8), the PDF is discontinuous and fluctuates. The histogram of a given DAC is a realization of such PDF, and must also be uniform except near the end points. Therefore when using the cyclic DDEM DAC for ADC testing, the DAC output range should be scaled so that the two ends fall outside the ADC input range.

The flatness of the PDF comes from two essential facts. First, the center (averaged value $\bar{I}(k)$) of a cluster of p samples corresponding to each code k is almost uniformly distributed. Secondly, the individual samples within each cluster are spread out suitably (σ not too large and not too small). The combined distribution of all these clusters becomes nearly continuous and flat. These two facts are controlled by two key parameters of the DDEM DAC, one is the DDEM iteration number p and the other is the DAC element mismatch variance σ. Generally speaking, larger p helps to achieve a more uniform histogram. On the other hand, in order to ensure proper spread among each cluster of p samples, extreme values of σ should be avoided. A fairly large range of σ values satisfy this requirement, including typical mismatches of near minimum sized current cells. [27] Because of this, an ideal DAC (or a very well designed DAC) is actually not a good candidate for using DDEM. Near-minimum sized DACs, whose elements suffer from significant variations, can actually lead to better performance after DDEM is applied.

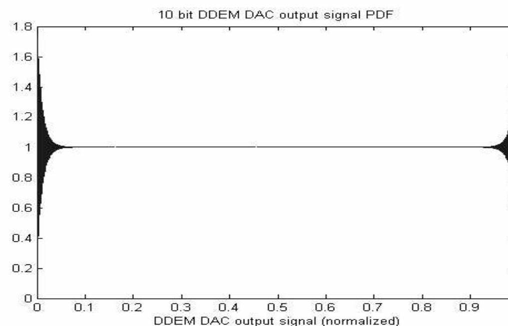


Figure 3 Output PDF of 10 bit DDEM DAC

It is obvious that DAC number of bits (NOB) is also one of the major factors that determine the ADC test performance when using DDEM DACs. Analysis shows that if a non-ideal DAC has an ENOB (effective number of bits) of n_E bits, then the DDEM DAC can achieve ADC testing performance that is comparable to the ADC testing performance of an "ideal" DAC with $n_E+\log_2 p$ bits of resolution. Hence, to correctly test n bit ADCs, it is recommended to have $n_E+\log_2 p >= n+2$.

4. Simulated ADC testing with DDEM DACs

To verify the DDEM approach, we simulated testing of flash ADCs with resistor mismatching by using a DDEM DAC with lower resolution/accuracy than the ADCs. In simulation, the DDEM technique is applied to a simulated current steering thermometer-coded DAC with static mismatching error in the current sources.

Most existing ADC testing approaches utilize DACs that have higher resolution than the DUT. This is generally considered necessary to avoid the introduction of significant quantization errors. Since the statistical linearity of the DDEM DAC can far exceeds its resolution, the question of whether the DDEM DAC resolution can be reduced to levels comparable to or possibly even less than the resolution of the DUT deserves attention. We will not provide a detailed investigation of this issue in this paper but will consider the specific situation where the resolution of the DDEM DAC is less than that of the DUT. Specifically, an 8-bit resolution DAC with 3 LSB INL was used to test 1000 12-bit and 11-bit ADCs with p=256 ($n_E+\log_2 p \approx 13.5$). The DAC has current sources mismatch modeled by a Gaussian distribution with σ = 0.3 and truncated at the 50%

variation level. The Flash ADC resistor strings are generated in a similar manner with σ = 0.15.

The simulation results are depicted in Figure 4 and Figure 5. The INL_k plot of the original 8 bit DAC without DDEM is shown in Figure 4. In Figure 5 (a) and (b), the INL_k testing errors using the DDEM DAC with different p for an 11-bit ADC and for a 12-bit ADC are depicted respectively. For the 11-bit ADCs, the maximum INL_k error was 0.65 LSB with p=256 (32 samples per ADC code), while for the 12-bits ADCs the maximum INL_k error was 1.52 LSB with p=256 (16 sample per ADC code). It should be pointed out that if an ideal 8-bit DAC is used to test the 12-bit ADCs, the average maximum INL_k error is equal to 16.5 LSB.

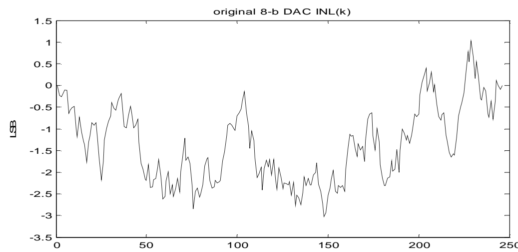
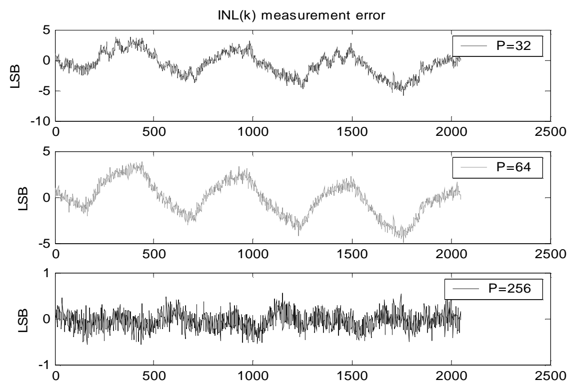
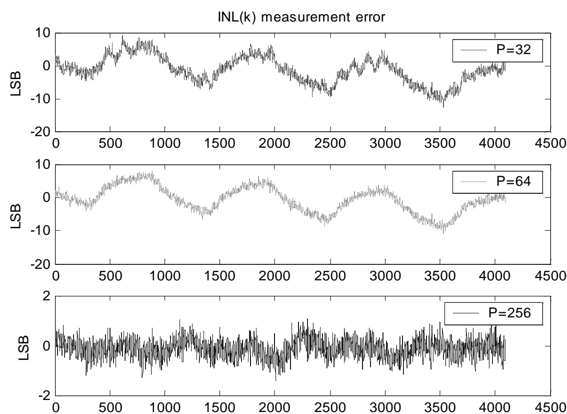


Figure 4 INL_k of the Original DAC (Simulated)



(a) INL_k test error for 11-bit ADC



(b) INL_k test error for 12-bit ADC

Figure 5 INL_k Test Error with Varying p (Simulated)

From these results we can go even further by increasing the DAC resolution to test high resolution ADCs. Figure 6 shows the simulation results obtained when a 12-bit DAC is used to test 100 16-bit ADCs with p = 256 (only 16 samples per ADC code). The DAC INL without using DDEM is 4.4 LSB, so the DAC linearity is a little less than 9 bits. Hence $n_E+\log_2 p < 17$. The figure depicts the estimated ADC INL's versus their true INL's. The estimation errors (estimated INL – true INL) range from -0.002 LSB to 0.348 LSB. Hence, the testing performance in terms of total INL measurement is much better than in terms of maximum INL_k error. Furthermore, since the INL errors are almost always slightly to the conservative side, this helps avoid sending bad parts to the customer.

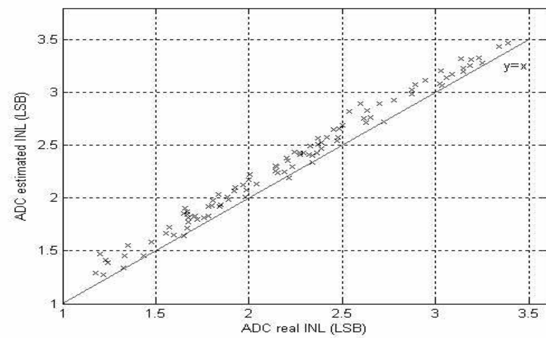


Figure 6 ADCs Real INL vs ADCs Estimated INL

It was mentioned in the previous section that deterministic DEM outperforms random DEM in implementation simplicity. A direct comparison of RDEM and DDEM for testing ADCs was also made in simulation. In Figure 7 we compare the performance of estimating the INL's of 100 11-bit ADCs using RDEM and DDEM respectively with p=128. In the comparison, the same 10-bit DAC with an INL of about 10 LSB was used. From Figure 7, one important observation can be made that the DDEM method offers substantial improvements in testing performance over the random DEM approach for a given number of samples.

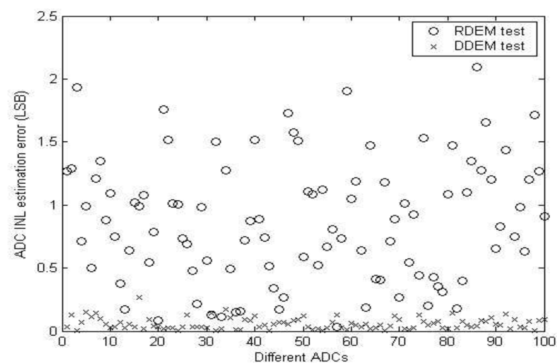


Figure 7 Comparison of RDEM and DDEM for Estimating 100 ADCs' INL with p= 128

5. DDEM DAC design and experimental results

To validate the DDEM approach further, an 8-bit DDEM DAC was designed and tested. In this section, we will first discuss the DDEM DAC design and then provide the measurement results.

5.1 DDEM DAC design

In implementing the DDEM DAC, two critical parts of the design are the current source elements and the DDEM control logic circuit. Other design issues such as gradient effect and output nonlinearity should also be considered. Benefited from the DDEM approach, the design is a quick and simple design, and the DAC occupies very small die area.

a) Current source element

There are quite a few current steering DAC structures. Since with the DDEM approach, the element matching issue is not critical, we can use a simple structure which uses fewer devices and hence less die area. Also DDEM makes it possible to use small-sized devices. By using a simple structure with small-sized devices, the DAC speed can be very high since it has small parasitics and therefore small capacitance load.

The current element structure used is the simple single-supply positive-output structure with three PMOS transistors [29] as depicted in Figure 8. To balance the output, both M1 and M2 have their drains connected to an output resistor respectively. We have Vu>Vb>Vd, and one shifter register unit (SR) to control M2's gate. If M2's gate is connected to Vu, the current in this current unit flows through M1 and Rp to the ground, and if M2's gate is connected to Vd, the current flows through M2 and Rn to the ground. For the single ended output mode, the voltage crossing either Rp or Rn serves as the output voltage. And for the differential output mode, the voltage difference between Rp and Rn serves as the output.

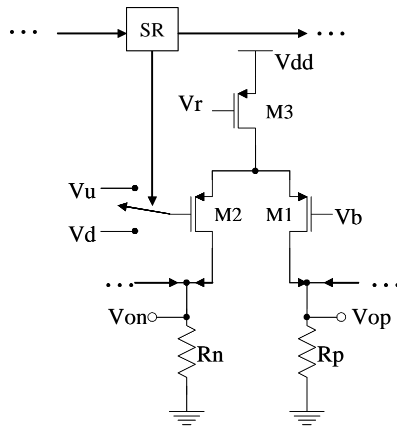


Figure 8 Current Steering Element Structure

To maximize the speed, the reference voltages should be chosen properly such that during switching none of the transistors will go into the deep triode region.

b) DDEM control logic

We described the Cyclic DDEM Switching Sequence for code k in Section 3.1. For each input code k, the DDEM DAC outputs p samples. For all the output samples corresponding to all the N input codes, it is equivalent to make the DDEM DAC output p N-step ramps with the p index current sources as the first element respectively. We built the control logic to generate these p ramps.

The control logic circuit is just a 256-bit shift register ring with each unit controlling one current source element. Starting from the all-zero state, one of the register units is selected as the index point and a logic '1' is continuously pumped into this unit. Then each time the clock signal advances, one more register unit is set to '1'. Thus the DAC output a monotonic ramp voltage by cluster current on Rp. In the meantime, the voltage crossing Rn is a declining signal. When all register units are set to "1", one RESET signal clears all the units, a different index point is chosen and the same operation is applied. To achieve high speed with small die area, the simple shift register was adopted as shown in Figure 9. It contains only 6 transistors with 2 CMOS inverter and 2 NMOS transistor switches in series. Two-phase non-overlapping clock signals are required to drive this shift register. [30]

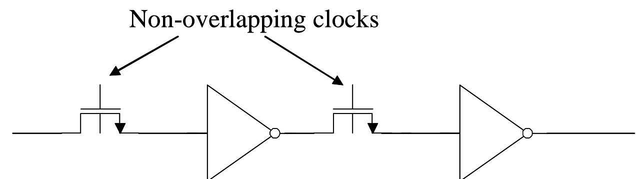


Figure 9 6-Transistor Shift Register Unit

c) Deterministic error minimization and compensation

The random mismatching error between current elements can be averaged out by DDEM. However, both theoretical analysis and simulation results show that two types of systematic errors cannot be totally averaged out by DDEM. One is the output node nonlinearity error, and the other is the periodical error in the DAC elements. The sources for the first type of error may be the nonlinearity from the MOS transistors or the load resistance nonlinearity. The periodic error may be from the layout gradient effect. We should reduce these two types of errors during the design. For example, we used the cascoded current source structure to alleviate the output node nonlinearity. To reduce the error from the layout gradient, proper layout strategy should be adopted.

Though the systematic errors cannot be averaged out by DDEM, fortunately, these errors are highly predictable.

With a set of chips from the same fabrication run, we may test a few of them first and predict the systematic errors for all the chips from that run (DDEM will take care of the remaining random errors). We can then compensate for the systematic errors during the ADC test.

5.2 Measurement results

The 8-bit DDEM DAC was fabricated in a 0.50µm standard CMOS process. The core die size is about 0.9mm×0.9mm for double 8-bit DACs (0.4 mm^2 for each single DAC). The die photo is shown in Figure 10. The power supply voltages are 5V for both digital and analog parts. As driving the 22 ohm resistance loads, the power consumption is 260mW for the analog part and 60mW for the digital part with 0~1V output range at single ended output node (-1~+1V for differential mode). The power dissipation can be dramatically reduced by using larger resistors as the loads.

To test the DDEM DAC performance, DDEM control signals generated by a pattern generator were applied to the DAC and the DAC output (single ended mode) is sampled using a data acquisition board with high resolution ADCs. Though the DAC can operate at a speed of 10Msample/sec, the DAC was tested with a clock speed of 1 kHz due to the speed limitation by the data acquisition board. The DAC output with different iteration parameter p was collected and stored in computer for performance evaluation.

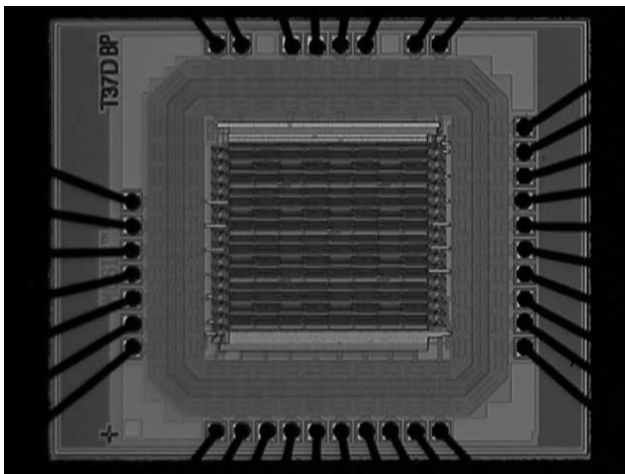


Figure 10: Photo of the DDEM DAC die

Figure 11 shows that without DDEM, the original 8-bit DAC has an INL error of 10.3 LSB, which means the original DAC has a linearity of less than 4 bits. The main error source for this DAC is the systematic nonlinearity. We can estimate the nonlinear error by measuring one or several samples from the fabricated chips. We can then apply the same nonlinear error compensation to all the chips from the same run, which brings the DAC linearity to about 5 bits linear without DDEM.

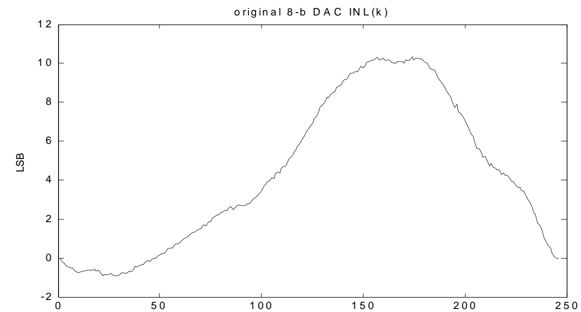
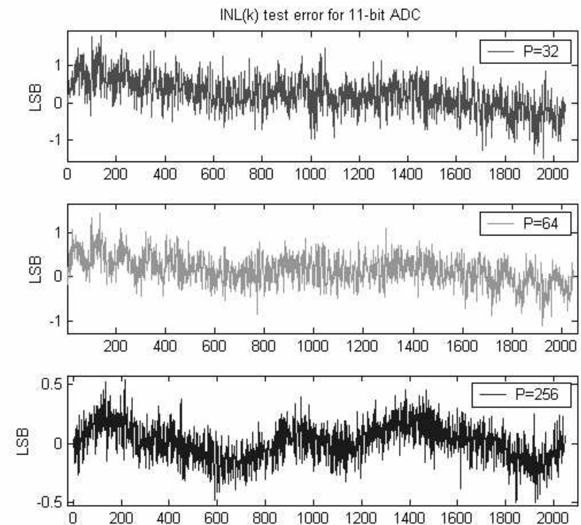


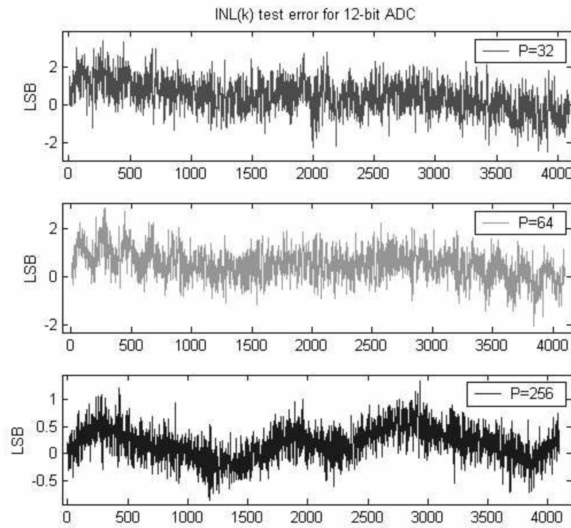
Figure 11: INL_k of the Original 8-bit DAC (Experimental)

The measured and stored DAC output was used as the stimulus to simulated ADCs and the ADCs' INL_k are estimated from the ADC output histogram. The simulated ADC's true INL_k are known by calculation. We calculated the difference between the estimated INL_k and the true INL_k. The difference is just the test error with DDEM DAC output as the stimulus to ADC under test.

To compensate for the systematic errors, we first estimate the systematic error by testing one randomly selected DAC. Based on the estimated nonlinear error, we obtained the compensation values for testing ADC. Then the compensation values were applied to other DACs. Experimental results show that the compensation values work for all the other tested DDEM DACs.



(a) INL_k test error for 11-bit ADC



(b) INL_k test error for 12-bit ADC

Figure 12: INL_k Test Error With Varying p (Experimental)

Figure 12 (a) and (b) show the test errors after nonlinear error compensation for an 11-bit ADC and a 12-bit ADC using a DDEM DAC with p=32, 64 and 256 respectively. The simulated ADCs' INL ranges from 5 LSB to 10 LSB. From Figure 12 we can see that 1) the test error decreases dramatically when p increases; 2) when p = 256 (full DDEM), the 8-bit DAC can test the 11-bit and 12-bit ADCs with error bounded by about ±0.5 LSB and ±1 LSB respectively using DDEM. (For the 12-bit ADC, the output histogram has around 16 hits for each bin.). Note such test performance is only achievable by using a DAC at least 13~14-bit linear if DDEM is not used, while in this case the original DAC's linearity is less than 5 bits without DDEM. It should be also noted that if the systematic nonlinearity is addressed then the error caused by current sources mismatches is eliminated by the DDEM, allowing us to use minimum sized devices.

6. Conclusions

In this paper we presented a DDEM approach which is applied to low resolution/accuracy DACs for testing high resolution ADCs, characterized its performance mathematically, and validated it through simulation and experimental results. It was shown that with this approach DACs' linearity can be significantly improved statistically, and therefore DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADCs. Since the DDEM is not used in the real-time signal path, limitations related to using DEM for real-time signal processing are avoided. Comparison against random DEM testing strategy demonstrates that DDEM performs substantially better than the standard RDEM from a testing viewpoint. An 8-bit current steering DAC with DDEM control was designed, fabricated, and tested to verify the DDEM approach. The measured and stored DDEM DAC output is used as stimulus to simulated ADCs under test. Results show that the testing error decreases when p increases. When p=256, the 8-bit DDEM DAC with original linearity less than 5 bits was able to test 12-bit ADCs with test error bounded by ±1LSB. The DDEM DAC technique offers potential for use in both BIST and production test environments, since the linearity of the testing signal generator, and therefore the area required, are relaxed.

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