A Segmented Thermometer Coded DAC with Deterministic Dynamic Element Matching for High Resolution ADC Test

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***ABSTRACT*—Dynamic element matching (DEM) is an effective way to achieve good average performance in the presence of device mismatch, yet it has not been widely adopted because of the time-local stationarity of the signal path. This paper presents a DEM approach to ADC testing in which low precision DEM DACs are used to generate stimulus signals for the ADCs under test. A deterministic DEM (DDEM) switching scheme is applied to a segmented thermometer coded DAC architecture. Detailed simulation results are presented to verify the expected performance of the proposed testing approach. The new approach is able to accurately test ADCs with linearity that exceeds that of the original DAC used as the signal generator. The new architecture is suitable for production test and built-in-self-test (BIST) environments where high linearity ADCs are difficult to test and characterize.**

I. INTRODUCTION

Due to increasing resolution and conversion rates, the challenge of testing analog to digital converters (ADCs) is growing [1]. Testing techniques that facilitate a reduction in the test cost would have a significant impact.

Built-in-self-test (BIST) structures offer the potential to reduce cost while also adding value to the circuits under test. BIST schemes can be used for self-calibration and hence improve circuit performance. Most existing approaches have been aimed at duplicating a standard tester on chip [2], in other words, to produce a highly accurate and linear stimulus on the chip. However, the prior arts have not demonstrated linearity adequate for testing high resolution ADCs on-chip.

A new approach relaxes the linearity requirements on the signal generator and uses signal processing techniques to accurately characterize the device under test (DUT). The mathematics behind linearity testing of ADCs using non-linear signals was presented in [3], where a nonlinear stationary excitation and its shifted replica are needed. In [4] a more rigorous analysis of the methods actually used and the new approach was done by the authors with simulation and experimental results included.

In this paper dynamic element matching (DEM) is applied to low linearity DACs so that they can be used to test high-resolution ADCs.

Due to process variation, element mismatching errors are inevitable. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases. The DEM technique accepts mismatching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average the output values are linear. The DEM method was used by various researchers [5-9] to improve the effective specifications of linearity performance of DACs. Most researchers use DEM in Delta-Sigma Converters.

Our application of DEM allows the signal generator for ADC testing to be realized with a low-linearity DAC, eliminating the need of large silicon area and careful design of the test signal generator. A preliminary study investigated the use of random DEM with a highly-nonlinear DAC to test low-resolution ADCs [10]. The idea behind DEM testing is to generate more than one DAC output samples as the ADC testing stimulus with a given DAC input digital word; each sample picks different elements following the DEM philosophy. Since DEM is used in the input signal generator we do not have to worry about DEM in the signal path. Deterministic DEM was introduced and compared with the random DEM (RDEM) testing in [11] using a thermometer coded current steering DAC. It was shown that the DDEM significantly outperformed RDEM. As an added benefit, the circuit complexity is reduced because no randomizer is required. However, when high resolution DACs need to be implemented, due to the large number of current sources and high complexity of switching logic, building them using the thermometer coded architecture is impractical. The design is not trivial and a large area is required. A simpler DAC architecture that maintains the benefits of the DAC used in [11] needs to be developed. The segmented thermometer coded architecture was chosen. Each segmented array (MSB and LSB) will use DDEM, as explained later in this work.

This paper is organized as follows. An explanation of how ADC INL is calculated is given in Section II. Details are presented in Section III about the DDEM segmented thermometer coded (STC) DAC architecture while in Section IV simulation results for high resolution ADC testing are shown and discussed. Section V concludes this work.

II. INL CALCULATION

There are several alternative but similar definitions of the INL of an ADC. In some cases, the INL is defined as a continuous function of the ADC input voltage, whereas in other cases, the INL is only defined at the ADC's transition points T_k, thus resulting in a discrete function INL[k], or denoted as INL_k. In this paper, we follow what is most commonly used by industry test engineers and use the transition point INL_k to characterize the ADC's linearity performance. To define the INL_k of the ADC, we first need the transition points of an ideal linear ADC which are usually defined as the endpoint fit line transition points $\underline{T_k}$:

$$\underline{T_k} = T_0 + \frac{T_{N-2} - T_0}{N-2} k, \qquad k = 0,1 \ldots N-2 \tag{1}$$

Equation 1 represents a straight line connecting the first and last transition points of the ADC, as seen in Figure 1. Actual transition points of an ADC are compared to their corresponding endpoint fit line transition points for linearity characterization. The difference between the actual transition points and the fit-line transition points is defined as INL_k and is expressed in LSBs. INL_k is defined mathematically by:

$$INL_k = \frac{T_k - \overline{T_k}}{1LSB} = \frac{T_k - T_0}{T_{N-2} - T_0}(N-2) - k \qquad (2)$$
$$k = 1,2...N-3$$

Notice that by definition the INL_k for the first (k=0) and last (k=N-2) transition points are 0 and they do not appear in (2).

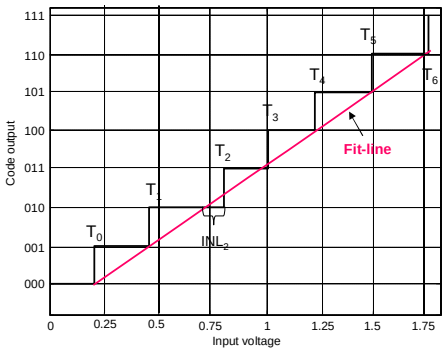


Figure 1. A non-ideal ADC transfer curve and its endpoint fit line

The most commonly used method for ADC INL testing is the standard histogram method and that is also the method that we will use in this paper to test ADC linearity. In the standard use of the histogram method, an ideal linear ramp is presented to the input of the ADC. The ADC takes samples of the input and the converted output codes are tallied into corresponding bins. Since V_{in} is proportional to time and the sampling intervals are constant, the total number of accumulated samples is proportional to V_{in}. Therefore a transition voltage is proportional to the total code hits for all output codes corresponding to lower voltages, and the accumulated histogram counts can be directly used to compute the INL_k of the ADC.

Naturally, in order for this method to work, it is imperative to have a highly linear ramp, with linearity a decade or more better than the resolution of the ADC under test, since any nonlinearity in the input signal will be directly translated into INL_k estimation error in the histogram method. If the ramp is generated using a DAC, it is required that the DAC have resolution and linearity that are at least 3 bits more than the targeted resolution of the DUT. This is a fundamental challenge in both production test and built-in-self-test of high resolution ADCs. The DDEM approach is proposed as a solution to this problem. The DDEM approach is used to provide stimulus generator with adequate statistical linearity for ADC testing while keep the cost at a much lower level.

III. DDEM METHOD FOR SEGMENTED THERMOMETER CODED DACS

In this section we will describe how we apply DDEM to a STC DAC. First we will review the DDEM switching scheme as used in [11] on a thermometer coded (TC) current steering DAC. To perform the DDEM method, we add one more extra current source element to the DAC, so that now the DAC has totally $N = 2^n$ current sources. We use $i_j \quad (j = 1,...,N)$ to represent the j[th] current source element out of the total N elements, and p represents the number of samples to be generated for each DAC input word. p is also termed as the DDEM iteration number. All current sources are arranged conceptually along a circle to visualize the wrapping effect (physical layout of the current sources can be a rectangular array). p starting places that are $q = N/P$ current sources apart are selected. Then, for each input code k, the DAC generates p samples of output where each sample is obtained by switching k current sources consecutively starting from one of the p starting places. The d[th] $(1 \le d \le p)$ sample is obtained by switching k current sources starting from $i_{(d-1)q+1}$ in the clock-wise direction. The output analog signal is obtained by forcing the summation of the selected k current sources to drive a resistor R_F.

For an n bit current steering DAC, we can divide the n bits to two parts: $n = n_M + n_L$, where n_M represents the more significant bits and n_L represents the less significant bits. If we let $N_M = 2^{n_M}$ and $N_L = 2^{n_L}$, we have $N = 2^n = N_M \cdot N_L$. For a DAC input code k, we can break it up as following:

$$k = k_M N_L + k_L \begin{pmatrix} 0 \le k \le N-1, \\ 0 \le k_M \le N_M - 1, \\ 0 \le k_L \le N_L - 1 \end{pmatrix} \qquad (3)$$

To get the analog signal corresponding to k, we can obtain the analog signals corresponding to k_M and k_L with different weights respectively first and then combine them together. To implement this, we can use a MSB current source array to generate k_M and use a LSB current source array to generate k_L. Here the MSB and LSB array have N_M-1 and N_L-1 current source elements respectively, and the weight of each MSB array element is N_L times that of a LSB array element. A 4-bit STC current steering DAC is shown in Figure 2 as an example. In this example, n=4, $n_M = n_L = 2$ and $N_M = N_L = 4$.

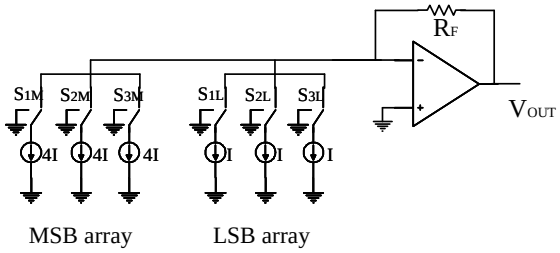
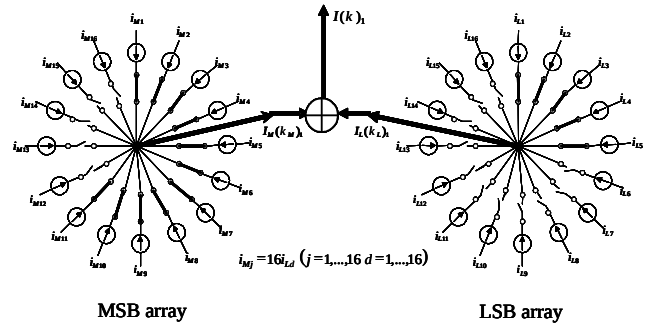


Figure 2. A 4-bit segment coded current steering DAC structure

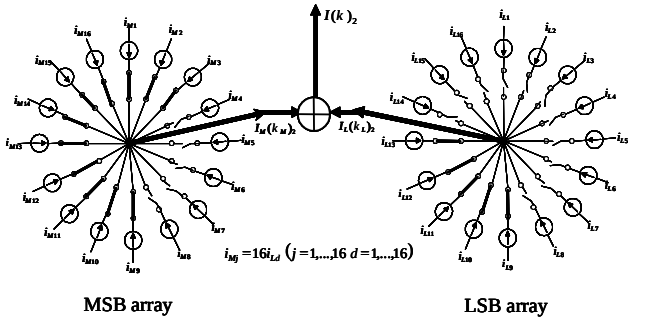
To implement the DDEM for a STC DAC, we only need to apply DDEM to both the MSB array and the LSB array simultaneously. We add one extra current source element for both the MSB and LSB array, then the MSB array has N_M current source elements and the LSB array has N_L currents source elements. We use $i_{M,j} \quad (j = 1,...,N_M)$ to represent the j[th] current source element out of the total N_M elements of the MSB array and $i_{L,j} \quad (j = 1,...,N_L)$ to represent the j[th] current source element out of the total N_L

elements of the LSB array. Each DAC input code k has p output samples. As what we did to a TC DAC, we choose p index elements from each array distanced by $q_M = N_M / p$ and $q_L = N_L / p$ respectively.

Suppose now that the DAC input code is $k = k_M N_L + k_L$ and that each code needs to have p output samples; then, in order to generate each output sample for a code k, the DDEM method picks k_M current sources from the MSB array and k_L current sources from the LSB array by applying DDEM switching scheme to the MSB and LSB array respectively. Figure 3 illustrates the current source switching scheme for an 8-bit STC DAC. In this example we have $n_L=n_M=4$ and $N_L=N_M=16$, and p is selected to be 2. For each input code k, 2 samples are output. In Figure 2, $k=191=11\times N_L+5$, hence $k_M=11$ and $k_L=5$. For the 1st output sample, i_{M1}~i_{M11} are selected from the MSB array and i_{L1}~i_{L5} are selected from the LSB array; for the 2nd output sample, i_{M9}~i_{M16} and i_{M1}~i_{M3} are selected from the MSB array and i_{L9}~i_{L13} are selected from the LSB array.



(a)1st output when D=191



(b) 2nd output when D=191

Figure 3. DDEM switching of a 8-bit STC DAC

The described DDEM STC DAC requires DDEM cyclic switching sequence on both the MSB and LSB arrays. Since the resolution of the two arrays are both quite low, the DDEM control logic complexity can be maintained at a low level.

IV. SIMULATION RESULTS

For the following simulation results, the ADCs have 16 bit resolutions while the STC DACs have 18 bits of resolution with a 9-bit MSB array and a 9-bit LSB array. The simulated ADCs have varying INL errors. The original DACs have an effective number of bit (ENOB) much less than 18 since there are large mismatching errors for the current elements inside the MSB and LSB arrays respectively and also a 1% matching error between the LSB and the MSB arrays was included. To simulate the actual test environment, noise was also added to the DAC output, and this noise could be as big as ± 3 LSB_{DAC}.

Figure 4 shows the INL distribution of the 1000 simulated ADCs. A STC DAC with an original INL equal to 38 LSB is simulated, which means that the actual DAC linearity is less than 12 bits. The DDEM approach is then applied to this DAC and the outputs are sent to the ADCs. In the simulation, p was set to be 128. We estimate the INL for each ADC based on the histogram with these inputs and calculate how much it deviates from the true ADC INL. The results are shown in Figure 5.

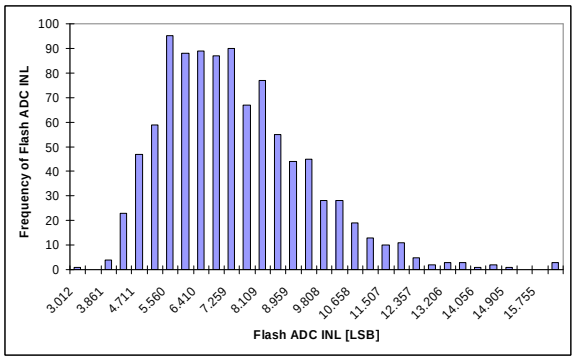


Figure 4. INL distribution for 1000 flash ADCs

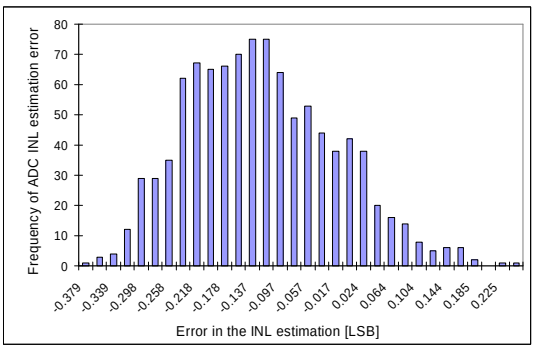


Figure 5. INL estimation error distribution using a DDEM STC DAC

From Figure 5, it can be seen that using the DDEM STC DAC the error in the INL estimation is between -0.39 and 0.2 LSB. The degradation in performance compared to previous work [11] may be attributable to LSB and MSB matching error. The degradation in estimation is only a factor of 2 while the circuit complexity was significantly reduced.

The resultant structure is suitable for BIST applications. In that case each ADC has a particular DAC to test it. To emulating the BIST environment, 1000 DAC-ADC pairs are simulated. The DACs have the same errors as before, while the ADCs used have an INL distribution as shown in Figure 6. As can be seen the ADCs to be tested are actually 16 bit linear since their INL is not bigger than ½ LSB in most of the cases. The DACs used for testing these ADCs have linearities of 12 to 13 bits without DDEM, which is actually 3 bits less than the linearity of the DUT's.

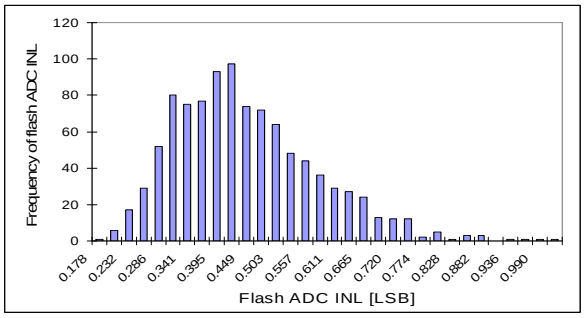


Figure 6. INL distribution for 1000 accurate ADCs

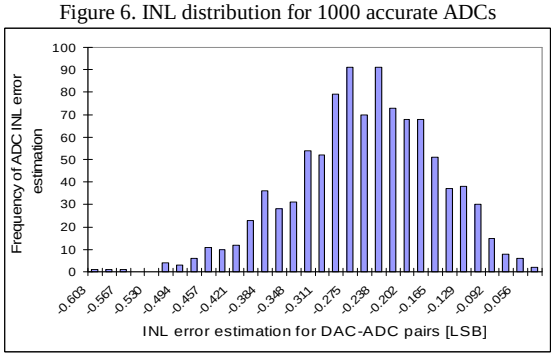


Figure 7. INL error estimation for DDEM STC DAC and ADCs 1000 pairs

Figure 7 shows the simulation results for the 1000 DAC-ADC pairs. We can see that the estimated INL has an error of less than ½ LSB for a majority of the cases. This test verifies that the technique is suitable for BIST applications.

More simulation was done to verify the reliability of the proposed technique as a test tool. In this simulation we tried to find if the ADC INL is underestimated using the DDEM STC DAC. We simulated 1000 ADCs with INL around 0.5 LSB (Figure 6). The DAC used to estimate the ADCs' INLs has an INL equal to 38 LSB and p= 128. Assume that the ADCs need to have less than 0.8 LSB INL in order to comply with their specifications, so the testing boundary to say that a part is a good part is below 0.8 LSB. The parts that have INL between 0.8 and 2 LSB are classified as "not so good" (NSG) parts and can be still marketed as less accurate parts. We can see in Figure 8 that although some good parts are tested as NSG ones, there are no NSG parts classified as good ones, which means that the customer will not receive a deficient part.

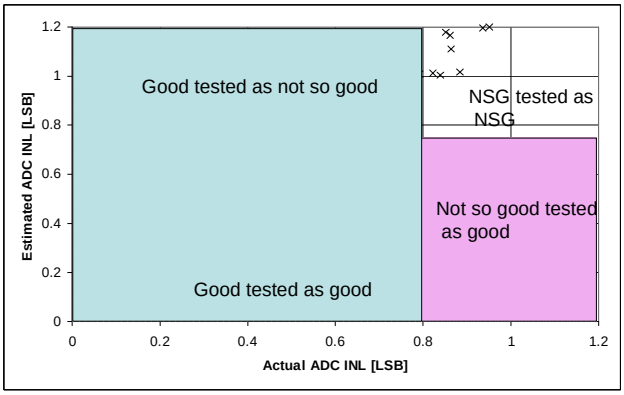


Figure 8. DDEM STC DAC used as a production tester for 1000 accurate flash ADCs

V. SUMMARY

A deterministic dynamic element matching (DDEM) approach was proposed on a segmented thermometer coded (STC) DAC structure for ADC testing purpose in this work. Simulations were used to validate this architecture. Simulation results showed that the approach is reliable to test high resolution ADCs. The architecture is suitable for BIST applications because it requires small area and uses a simple switching scheme to implement. The performance of the new DDEM STC DAC is similar to the DDEM TC DAC presented in previous work and can be successfully employed.

Finally we should point out that high resolution ADCs were successfully characterized using a DAC with original linearity 3 bit worse than that of the DUTs.

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