Dither Incorporated Deterministic Dynamic Element Matching for High Resolution ADC Test Using Extremely Low Resolution DACs

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***Abstract*—A novel Dither Incorporated Deterministic Dynamic Element Matching (DiDDEM) approach is proposed. With this approach, the combined output of a DDEM DAC and a dither DAC serves as the stimulus to an ADC under test. Theoretical analysis shows that the test performance with the DiDDEM DAC is equivalent to that of a DAC with an ENOB (Effective Number Of Bits) equal to the summation of the ENOB's of the DDEM DAC and the dither DAC plus $\log_2 p$, where p is the DDEM iteration number. The test performance using DiDDEM is also validated by simulation results.**

I. Introduction

With the increasing conversion resolution and rate, testing ADC (Analog-to-Digital Convert) is increasingly challenging. Testing high-resolution high-speed ADCs is one of the most important tasks that test engineers need to handle. Also ADC is a critical component of the SOC's (System-On-a-Chip). Built-In-Self-Test (BIST) is the most promising solution to test those deeply embedded ADCs cost effectively. It is significant to develop methods for BIST of embedded ADCs with affordable hardware and computation payload.

It is the common belief that for accurate ADC test highly accurate test signals are required. Usually it is recommended that the stimulus to the DUT should have accuracy 10 times or 3 bits better than ADC's. The consequence of this conventional idea is the ubiquitous use of high-accuracy test equipment. It also follows that test methods developed for the product test environments cannot be used for BIST situations, since it is impractical to duplicate the high-accuracy test equipments on chip using limited die area.

To provide cost effective test approaches for ADC production test and BIST, alternative approaches that override this belief have been proposed. With these approaches the requirements on the test stimulus are relaxed by orders of magnitudes. The DDEM (Deterministic Dynamic Element Matching) approach is one candidate that can be applied on low resolution/accuracy DACs to generate evenly spaced signals for high-resolution ADC test. [2-4]

The DEM technique is widely used in Σ-Δ modulators to improve the dynamic performance. Similar to the DEM technique, dither is also a technique widely used in data converter applications to improve the output performance statistically [1]. In this work, we adopt the dither technique in the test application, as the case of DDEM for test purpose.

In this paper, a new approach will be proposed to provide a highly cost effective stimulus generator for high resolution ADC test based on both the DDEM and dither techniques. It is capable of both production test and BIST. With this new approach, the requirement on stimulus generator will be relaxed further compared to the DDEM approach. The approach will be explained, theoretically proved and finally validated by simulation results.

This paper is organized as follows. An explanation of histogram based ADC test is given in Section II, and a brief review of the DDEM approach is given in Section III. In section IV, the new approach is introduced. The mathematical proof of this approach will be provided in Section V, followed by simulation results in Section VI.

II. Histogram Based ADC Test

In this paper, we focus on the ADC static performance test. The ADC static performance is totally determined by the transition voltages. For an n-bit ADC, we denote T_k as the transition voltage between code k-1 and k. Then code width W_k for code k can be defined as T_{k+1}-T_k. The DNL (Differential Non-Linear error) for code k can be defined as the difference between the actual code width W_k and the average code width W_0. The average code width is also known as the LSB (Least Significant Bit) step. The INL (Integral Non-Linear error) for code k is defined as the difference between the actual transition voltage T_k and the ideal position for T_k. Since the DNL[k] curve can be obtained by differentiating the INL[k] curve, we only discuss the INL test in the following sections.

Histogram based test is usually used to test ADC INL[k] curve. Among various types of histogram based test, the linear ramp based test is the easiest and most commonly adopted. As stated in [4], what is sufficient in linear ramp based test is just a signal with uniform voltage distribution. To achieve a uniform voltage distribution without caring the time-located linearity is drastically easier than to achieve a high-accuracy linear ramp.

With stimulus having ideal uniform voltage spacing, the ADC output code bin height H[k] for each code k will be proportional to the code width W_k. Assume the ADC test range is $[V_{min}, V_{max}]$. The stimulus output range should cover the DAC test range. For an arbitrary voltage V_t, let $h(V_t)$ represent the number of stimulus samples that fall into $[V_{smin}, V_t]$. It is clear that H[k] is determined by $h(T_k)$ and $h(T_{k+1})$. Based on that, we can evaluate the ADC test accuracy using a given stimulus by estimating how linear $h(V_t)$ is with respective to V_t. For the new proposed stimulus generator, we will validate the performance by estimating the nonlinearity of $h(V_t)$.

III. DDEM DAC

Before evaluating of the new approach, the DDEM DAC will be briefly reviewed in this section. The DDEM DAC is proposed for histogram based ADC test [2-4], where the DDEM approach is applied to a thermometer coded current steering DAC to generate the stimulus to the ADC.

An n-bit DDEM DAC has totally 2^n current sources. Let $N = 2^n$. Use i_j $(j = 1,..., N)$ to represent the j[th] current element out of the total N elements. Let p denote the DDEM iteration number. p represents the number of samples to be generated for each DAC input word k. Define $q = N / p$. The following Cyclic DDEM switching scheme is applied to the current elements:

1. All current sources are arranged conceptually along a circle to visualize the wrapping effect, p index elements that are $q = N / p$ distanced are selected.
2. For each input code k, the DAC generates p samples of output. Each sample is obtained by switching k current sources consecutively starting from one of the p index elements. The d[th] $(1 \le d \le p)$ sample is obtained by switching k current sources starting from $i_{(d-1)q+1}$ in the clock-wise direction.
3. The output analog signal is obtained by forcing the selected k current elements to drive a resistor R_C.

According to theoretical analysis, if a DAC has an effective number of bits (ENOB) of n_{ENOB}, then with the DDEM approach, the DAC can achieve test performance comparable to an ideal DAC with $n_{ENOB}+\log_2 p$ bits resolution. The DDEM approach uses a low resolution/lineaerity DAC to test high resolution ADCs. The DAC element mismatch is highly tolerated, and hence minimum sized current elements can be used. The control logic to implement this approach is simple and easy. The total die size and design effort to implement a DDEM DAC will thereby be greatly reduced. The DDEM approach is capable of both production test and BIST test. The DDEM approach greatly relaxes the stimulus requirement for ADC test. In this work, a new approach based on DDEM will be proposed. With this new approach, the stimulus requirement can be further reduced.

IV. DITHER INCORPORATED DDEM

Here, a new approach for ADC test is proposed which incorporates the DDEM technique with dither. One low-resolution DDEM DAC and one low-resolution dither DAC are combined to provide the stimulus to the ADC under test. We term the new approach as the Dither Incorporated DDEM (DiDDEM).

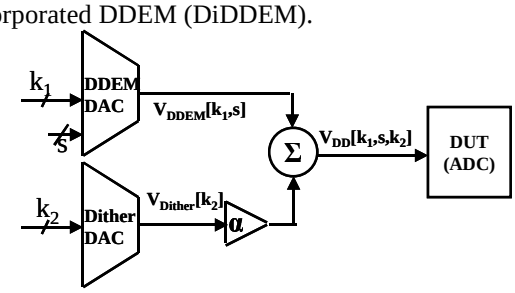

Figure 1. DiDDEM DAC for ADC test

Assume we have one DDEM DAC with n_1-bit resolution and one dither DAC with n_2-bit resolution. The DDEM iteration number is p. As we know that the DDEM DAC has two control words, one is the input code (denoted as k_1), and the other is the DDEM iteration code (denoted as d). We denote the output from the DDEM DAC as $V_1[k_1,d]$ $(1 \le k_1 \le N_1$ & $1 \le d \le p$, $N_1 = 2^{n1})$. Denote the dither input code as k_2, and the output from the dither DAC as $V_2[k_2]$ $(1 \le k_2 \le N_2$, $N_2 = 2^{n2})$. The dither DAC's output is attenuated by a factor α and then added to the DDEM DAC's output. If the maximum outputs of the two DACs are V_{1m} and V_{2m} respectively, nominally α is given by

$$\alpha = \frac{1}{p}\frac{V_{1m}}{V_{2m}} \qquad (1)$$

The summation output serves as the stimulus to the ADC under test. It is clear that the final DAC output has 3 control words: k_1,d and k_2. We denote the combined output as $V[k_1,d,k_2]$. Without repeating the control words, the DiDDEM DAC can have $N_1 * p * N_2$ output samples.

V. TEST PERFORMANCE EVALUATION

We use the output of the DiDDEM DAC as the stimulus to the ADC. The test performance will determined by the distribution of $V[k_1,d,k_2]$ $(1 \le k_1 \le N_1, 1 \le d \le p \& 1 \le k_2 \le N_2)$. In the following part of this section, the test error will be evaluated by estimating $e(V_t)$ defined in (1) for any voltage V_t in $[V_{min}, V_{max}]$.

A. Voltage Distribution of DDEM DAC

The DDEM DAC has N_1 current elements: $i_j (1 \le j \le N_1)$

Let $i_{N+j} = i_j$ $(j = 1,.., N_1)$, then virtually we have $2N_1$ current elements $i_1, i_2, ..., i_{N_1}, i_{N_1+1}, ..., i_{2N_1}$

Let $V_1[0] = 0$ and $V_1[k_1] = R_C \cdot \sum_{j=1}^{k_1} i_j \, (k_1 = 1,..., 2N_1)$, where R_C is the output resistance of the DDEM DAC. Note that the

first half of the sequence is the output voltage sequence of a regular n_1-bit DAC. Let $V_{1m} = V_1[N_1]$. V_{1m} is the maximum output of the DDEM DAC. Define

$$LSB_1 = V_{1m} / N_1$$

Now define *INL* and *DNL* for the DDEM DAC. Let

$$INL_1[k_1] = \left(V_1[k_1] - k_1 \cdot LSB_1\right) / LSB_1 \, (k_1 = 0,...,2N_1)$$

and $DNL_1[k_1] = \left(V_1[k_1] - V_1[k_1 - 1] - LSB_1\right) / LSB_1 \, (k_1 = 1,...,2N_1)$

With DDEM cyclic switching sequence, the DAC outputs *p* ramps. Let q=N/p. The d^{th} ($1 \le d \le p$) ramp is given by $R_C \cdot \sum_{j=1+q(d-1)}^{k+q(d-1)} i_j \quad (k = 1,..., N_1)$, which is equivalent to

$$\left\{V_1^{(d)}[k_1]\right\} = \left\{V_1[k_1 + q(d-1)] - V_1[q(d-1)] : 1 \le k_1 \le N_1\right\}$$

For any V_t less than V_{1m} , let $g^{(d)}(V_t)$ denote the number of elements in $\left\{V_1^{(d)}[k_1]\right\}$ that are not larger than V_t .

$$g^{(d)}(V_t) = \left|\left\{V_1^{(d)}[k_1] : V_1^{(d)}[k_1] \le V_t, 1 \le k_1 \le N_1\right\}\right|.$$

Let $g^{(0)}(V_t) = floor\left(N_1 \cdot V_t / V_{1m}\right)$

We have the follow approximation for $g^{(d)}(V_t)$

$$g^{(d)}(V_t) \approx g^{(0)}(V_t) + \frac{V_t - V_1^{(d)}\left[g^{(0)}(V_t)\right]}{LSB_1} \quad (1 \le d \le p)$$

$$\approx \frac{V_t}{LSB_1} - \sum_{k_1=1}^{g^{(0)}(V_t)} DNL_1[k_1 + q(d-1)] \quad (1 \le d \le p)$$

It is clear that the number of DDEM DAC output samples that are less than V_t is given by

$$g(V_t) = \sum_{d=1}^{p} g^{(d)}(V_t) \approx p\frac{V_t}{LSB_1} - \sum_{d=1}^{p}\sum_{k_1=1}^{g^{(0)}(V_t)} DNL_1[k_1 + q(d-1)]$$

If $g^{(0)}(V_t) = q \cdot t + m \; (0 < m \le q, 0 \le t < p, t \,\&\, m \in Z)$, finally we have

$$g(V_t) \approx p\frac{V_t}{LSB_1} - \sum_{d=1}^{p}\sum_{k_1=1}^{m} DNL_1[k_1 + q(d-1)] \qquad (2)$$

B. Test error with dither incorporated DDEM DAC

Now look at the output of the dither incorporated DDEM DAC. We denote the n_2-bit dither DAC output sequence as $\{V_2[k_2] : 1 \le k_2 \le N_2\}$. Let $V_{2m} = V_2[N_2]$ .We can also define INL[k] and DNL[k] for the dither DAC.

The DiDDEM DAC output is expressed as

$$V[k_1, d, k_2] = V_1[k_1, d] + \alpha V_2[k_2]$$

The maximum output of the combined DAC is

$$V_m = V_{1m} + \alpha V_{2m}$$

For any V_t less than V_m , let $h(V_t)$ denote the number of output samples that are not larger than V_t .

$$h(V_t) = \left|\left\{V[k_1, d, k_2] : V[k_1, d, k_2] \le V_t\right\}\right|$$

By definition, $h(V_t) = \sum_{k_2=1}^{N_2} g\left(V_t - \alpha V_2[k_2]\right)$

Substitute (2) into it, we have

$$h(V_t) = \sum_{k_2=1}^{N_2}\left\{p\frac{V_t - \alpha V_2[k_2]}{LSB_1} - \sum_{d=1}^{p}\sum_{k_1=1}^{m_{k_2}} DNL_1[k_1 + q(d-1)]\right\} \qquad (3)$$

$$= N_2 p\frac{V_t}{LSB_1} - p\alpha\sum_{k_2=1}^{N_2}\frac{\alpha V_2[k_2]}{LSB_1} - \sum_{k_2=1}^{N_2}\sum_{d=1}^{p}\sum_{k_1=1}^{m_{k_2}} DNL_1[k_1 + q(d-1)]$$

where m_{k_2} is given by $g^{(0)}\left(V_t - \alpha V_2[k_2]\right) = q \cdot t_{k_2} + m_{k_2}$.

There are 3 items in (3). The first item is the linear part and the second is a fixed value for any V_t. The third item contains the nonlinearity with respective to V_t. Let $h_e(V_t)$ denote this nonlinearity and change the summation order

$$h_e(V_t) = -\sum_{d=1}^{p}\sum_{k_2=1}^{N_2}\sum_{k_1=1}^{m_{k_2}} DNL_1[k_1 + q(d-1)] \qquad (4)$$

Let $h_{ed}(V_t) = \sum_{k_2=1}^{N_2}\sum_{k_1=1}^{m_{k_2}} DNL_1[k_1 + q(d-1)]$ (5)

If the dither DAC is ideal, then m_{k_2} will be values taken from 1 to q when k_2 varies. Each number from 1 to q will be taken by $r_0 = \frac{N_2}{q}$ times. Then

$$h_{ed}(V_t) = \sum_{m=1}^{q}\left(r_0\sum_{k_1=1}^{m} DNL_1[k_1 + q(d-1)]\right) \qquad (6.a)$$

With the non-ideal dither DAC, the r_0 in (6.a) should be replaced by $r_0 + r_e[m]$, where

$$r_e[m] \approx \sum_{k_2=(m-1)N_2/q+1}^{mN_2/q} DNL_2[k_2]$$

$$h_{ed}(V_t) \approx \sum_{m=1}^{q}\left(\left(r_0 + \sum_{k_2=(m-1)N_2/q+1}^{mN_2/q} DNL_2[k_2]\right)\sum_{k_1=1}^{m} DNL_1[k_1 + q(d-1)]\right) \qquad (6.b)$$

If the standard deviations of the DDEM DAC and dither DAC DNL[k]'s are σ_1 and σ_2 respectively. The variance of $h_{ed}(V_t)$ is given by

$$Var_{ed}(V_t) \approx \left(\sum_{k=1}^{q} k\frac{N_2}{q}\sigma_2^2\right)\cdot\sigma_1^2 = \frac{(q+1)\sigma_1^2 N_2\sigma_2^2}{2}$$

The variance for $h_e(V_t)$ is

$$Var_e(V_t) = p \cdot Var_{ed}(V_t) \approx \frac{N_1\sigma_1^2 N_2\sigma_2^2}{2} \qquad (7)$$

The normalized $h_e(V_t)$ standard deviation is given by

$$\overline{\sigma}_e = \sqrt{Var_e\left(V_t\right)} / \left(N_1 p N_2\right) \approx \sqrt{2}\sqrt{N_1/2}\sigma_1 \cdot \sqrt{N_2/2}\sigma_2 / \left(N_1 p N_2\right)$$

Also usually we have

$$\sigma_{INL_{k1}} = \sqrt{N_1/2}\sigma_1 \text{ and } \sigma_{INL_{k2}} = \sqrt{2N_2/2}\sigma_2 .$$

If $n_{ENOB1} = \log_2\frac{N_1}{\sigma_{INL_{k1}}}$ and $n_{ENOB2} = \log_2\frac{N_2}{\sigma_{INL_{k2}}}$

Then $\log_2 \frac{1}{\bar{\sigma}_e} = \log_2 p + n_{ENOB1} + n_{ENOB2} - 0.5$.

We may ignore this -0.5 and the equivalent test performance of the DiDDEM DAC will be equivalent to that of a DAC with ENOB equal to

$$\tilde{n}_{ENOB} \approx \log_2 p + n_{ENOB1} + n_{ENOB2} \qquad (8)$$

In reality, when other non-idealities are included, the test performance might be a little bit lower than given in (8).

VI. Simulation Results

The test performance using the proposed DiDDEM DAC is verified by simulation. In the simulation, the DDEM DAC is a 9-bit DAC and the dither DAC is a 6-bit DAC, and both have the same current element distribution with normalized standard deviation equal to 0.1, which means the mismatch can be up to about 30% if counting the 3σ range. The DDEM iteration number p is 64. The simulated ADCs under test are 14-bit ADCs. The estimated INL[k] and INL with the DiDDEM DAC as test stimulus are compared to true INL[k] and INL. The differences are the test errors using the DiDDEM DAC.

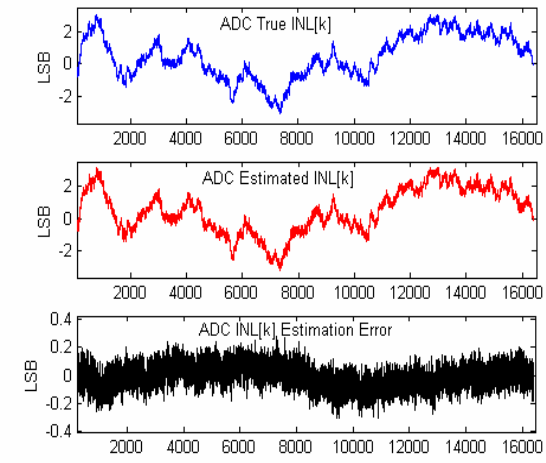

Figure 2. ADC true & est. INL[k] and estimation error

Figure 2 depicts the ADC true INL[k], estimated INL[k] curves and estimation error from a single simulation. The simulated DDEM DAC has an INL of 1.89 LSB at 9 bits level, and the dither DAC has an INL of 1.16 LSB at 6 bits level, so $n_{ENOB1}+n_{ENOB2}\approx 12$ bits. According to (8), the expected test performance is $n_{ENOB1}+n_{ENOB2}+\log_2 p \approx 18$ bits. In simulation, the ADC true INL is 3.15 LSB, and the estimated INL is 3.25 LSB. INL estimation error is only 0.1 LSB. The maximum INL[k] estimation error is 0.3 LSB at 14-bit level. So the test performance is at about 16 bits level. The actual achieved test performance is comparable to that predicated by (8).

To verify the robustness of the DiDDEM approach, 100 DiDDEM DACs are simulated to test 100 ADCs respectively. The simulation setting is the same as previous. Figure 3 shows the estimated INL versus the true INL curve for these 100 DAC-ADC pairs. The maximum INL estimation error (estimated INL – true INL) is 0.42LSB and the minimum error is –0.15LSB. First, the errors are quite small, which means the DiDDEM approach is robust. Secondly, the lower bound (-0.15) is adequately small, which means there is almost no risk of underestimating ADC's INL with the DiDDEM DAC, This merit is critical for real test, since it can guarantee no "bad" parts are delivered as "good" parts.

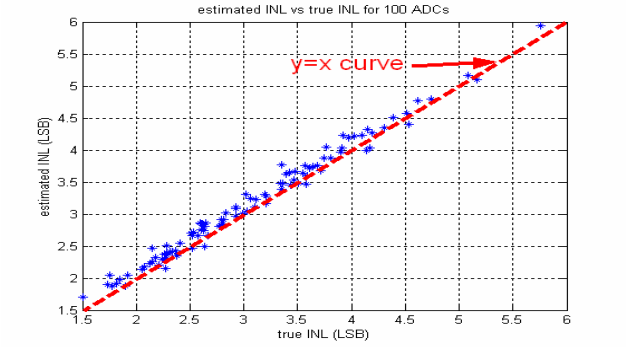

Figure 3. Estimated INL vs true INL for 100 ADCs

VII. Conclusion

A new dither incorporated deterministic dynamic element matching (DiDDEM) approach has been proposed for high resolution ADC test using extremely low resolution DACs. With this approach, the outputs of a DDEM DAC and a dither DAC are combined and serve as the stimulus to the ADC under test. Theoretical analysis shows that the test performance of a DiDDEM DAC is equivalent to that of a linear DAC with ENOB equal to the summation of the DDEM DAC ENOB and dither DAC ENOB plus $\log_2 p$, where p is the DDEM iteration number. Simulation results show that the actual test performance is comparable to the theoretical prediction. The robustness and reliability of this approach are also verified by simulation. The future work will include verifying this new approach with experimental results and implementing a DiDDEM DAC on-chip for BIST environment validation.

References

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