Fast-Switching Adaptive Bandwidth Frequency Synthesizer using a Loop Filter with Switched Zero-Resistor Array

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Abstract— **Secondary glitches caused by the switching of bandwidth in adaptive-bandwidth frequency synthesizers, are studied and a simple solution based on stepped-bandwidth switching is proposed to reduce their effects on the switching time of the synthesizer. Behavioral simulations using GSM specifications indicate nearly 35% improvement in switching time using the proposed solution.**

I. INTRODUCTION

Frequency synthesizers are ubiquitous in today's wireless communication systems. In the design of PLL frequency synthesizers, there exists a trade off between the settling time and spur level at the output [1] [2]. Though theory allows a maximum of 1/10 of the reference frequency for the loop bandwidth, practically the bandwidth is several orders of magnitude smaller than this limit in order to meet the noise specification. Further in Integer-N synthesizers, the reference frequency cannot exceed the channel spacing. These limitations result in elongated switching times for conventional synthesizers.

A common solution to offset the limitation on the loop bandwidth set by the noise requirement is to use an adaptive bandwidth synthesizer [3]. In this approach, high loop bandwidth is used during frequency jumps and the loop bandwidth is restored to its nominal value after the frequency has settled to its new value. The loop bandwidth in high bandwidth mode is still limited by the reference frequency, the theoretical maximum being 1/10 of the reference frequency. The switching of bandwidth is accomplished by switching an element in the loop filter usually a resistor. If the synthesizer has to settle to a very small frequency error in a very short time, it becomes important to make the transition from high bandwidth to low bandwidth as smooth as possible; otherwise the glitches arising from switching of bandwidth contribute significantly to the overall switching time [4]. An applicable case is the synthesizer used in a GSM base station transmitter which has a switching time specification of less than 10μs for a frequency jump of 75MHz with 0.1ppm tolerance. This work focuses on studying the non-ideal effects in the elements of the loop filter that can cause the transition from high bandwidth to low bandwidth to be not as smooth as desired. A solution is then proposed to counter these effects.

This paper is organized as follows. In section II, the basic principle of an adaptive bandwidth synthesizer is explained in terms of loop parameters and also the secondary glitch effects are studied. In section III, the proposed solution for controlling the secondary glitches is described. In section IV, verification of the proposed scheme through behavioral level simulations is presented followed by conclusions.

II. BASIC PRINCIPLE OF AN ADAPTIVE PLL SYSTEM

The switching time of an under damped type-II second-order PLL is given by

$$t_s \cong \frac{\ln\left(\dfrac{\Delta f_o}{\varepsilon\sqrt{1-\zeta^2}}\right)}{\omega_n \zeta} \qquad (1)$$

where Δf_o is the output frequency step, ε is the frequency error tolerance, ω_n is the natural frequency and ζ is the damping factor of the loop. Thus, the settling time for a given frequency step and error tolerance depends on the natural frequency and the damping factor. The switching time can also be expressed in terms of the change in VCO tune voltage corresponding to the frequency step Δf_o in which case the frequency error tolerance ε will be replaced with the equivalent tune voltage error tolerance. The VCO gain sensitivity relates the equivalent parameters in the two

expressions. Since a closed-form expression for switching time of a type-II third-order loop shown in fig. 1 is difficult to obtain, we will neglect the effect of loop filter pole in this discussion. This is a valid assumption since the pole can be added only after locking is complete if so chosen. The natural frequency and the damping factor (ignoring C_p) are given by:

$$\omega_n = \sqrt{\frac{I_{cp} K_{vco}}{2\pi N C_z}} \tag{2}$$

$$\varsigma = \frac{1}{2}\tau_z \sqrt{\frac{I_{cp} K_{vco}}{2\pi N C_z}} \tag{3}$$

where $\tau_z = R_z C_z$.

Equations (1), (2), (3) indicate that to reduce the settling time by a factor of β, the natural frequency has to be increased by a factor of β while keeping the damping factor constant. In terms of the loop component parameters this is equivalent to increasing the charge pump current I_{cp} by a factor of β^2 and reducing the zero resistor R_z by a factor of β. The open loop bandwidth increases by a factor of β with the reduction in R_z. Even though noise requirements limit the loop bandwidth to be narrower, it can be made wider during the locking process and then restored after lock is established. This is the basic principle of operation of the adaptive PLL of fig. 1. The lock signal generated by a lock-detect circuit not shown, or a predetermined timing signal is utilized for the adaptive bandwidth control.

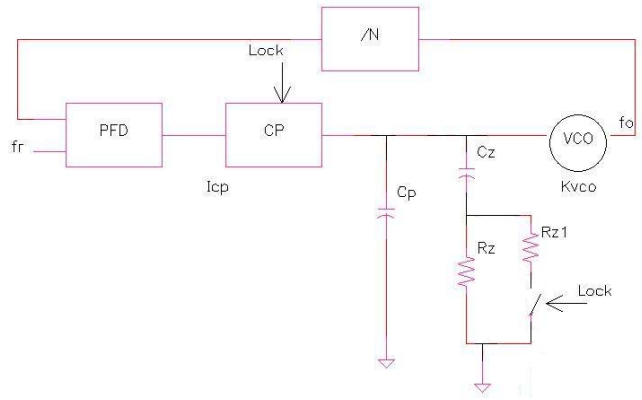

Figure 1 Adaptive Bandwidth Synthesizer

The adaptive system described above can be employed to achieve significant improvement in the lock time as long as the theoretical limit on loop bandwidth, which is 1/10 of reference frequency, is not exceeded during the high-bandwidth mode. However, as discussed in section I it is important to limit the level of secondary glitches when switching from high bandwidth to low bandwidth mode. Switching a memory less element such as a resistor inside a filter that's completely settled should not give rise to transient behavior. Thus the sources of the secondary glitches are the parasitic capacitances associated with the switch element (typically an NMOS). At the time of frequency jump, the switch in fig. 1 is closed to reduce the effective resistance in the loop filter by a factor β. When the settling is complete the switch has to be opened to restore the bandwidth. The transitions on the voltage signal controlling the on/off states of the MOS switch cause glitches on the tune voltage line. The size of the parasitic gate-drain capacitance of the MOS switch determines among other things, the level of these glitches. If the tune voltage has already settled to within the tolerance window at the time of turning off the MOS switch, then the glitches can cause the tune voltage to swing outside of the window, thus increasing the over all lock time of the synthesizer.

III. PROPOSED SCHEME

As described in section II, minimizing the gate-drain capacitance of the MOS switch helps to restrict the level of glitches to within the tolerance window. A second factor that determines how fast the VCO tune voltage settles after a glitch occurs, is the effective bandwidth after switching. Thus if a relatively large MOS switch is used to switch from 8x bandwidth (high bandwidth) to 1x bandwidth (nominal bandwidth), then the size of the MOS switch and the 1x bandwidth after switching together contribute to significantly large switching time. Instead in this paper, a scheme is proposed wherein bandwidth is reduced from 8x to 1x in several steps using multiple MOS-switched resistors in parallel with the nominal zero-resistor R_z to form a switched-resistor-array. The largest sized MOS switch in the array would still be smaller than the single MOS switch used in the one-step approach. To keep the damping factor constant and only increase the natural frequency the following relationship has be valid at each of the bandwidth steps.

$$\sqrt{I_{cp}} \times R_z = constant \tag{4}$$

One of the factors determining the effectiveness of the proposed scheme is the pattern used for the steps. There are several possibilities such as binary stepping of I_{cp}, linear stepping of I_{cp} or the Fibonacci pattern for I_{cp}. Binary stepping and the Fibonacci pattern result in successive bandwidths being close to each other near the nominal bandwidth and far apart near the high bandwidth. Linear stepping of bandwidth results in equal-sized MOS switches and is also an optimum choice. Though the different patterns were simulated, the results are presented in section IV only for the binary pattern. Note that once the high bandwidth and the type of pattern are chosen, the no. of steps will be fixed. For, example if the high bandwidth is 8 times the nominal bandwidth and if binary stepping of I_{cp} is chosen, then the

no. of steps will be six corresponding to I_{cp} multipliers of 64, 32, 16, 8, 4, 2, 1. The second factor determining effectiveness is the time at which each step occurs. In the two-step case presented in section IV, the time for the next step is chosen to be the time of the first zero-crossing of the tune voltage in the current step. +/- 15% variation of this time has also been considered to demonstrate the robustness of the proposed scheme.

IV. BEHAVIORAL SIMULATION

The proposed scheme is verified through behavioral simulation of a synthesizer using GSM specifications. In order to focus primarily on the non-idealities of the switches used to adjust the loop filter resistor, the simulation setup uses ideal components except for the NMOS transistors, which. In all the branches of the switched-resistor-array, containing a fixed resistor and a MOS switch, the on-resistance of the switch is always chosen to be 1/10 of the fixed resistance. Firstly, comparison is done between the switching times obtained in the following two cases.

Case1: High bandwidth switched to nominal bandwidth in one step

$$8x \rightarrow 1x$$

Case2: High bandwidth switched to nominal bandwidth in two steps

$$8x \rightarrow \text{sqrt}(8)x; \quad \text{sqrt}(8)x \rightarrow 1x$$

The simulation setup used for the two cases is shown in fig. 2. The list of common specifications is given below:

Frequency jump: 1710 MHz - 1785 MHz

Reference Frequency: 26 MHz

Nominal charge pump current (1x): 0.213 mA

Nominal loop bandwidth (1x): 40 kHz

Intermediate loop bandwidth (sqrt(8)x): 113 kHz

High loop bandwidth (8x): 320 kHz

Phase margin: 46.4^{o}

VCO gain: 37.5 MHz/V

Loop filter zero: 16 kHz

Loop filter pole: 100 kHz

Nominal R_z: 2.5 K

C_z: 3.98nF

C_p: 758pF

In the one-step case, the bandwidth is switched at 10.5µs, whereas in the two-step case, the first step occurs at 10.5µs and the second at 11.43µs. Fig. 3 shows the locking profile where the VCO tune voltage settling to the tolerance window is shown against time. The total switching time is 18.21µs for the one-step case and 11.75µs for the two-step case. This is nearly 35% improvement in the switching time.

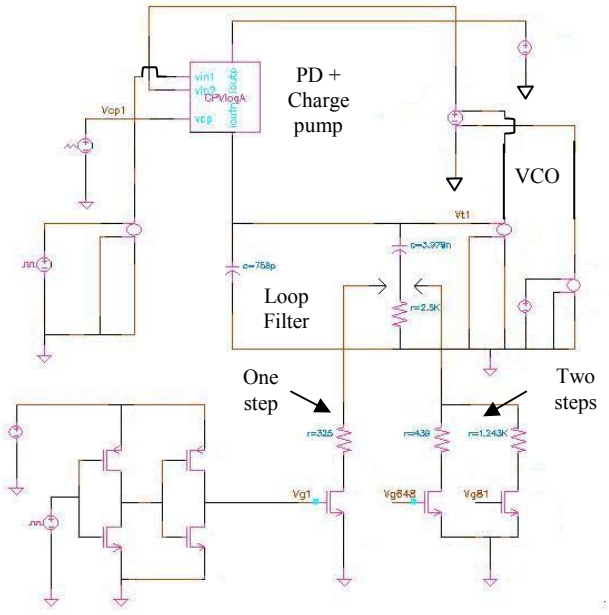

Figure 2 Simulation setup to compare one step vs two-step bandwidth switching

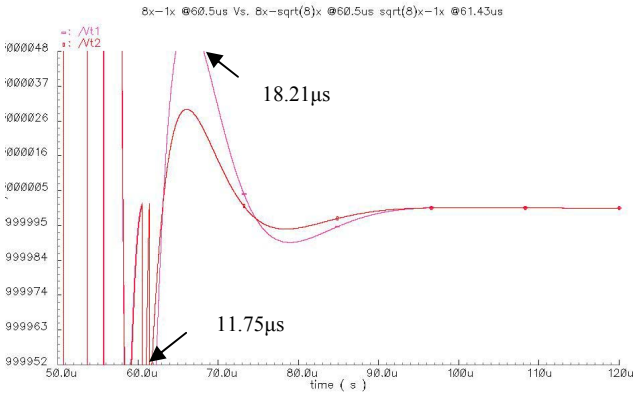

Figure 3 Locking profile for one- and two-step bandwidth switching

It was mentioned in section III that the time at which switching of bandwidths has to occur is determined based on the zero-crossings of the tune voltage. To demonstrate robustness of the proposed scheme, simulations are performed with +/- 15% variations in these times. Table 1 shows the results of these simulations. It can be observed that with the variations included, there is still 35% improvement in the total switching time.

Table 1 Switching time Variations

One step at t_{sw}	Total switching time	Two steps; first step at t_{sw1}; second step at t_{sw2}		Total switching time
t_{sw}(µs)	t_s(µs)	t_{sw1}(µs)	t_{sw2}(µs)	t_s(µs)
10.5	18.21	10.5	11.43	11.75
			11.29	11.84
			11.57	11.67
10.14	18.46	10.14	11.43	11.43
			11.29	11.29
			11.57	11.57
10.36	19.11	10.36	11.43	11.52
			11.29	11.61
			11.57	11.57

Finally, a synthesizer with six bandwidth steps is simulated. The first step occurs at 8.1µs and time between subsequent steps is 0.5µs. Simulation setup is shown in fig. 4 and the results are shown in fig. 5. I_{cp} and R_z at each step are multiplied by factors as shown below.

I_{cp} multiplier: 64 → 32 → 16 → 8 → 4 → 2 → 1

R_z fraction: 1/8 → $1/\sqrt{32}$ → 1/4 → $1/\sqrt{8}$ → 1/2 → $1/\sqrt{2}$ → 1

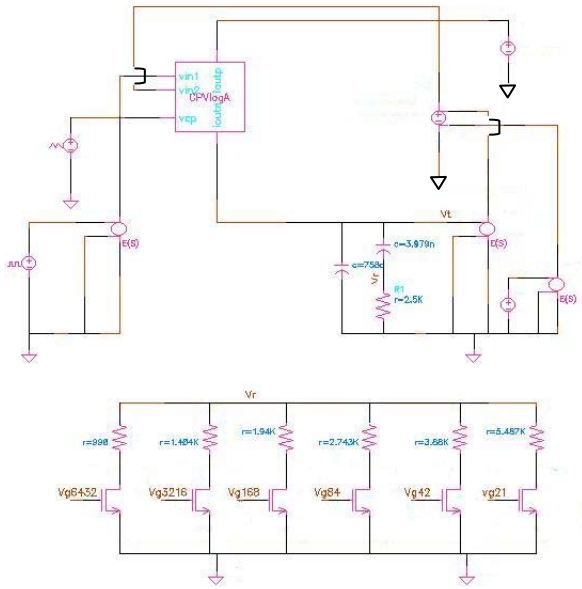

Figure 4 Simulation setup for six step bandwidth switching

The total switching time in this case is 10.62µs.

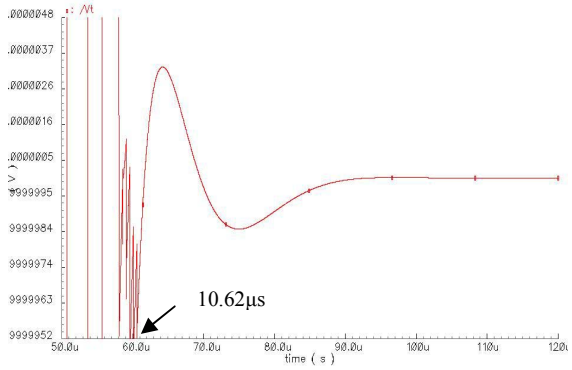

Figure 5 Locking profile for six step bandwidth switching

CONCLUSIONS

In adaptive bandwidth synthesizers, the effect of secondary glitches sometimes dominates the overall switching time. The stepped bandwidth approach presented in this paper achieves significant improvement in overall switching time for the cases studied. It is a simple and practical on-chip solution. A rigorous optimization in the areas mentioned earlier, would make this solution viable for many applications.

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