Power Dependence of Feedback Amplifiers on OpAmp Architecture

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***Abstract*— Power optimized design strategies for operational amplifiers (opamps) used in finite gain feedback applications with fixed closed-loop settling constraints are introduced. A comparison of several opamp architectures shows that the optimal amplifier architecture is dependent upon the desired closed-loop gain. Closed form expressions are given which relate power dissipation and closed loop bandwidth for a given closed loop gain.**

I. Introduction

The design of power efficient Analog-to-Digital converts (ADC) with high accuracy and high speed is a growing interest to the semiconductor industry. The common choice for such ADCs is a pipeline structure where the individual stage amplifiers define the total power consumption. In the literature one can find many different amplifier architectures but most are minor variants of a small number of well-known structures. The amplifier performance in general and the power efficiency in particular are strongly dependent upon architecture. For high speed and high accuracy requirements, these amplifiers often become the bottleneck in the design. Several authors have focused on design optimization. A good survey of such approaches is available in [1]. Two similar approaches utilizing analytical equation-based optimization are discussed in [2] and [3]. Both techniques rely on posynomiality of the amplifier performance equations under specific constraint conditions. Work done by Mandal [3], includes a procedure to update these constraint conditions after each iteration to get a better solution whereas Hershenson's work [2] includes the parasitic capacitance effects that are the dominant contributor for a high speed performance. The optimized results in both the approaches are based on numerical approaches and hence lack an intuitive insight into amplifier design and the choice of architecture. Regardless, there is minimal use of these approaches in industry today.

An alternative analytical approach is presented in [4]. In the paper it was shown that the use of an alternate design space can help designers better understand the operation of the amplifier. This alternate design space has been exploited for finding an optimized design of CMOS opamp in [5]. In Loulou's work on the two stage amplifier [5], the effects of the loop factor (β) in a closed loop negative feedback configuration on the compensation capacitance (C_c) have not been included. In this work analytical expression for the relationship between settling time, C_c, and power dissipation in a two-stage opamp used in finite gain application are developed. A comparison of the performance of the optimized two-stage opamp with that of single stage opamp is made to facilitate the selection of an optimal amplifier topology.

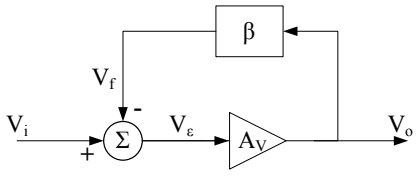

Fig. 1. Negative Feedback Configuration

II. Amplifier Optimization Formulation

Consider an amplifier in a negative feedback configuration as shown in Fig. 1. The closed loop gain is given by

$$A_{FB}(s) = \frac{V_o}{V_i} = \frac{A_V(s)}{1 + \beta A_V(s)} \tag{1}$$

We will be considering three simple amplifier structures: a single stage amplifier, a two stage amplifier with Miller compensation and a two stage amplifier with Miller and Resistive compensation.

A. Case 1: Single Stage Amplifier

The Gain-Bandwidth product, GB, is defined as the product of the DC gain and the 3 dB bandwidth. For a simple single stage amplifier of Fig. 2, GB can be expressed in the alternate design space with parameters $\{P, V_{EB1}, V_{EB3}\}$ [4] as,

$$GB = \frac{g_{m1}}{2C_l} = \frac{P}{2V_{DD}V_{EB1}C_l} \tag{2}$$

where V_{EB1} is the excess bias of the input transistor M_1, V_{EB3} is the excess bias of the load transistor M_3, P is the total power consumption in the amplifier, C_l is the total load capacitance at the output node and where the diffusion capacitances have been neglected. The GB is independent of the loop factor β. This expression becomes more complex if the diffusion capacitances are included. Consider the transistor depicted in Fig. 3. If we assume that the sidewall parasitic capacitances associated with the X_A and X_B sides can be neglected, the

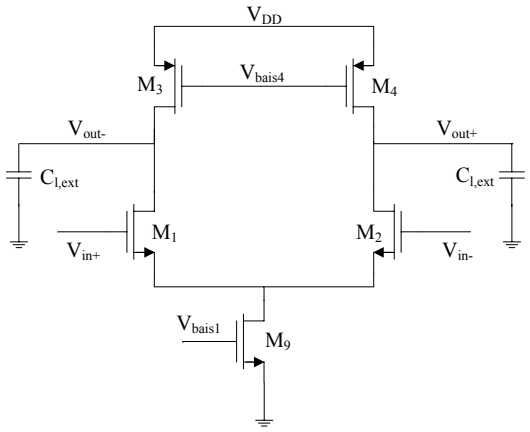

Fig. 2. Single Stage Amplifier

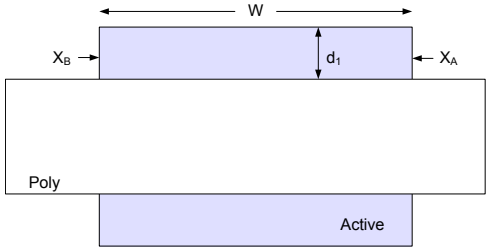

Fig. 3. Transistor Layout

parasitic capacitances associated with the n-transistors and the p-transistors are given by,

$$\begin{aligned} C_{p_n} &= W_n C_{SW_n} + W_n d_1 C_{Bottom_n} \\ C_{p_p} &= W_p C_{SW_p} + W_p d_1 C_{Bottom_p} \end{aligned} \quad (3)$$

where C_{SW} is the side-wall capacitance density, C_{Bottom} is the bottom capacitance density associated with the active region of the transistors and d_1 is the extension of the active region from the poly, typically 5λ or 6λ, where 2λ is the minimum feature size of a given process. We can define parasitic capacitance factor for n-channel and p-channel as

$$\begin{aligned} C_{x_n} &= (C_{SW_n} + d_1 C_{Bottom_n}) \frac{1}{c_{ox} L_{min}} \\ C_{x_p} &= (C_{SW_p} + d_1 C_{Bottom_p}) \frac{1}{c_{ox} L_{min}} \end{aligned} \quad (4)$$

where $L_{min} = 2\lambda$ and c_{ox} is the capacitance of oxide. Hence the total capacitance is

$$C_l = C_{l,ext} + (W_n C_{x_n} + W_p C_{x_p}) c_{ox} L_{min} \quad (5)$$

Under the assumption that $L_1 = L_3 = L_{min}$, from (2) and (5), GB can be rewritten as,

$$GB = \frac{P}{2V_{DD} C_{l,ext} V_{EB1} + \frac{2PL^2_{min}}{\mu_n V_{EB1}} \left[C_{x_n} + C_{x_p} \frac{\mu_n}{\mu_p} \frac{V^2_{EB1}}{V^2_{EB3}} \right]} \quad (6)$$

The second denominator term in (6) represents the total parasitic contribution from the n-channel and p-channel transistors. The GB in (6) is a function of P, V_{EB1} and V_{EB3} and is an increasing function of V_{EB3}. Therefore the output swing requirement will define the maximum allowable V_{EB3}. Another observation is that GB has a physical limit which is defined by the process. At this stage one can look at two optimization problems: first maximizing GB under fixed power conditions; second minimizing power requirement for fixed GB application. Both cases will reduce to a two dimensional problem. However, the latter case is more commonly encountered in most of the applications since GB of the amplifier would be defined by the settling requirements. For this, the design space variables needs to be changed to $\{GB, V_{EB1}, V_{EB3}\}$ and P is considered a dependent variable. From (6), the required power can be expressed as

$$P = \frac{2V_{DD} V_{EB1} C_{l,ext} GB}{\left[1 - 2GBL^2_{min} \left\{ \frac{C_{x_n}}{V_{EB1} \mu_n} + \frac{C_{x_p} V_{EB1}}{V^2_{EB3} \mu_p} \right\} \right]} \quad (7)$$

provided

$$V_{EB1,min} < V_{EB1} < V_{EB1,max} \;\&\; V_{EB3} \geq V_{EB3,min} \quad (8)$$

where

$$\begin{aligned} V_{EB1,min/max} &= \left[C \mp \sqrt{C^2 - D} \right] E \\ V_{EB3,min} &= 4GBL^2_{min} \sqrt{\frac{C_{x_n} C_{x_p}}{\mu_n \mu_p}} \\ C = \frac{1}{2GBL^2_{min}},\; D &= \frac{4C_{x_n} C_{x_p}}{V^2_{EB3} \mu_n \mu_p} \;\&\; E = \frac{V^2_{EB3} \mu_p}{2C_{x_p}} \end{aligned} \quad (9)$$

and keeping V_{EB3} fixed, P will be only a function of V_{EB1}. The minimum power required to achieve the given GB w.r.t V_{EB1} is given by

$$P_{opt} = \frac{16V_{DD} C_{l,ext} GB^2 L^2_{min} C_{x_n}}{\mu_n \left[1 - 16 \frac{GB^2 L^4_{min}}{V^2_{EB3}} \frac{C_{x_n} C_{x_p}}{\mu_n \mu_p} \right]} \quad (10)$$

The required V_{EB1} for achieving P_{opt} is given by

$$V_{EB1,opt} = 4GBL^2_{min} \frac{C_{x_n}}{\mu_n} \quad (11)$$

which is a function of GB and the process only and independent of V_{EB3}. A plot of power vs. V_{EB1} is shown for different values of V_{EB3} in Fig. 4 for TSMC $0.35\mu m$ process with V_{DD} of 2V, $C_{l,ext}$ of 1.5pF and GB requirement of 1.32GHz.

B. Case 2: Two Stage Miller Compensated Amplifier

The transfer function of the two stage Miller compensated amplifier of Fig. 5 can be expressed as

$$A(s) = \frac{V_{out+}}{V_{in+} - V_{in-}} = \frac{g_{m1}(g_{m5} - sC_c)}{2(s^2 C_c C_l + s g_{m5} C_c + g_{oo} g_{od})} \quad (12)$$

where g_{m1} is same as before, g_{m5} (or g_{m7}) is the transconductance of the 2^{nd} stage input transistor, C_c is the Miller capacitance and g_{dd} and g_{oo} are the output conductances of the 1^{st} and 2^{nd} stages respectively. For the amplifier in a negative

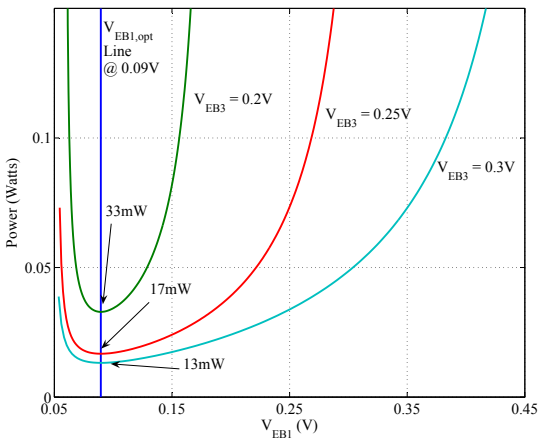

Fig. 4. Power vs. V_{EB1} for single stage amplifier

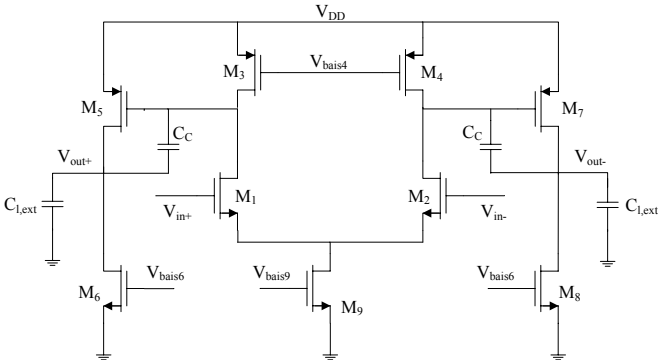

Fig. 5. Two stage Miller Compensated Amplifier

feedback configuration with loop factor of β and pole Q, it can be shown that the

$$C_c = \frac{\beta C_l}{2Q^2} \frac{\frac{\theta}{\gamma(1-\theta)}}{(\frac{\theta}{\gamma(1-\theta)} - \frac{\beta}{2})^2} \text{ provided } \theta > \frac{\beta\gamma}{2+\beta\gamma} \quad (13)$$

where θ is the ratio of the current in the output stages w.r.t. the total current and γ is the ratio of the excess bias of the 2^{nd} stage input transistor to that of the 1^{st} stage input transistor. Hence the value of C_c dramatically reduces as θ approaches 1. The GB in the alternate design space, with design variables $\{P, V_{EB1}, V_{EB6}, \theta, \gamma, \beta, Q\}$, where V_{EB6} and V_{EB8} are same, can be derived as

$$GB = \frac{PQ^2}{V_{DD}V_{EB1}C_l} \frac{(\theta - \frac{\beta\gamma}{2}(1-\theta))^2}{\beta\gamma\theta} \quad (14)$$

It can be shown that GB is a monotonically decreasing function of γ but for practical purpose we will use $\gamma = 1$. Similarly, GB is a monotonically increasing function of θ. Allocating more power consumption in the 2^{nd} stage as opposed to the 1^{st} stage will result in larger value of GB. Under these conditions, GB is inversely proportional to β, i.e., decrease in the β value will results in higher achievable GB. A similar analysis of power optimization can be done for a fixed GB and V_{EB6} including the parasitics of the 2^{nd} stage only. The optimized power is given by

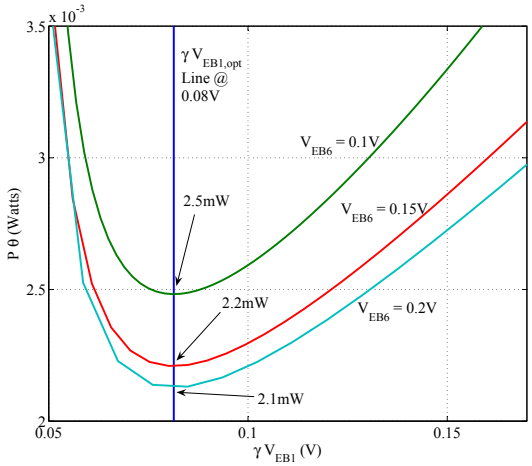

Fig. 6. $P\theta$ vs. γV_{EB1} for two stage Miller compensated amplifier

$$P_{opt}\theta = \frac{4V_{DD}C_{l,ext}GB^2L_{min}^2C_{x_p}}{\mu_p\left[\frac{Q^4}{\beta^2} - \frac{4GB^2L_{min}^4}{V_{EB6}^2}\frac{C_{x_n}C_{x_p}}{\mu_n\mu_p}\right]} \quad (15)$$

and the corresponding required V_{EB1} is

$$\gamma V_{EB1,opt} = 2GBL_{min}^2\frac{C_{x_p}}{\mu_p}\frac{\beta}{Q^2} \quad (16)$$

Even though we are optimizing $P\theta$ in this case, for $\theta \approx 1$ the total power consumption will be approximately equal to $P\theta$ value. Plot of $P\theta$ vs. γV_{EB1} is shown for different values of V_{EB6} in Fig. 6 for β of 0.25 and other parameters as listed in the previous section of single stage amplifier. In this simple analysis, we have neglected the internal node parasitics in order to develop an insight to the behavior of an amplifier.

C. Case 3: Two Stage Miller and Resistive Compensated Amplifier

For the amplifier in Fig. 7, it is possible to move the right half plane zero to left half plane by adjusting the compensating resistance (R_c). This adjustment can cancel the 2^{nd} high frequency pole and reduces the system to a single pole system. To avoid long settling due to pole-zero cancellation mismatch, 1^{st} pole in feedback (p_{1f}) should not be beyond the open loop 2^{nd} pole (p_2), i.e.

$$|p_{1f}| = \eta|p_2| \qquad \text{where} \qquad 0 \leq \eta \leq 1 \quad (17)$$

The compensating capacitance for this case is given by

$$C_c = \left(1 + \beta\frac{g_{m1}g_{m5}}{2g_{oo}g_{od}}\right)\frac{g_{oo}g_{od}}{\eta\psi^2 g_{m5}^2}C_l,\ \psi = 1 + \frac{g_{oo}g_{od}}{g_{m5}g_c} \quad (18)$$

and the compensating resistance is

$$g_c \approx \frac{g_{m5}}{1 + \eta\frac{2}{\beta}\frac{g_{m5}}{g_{m1}}} \quad (19)$$

For this case, the alternate design space is $\{P, V_{EB1}, V_{EB6}, \theta, \gamma, \beta, \eta\}$. Including the parasitics of

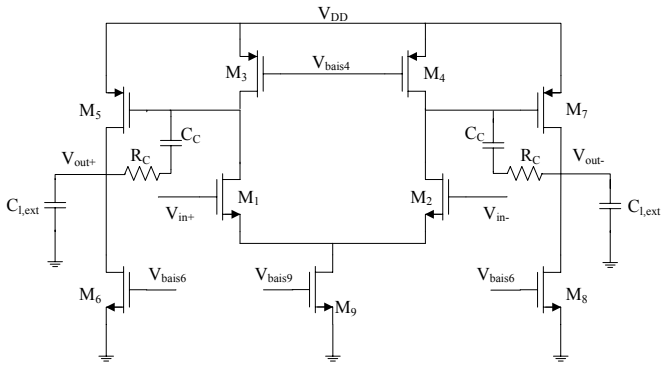

Fig. 7. Two Stage Miller and Resistive Compensated Amplifier

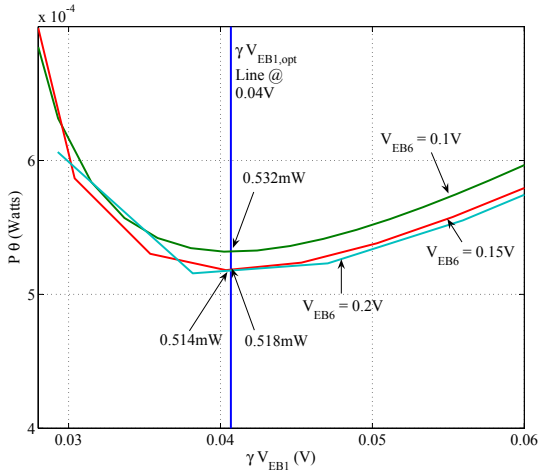

Fig. 8. $P\theta$ vs. γV_{EB1} for two stage amp. with Miller and Res. compensation

2^{nd} stage only and assuming that $\theta \simeq 1$, it can be shown that only Q^2 needs to be replaced by η in the analysis of section II-B. Similar plot of $P\theta$ vs. γV_{EB1} is shown in Fig. 8 for $\eta = 1$.

III. Results

A comparative study of three common opamp structures was performed using the TSMC $0.35\mu m$ process. Table I summarizes the optimal power requirement for respective optimal excess bias conditions for the three structures. The results were derived for $\beta = \frac{1}{4}$, $GB = 1.3$ GHz and $C_{l,ext} = 1.5$ pF. Note that for case 3, the optimized excess bias is too low. Such low value of excess bias will cause the transistors to go out of saturation region. To avoid that possibility, if the excess bias for the same structure is increased to 0.1 V, same GB performance can be achieved for power consumption of 0.8 mW. Even with this higher excess bias, power saving of 3 to 4 times can be achieved as compared to case 2. This power saving is originating from the fact that for the case 2 amplifier we need to move the 2^{nd} pole far away from GB frequency for proper compensation. Similarly, when comparing case 1 with case 2 (or case 3), the power saving results from the fact that the gain of the 1^{st} stage of a two stage structure is essentially free as it requires very low power.

TABLE I

Comparison of power requirement for the three structures

Case	P_{opt}(mW)	$V_{EB1,opt}$(V)
1 (II − A)	13 − 17	0.09
2 (II − B)	2 − 2.5	0.08
3 (II − C)	~ 0.5	0.04

For given application specifications, if we compare the optimized power requirement of case 1 with that of case 2 (or case 3), we can derive a critical value of the loop factor (β_{crit}). If the calculated β_{crit} is larger than the desired β, i.e., $\beta_{crit} > \beta_{desired}$, the designer would choose structure of case 2 (or case 3). Conversely, if $\beta_{crit} < \beta_{desired}$, case 1 structure would be used. Comparing (10) and (15), β_{crit} is given by

$$\beta_{crit} = 2\zeta\left[16GB^2L_{min}^4\frac{C_{x_n}C_{x_p}}{\mu_n\mu_p}\left\{\frac{1}{(V_{EB6}^{TS})^2} - \frac{\mu_nC_{x_p}}{(V_{EB3}^{SS})^2\mu_pC_{x_n}}\right\} + \frac{\mu_nC_{x_p}}{\mu_pC_{x_n}}\right]^{-\frac{1}{2}} \quad (20)$$

where $\zeta = Q^2$ for case 2 or $\zeta = \eta$ for case 3, V_{EB6}^{TS} is the excess bias of the load transistor of the 2^{nd} stage of a two stage structure and V_{EB3}^{SS} is the excess bias of the load transistor of a single stage structure. The β_{crit} is a function of GB, excess biases and process. For $V_{EB6}^{TS} = V_{EB3}^{SS} = 0.25$ V, the β_{crit} value for case 2 is approximately 0.65 whereas for case 3 is approximately 1.29.

IV. Conclusion

A comparative study of the tradeoffs between power dissipation and settling time for three common amplifier architectures was presented. It was shown that a two stage structure gives better overall performance for high feedback gains whereas the single stage structure performs better for smaller feedback gains. From optimized power expressions, a critical value of feedback factor was derived. For a given set of specifications, a strategy was proposed to use this factor for choosing the appropriate power optimized amplifier structure.

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