A Test Strategy for Time-to-Digital Converters Using Dynamic Element Matching and Dithering

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Abstract-**This work presents a cost-effective test structure that is applicable to built-in self-test of time-to-digital converters (TDCs). The proposed structure uses deterministic dynamic element matching and dithering to generate linear time interval excitations for precision TDC test. Transition time points of a TDC can be measured with picosecond accuracy by using the proposed strategy, which enables the test and calibration of TDCs used in jitter characterization of communications systems with multi-gigabit-per-second data rates.**

I. INTRODUCTION

The 2003 edition of the *International Technology Roadmap for Semiconductors* (ITRS) repeatedly identified jitter as a key parameter for many important yet ubiquitous circuit functions including transmitters, receivers, clock distribution circuits, high speed interfaces, and high speed analog source/capture [1]. It points out that "currently, jitter measurement capability on ATE is in its infancy, there is no instrument available" that is sufficient for even today's circuit specifications. Furthermore, "jitter testing results in high test-times and equipment capital costs" and "remains a key challenge," while the price of integrated circuit (IC) products continues to decrease, along with the increasing level of integration and the ever-shrinking feature size. The ITRS concludes that new jitter measurement methods need to be developed to manage the cost scaling.

Direct measurement of jitter in the time domain is commonly performed with a time-to-digital converter (TDC) or its equivalent. A TDC's full range, resolution, repeatability, and accuracy, as well as conversion speed are some of the most important specifications [2]. Sufficient range and raw resolution are relatively easy to achieve, but repeatability, accuracy and the speed are subject to fundamental limitations that are difficult to overcome. Intrinsic noise, which causes inherent jitter, and parasitics, which cause delay and distortion in the TDC itself, impose ultimate limits on the repeatability and speed. Systematic errors due to mismatch and other parametric variations contribute to the bulk of jitter measurement errors that cannot be reduced by averaging. In nearly all existing approaches of TDC design, focus is placed on limiting the systematic error to within a bound by reducing mismatches, which adversely leads to larger parasitics, slower operation, and larger inherent jitter. The random error from inherent jitter is reduced by averaging over a large number of samples, which further slows down the jitter measurement.

This work takes a fundamentally different approach to TDC design: we first focus on driving the inherent jitter and parasitics in the TDC to an absolute minimal level at the expense of introducing larger parametric variations; and then we use a built-in self-test (BIST)-based self-calibration method to correct systematic errors due to parametric variations. By doing so, the ultimate performance limit of the TDC can be dramatically enhanced in terms of repeatability and speed. The successful self-test and calibration will bring jitter measurement accuracy to the desired level. Pelka, Kalisz, and Szplet discussed digital calibration of TDCs based on tested nonlinearity characteristics and achieved 24 pS accuracy after correction [3]. Recently, Chan and Roberts reported a self-calibrating TDC structure that had 18.9 pS resolution [4]. More other important practices on self-test and calibration of TDCs can be found in the literature and not listed here because of the limited space.

In a conventional approach, calibrating all transition points of a TDC requires precisely known time intervals with a wide range of interval lengths, which is virtually impossible at the sub-nanosecond level. This work proposed a time interval generator using a Vernier delay line (VDL) with deterministic dynamic element matching (DDEM) and dithering. Time intervals generated by the VDL will range from a small fraction of a picosecond to the full range of a TDC and will be densely and nearly uniformly distributed over the total range as a consequence of DDEM and dithering. These time intervals will be presented to a TDC under test whose output histogram will be used to accurately characterize all transition points of the TDC. The transition point knowledge can then be easily used to generate calibration codes for the TDC output.

II. REVIEW OF TIME-TO-DIGITAL CONVERSION USING A VERNIER DELAY LINE

A VDL TDC contains two chains of delay stages, for which the gate delay in one chain is slightly larger than that in the other chain. A START signal and a STOP signal, which lags the START signal, go through the chains with larger and smaller delays, respectively. At the output of a pair of delay stages, the STOP signal will catch up a little bit with the START signal. The number

of stages before the STOP signal leads the START signal is a measurement of the time interval between the two signals, where the difference between the two gate delays is a quantization unit used in the measurement. Since this difference can be much smaller than either of the gate delays, the resolution of the VDL TDC is not limited by the intrinsic gate delay under a given technology.

Similar to transition points of an ADC, a transition point of a TDC, T_k, is defined to be the width of a time interval at which the TDC output code changes from k-1 to k. Nominally, increments between any two consecutive transition points in a VDL TDC are identical and equal to the difference between the gate delays in the two chains,

$$\tau_0 = \tau_{20} - \tau_{10} = T_k - T_{k-1} \qquad \text{for any } k, \tag{1}$$

where τ_{10} and τ_{20} are nominal small and large gate delays, respectively. These transition points are linearly spaced and lie on a straight line connecting the first and last transition point, usually called an end-point fit line. Unfortunately, mismatch errors in delay stages caused by process variation and gradient effects during fabrication will inevitably introduce errors into transition points of a TDC. These errors can be characterized by the term integral nonlinearity (*INL*), which is defined by

$$INL_k = \frac{T_k - T_1}{LSI} - (k-1), \tag{2}$$

and

$$INL = \max_k \{| INL_k |\}, \tag{3}$$

where INL_k is the deviation of the true transition point, T_k, from the end-point fit line, the least significant interval $LSI = (T_N - T_1)/(N-1)$ is the average increment between transition points and N is the total number of transition levels of the TDC. To calibrate a TDC will first need to find out the INL_k at each transition point.

III. TDC Test Using DDEM and Dithering

The histogram method is one of the most widely used methods for ADC linearity testing. We will also use it to test TDCs. If we can generate START and STOP signals with time intervals in between uniformly distributed over the dynamic range of a TDC under test and use them to excite the TDC, the probability of output codes belonging to [1, k) is proportional to T_k-T_1 and can be used to estimate a TDC's linearity. Now the problem is how to generate two signals with uniformly distributed time difference. Conventional approaches use well-designed accurate circuits to generate the time intervals. These circuits are usually very expensive and may not be applicable to on-chip test. This work proposes a strategy of using low-accuracy circuits to generate time intervals, while the uniform distribution is guaranteed by using DDEM and dithering.

A. Time Interval Generation Using DDEM

In our proposed method, the basic time interval generation structure is an N-stage VDL with its head connected to its tail to form a loop, as shown in Figure 1. There are three types of switches used in this VDL to do DDEM: "I set" selects the node for the trigger signal; "A set" selects the node for the START signal; and "B set" selects the node for the STOP signal.

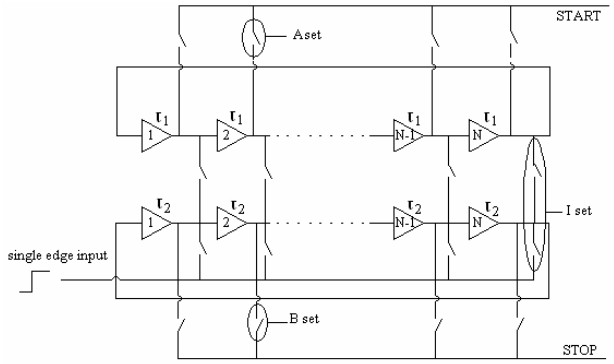

Figure 1. A time interval generator using a VDL with DDEM.

For a specific delay length, we control the three sets of switches to generate P output intervals, each of which generated by different stages on the loop. The following are the specific steps, where we define q=N/P for convenience of description:

1) We first input the trigger signal to the first stage by closing the I set switches after the N^{th} stage, and take the START and STOP at the outputs of the k^{th} stages of the fast and slow chains, respectively, by closing associated A set and B set switches. A time interval sample is obtained as the difference between the total delays of first k stages on the fast and slow chains.

2) We repeat step 1) by P-1 times, each time the position of the closed I set, A set and B set switches are shifted by q stages. For the d^{th} sample, the trigger signal is input to the (d-1)q+1th stage, and the START and STOP signals are taken at the output of the (d-1)q+k+1th stage (in a loop around sense if necessary) on the two chains. Numbers of delays for the P time interval samples are equal to k, but the samples are generated by different stages on the loop and may have different widths in existence of mismatchs.

3) Let k change from 1 to N and repeat 1) and 2), we can get sets of P time intervals with different nominal widths.

We assume τ_1 and τ_2 with mismatches obey N(τ_{10}, σ_1^2) and N(τ_{20}, σ_2^2) distributions, respectively. Considering a pair of two delay stages, the distribution of the delay difference $\tau = \tau_2 - \tau_1$ is N(τ_{20}-τ_{10}, σ_1^2+ σ_2^2). We redefine $\tau_j = \tau_o(1+\varepsilon_j)$, where τ_j is the delay difference of stage j, and ε_j obeys N(0, σ_ε^2=(σ_1^2+ σ_2^2)/ σ_0^2). If the trigger signal goes through k stages, the average delay is

$$\bar{t}_k = \frac{1}{P}\sum_{d=1}^{P}\sum_{j=1}^{k}\tau_{(d-1)q+j} = k\tau_o + \tau_o\frac{1}{P}\left(t\sum_{j=1}^{N}\varepsilon_j + \sum_{d=1}^{P}\sum_{j=1}^{s}\varepsilon_{(d-1)q+j}\right), \tag{4}$$

in which tq+s=k where t=0, 1… P-1 and s=1, 2… q. Going through similar derivations as in [5] gives an important result: $\overline{INL_k}$ ~ N (0, $\sigma_\varepsilon^2 s(q-s)/(pq)$). s=0.5q gives the maximum standard deviation of INL_k as

$$\sigma'_{INLk} = \sigma_\varepsilon \sqrt{N}/(2P). \quad (5))$$

This maximum value is decreased by $2P$ times as compared to the original time interval generator without DDEM. Therefore DDEM can significantly increase linearity of the time interval distribution.

B. Time Interval Generation with Dithering

Another method to improve linearity of the time interval distribution is to add dither to the DDEM structure as shown in Figure 2. The dithering block consists of a constant delay stage and a voltage-controlled (VC) delay stage with an N_d-bit low-resolution DAC that is easy to achieve high linearity. The structure of VC delay stage was discussed in [4].

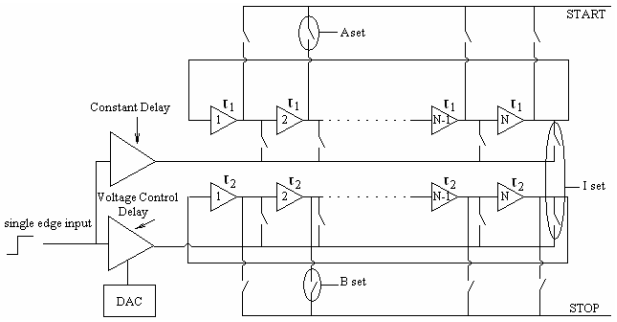

Figure 2. Time interval generation with dithering.

We only use the linear region of the voltage-delay relationship of the VC delay stage and set the constant delay at the center of that region. The dithering delay will have $K_d=2^{Nd}$ values from $-(K_d-1)\Delta_d/2$ to $K_d\Delta_d/2$, where Δ_d is the step size of dithering, and shift every delay generated by the DDEM structure K_d times.

Assume the probability density function (PDF) of time intervals generated by the DDEM is f(t), where t is the time difference, then the PDF generated by the dithered structure is

$$f_d(t) = \frac{1}{K_d} \sum_{i=-(K_d-1)/2}^{K_d/2} f(t - i\Delta_d). \quad (6).$$

It can be seen from (6) that dithering works as a low-pass filter that filters out non-uniform components in the PDF from DDEM.

C. TDC INL Estimation in Existence of Jitter

Noise sources, which are coupled onto the system from both on-chip and off-chip, introduce uncertainty in the timing edge of a signal, known as jitter. Jitter has significant effects on high accuracy test, especially in some serial structures where the jitter errors will accumulate, such as a VDL. In this section, we will discuss the effect of jitter on TDC test and the strategy we take to cancel the negative effect.

Assume there is a TDC under test with an N_D–stage VDL. Each stage's delay $\tau'_i = \tau'_o(1+\varepsilon'_i)+J_i$ has a mismatch term ε'_i from $N(0,\sigma'^2_\varepsilon)$ distribution and a random jitter from N $(0, J^2)$ distribution. The total delay at the k^{th} stage is

$$t'_k = k\tau'_o + \tau'_o \cdot \sum_{i=1}^{k} \varepsilon'_i + \sum_{i=1}^{k} J_i. \quad (7)$$

As to a specific TDC, the first two terms in (7) are fixed, while the jitter term is random. Thus, t'_k obeys $N(k\tau'_o + \tau'_o \cdot \sum_{i=1}^{k} \varepsilon'_i,\ kJ^2)$ distribution. It is obvious that the variance at each stage is proportional to the index of this stage, which is caused by the cumulative effect of jitter. So the uncertainty at the last several stages is large enough to draw our attention. In our proposed approach, we take multiple, N_r, measurements of a TDC and use the mean value of estimated INL_k's for a same code k from different measurements as the final test result to average out the jitter effect on each delay stage.

IV. Simulation Results

Simulation is done in MATLAB to validate the above analysis. In simulation, the TDC under test is modeled such that N_D=256, τ'_0=32pS, and σ'^2_D=2.89pS^2; DDEM TDC is modeled such that N_d=512, τ_0=32pS, σ_d^2=6.96pS^2, and P=64; dither is set that K_d=16, Δ_d=2pS, and σ^2=0.16pS^2; and N_r=16. A jitter with zero mean and 1 pS^2 variance is introduced into the system. Note that the following delay differences of each stage seem to be small, but the delay time of the two delay units composing the stage is large enough to be practically fabricated in an existing process.

Firstly, we compare the accuracy levels achieved by using different methods: DDEM only, DDEM plus dither, and DDEM plus dither plus multi-test. In Figure 3, the INL_k estimation errors with the three methods are plotted from top to bottom, respectively. The maximum error with DDEM only is 0.1735 LSI, the maximum with DDEM+dither is 0.0539 LSI, and 0.0221 LSI with DDEM+dither+multi-test. The last method has the best estimation performance with 0.7072 pS accuracy.

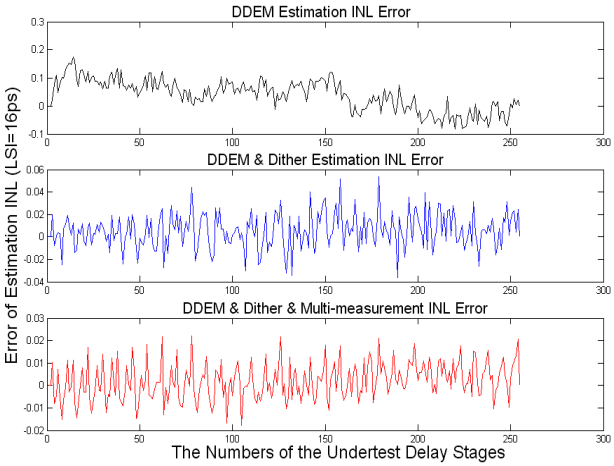

Figure 3. INL_k estimation errors by using different methods

Under the same assumption, maximum INL_k estimation errors of 100 different TDCs are tested by the

same DDEM TDC with dither are shown in Figure 4. From the plot we can see all the errors with DDEM+dither+multi-test are less than 1 pS. Although the nominal stage delays of both DDEM TDC and TDC under test are set to be equal, the testing accuracy is not limited by the nominal stage delay of the DDEM TDC, which can even be larger than that of TDC under test. As a result, the length of DDEM TDC can be reduced.

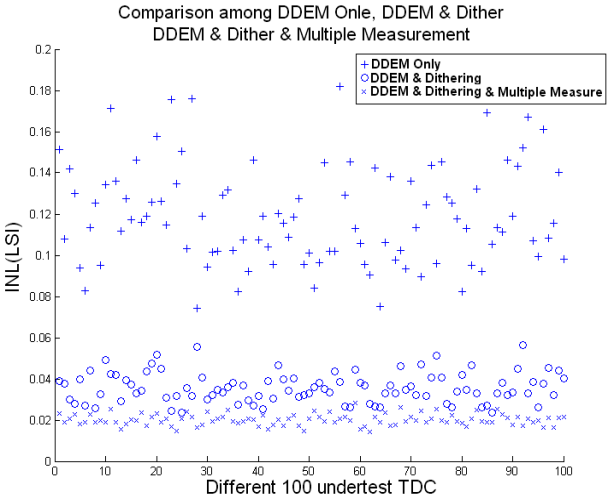

Figure 4. Maximum estimation errors for 100 different TDCs

For the test method proposed in this paper, the number of effective samples is $(N*R)*P*K_d*N_r$, where R is the ratio between the dynamic range of the TDC under test and the range of time intervals generated by the DDEM TDC, and the number in the parenthesis is the effective number of DDEM time intervals that fall in the range of the TDC under test. Therefore P, K_d, and N_r can trade off among themselves and determine an appropriate time interval density, when the total effective number does not change. Different factorization of the three parameters with the same total effective samples and a fixed factor are given in Table I.

Table I. Maximum Estimation Errors v.s. P, K_d, and N_r

P	N_d	N_r	Max Error(LSI)
64	16	16	0.0215
64	32	8	0.0205
128	16	8	0.0158

Meanwhile their INL_k estimation error curves corresponding to Table I setups are shown in Figure 5.

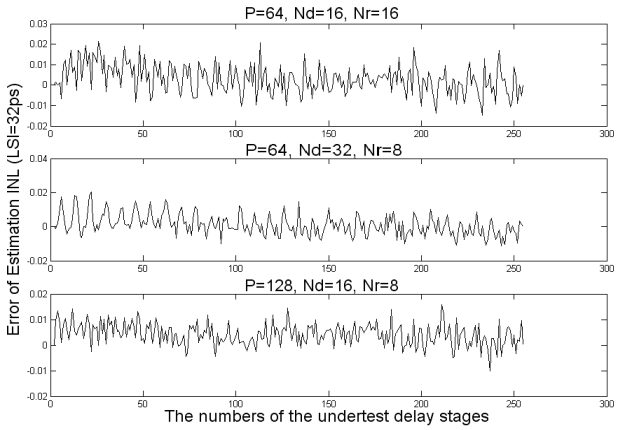

Figure 5. INL_k estimation errors with different P, K_d and N_r.

V. CONCLUSIONS

A cost-effective test strategy for TDCs is proposed in this paper. Considering uncertainty introduced by jitter as an inevitable negative factor, DDEM, dither and multi-test approaches improve the error performance of INL test step by step and achieve a high accuracy eventually, better than 1 pS, by implementing them together. On the other hand, the respective time and structure complexity level of the three testing parts can exchange among each other without accuracy loss. So this character provides much flexibility for the design according to other specific limitations. The DDEM approach does not require individual time interval lengths to be accurate or known. The proposed architecture mixes and rearranges unknown varying time intervals from an imprecise VDL by using DDEM and dithering to create an overall uniform distribution of time interval lengths. The proposed VDL is not only robust to parametric variations but also takes advantage of them to achieve high TDC testing performance. The uniform distribution of the time intervals from the DDEM VDL is the key enabler that allows for the accurate testing and calibration of all deterministic errors in the TDC. This in turn makes it possible to shift the TDC design focus from reducing parametric variations to minimizing inherent jitter and parasitics, leading to dramatic improvements in TDC repeatability and operating speeds.

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