A Two-Step DDEM ADC for Accurate and Cost-Effective DAC Testing

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Abstract— **This paper presents a scheme for testing DACs' static non-linearity errors by using a two-step flash ADC with deterministic dynamic element matching (DDEM). In this work, the structure of the two-step ADC, the switching strategy of DDEM, and the DAC test algorithm are discussed. The performance of the proposed approach is validated by using numerical simulation. Simulation results show that a low accuracy two-step ADC with an 8-bit coarse stage and a 6-bit fine stage is capable of testing a 14-bit DAC to 1-LSB accuracy by using the proposed DDEM strategy. This test approach has potential for build-in self-test (BIST) of precision DACs because of the low requirement on ADC performance and the simple element matching strategy.**

I. INTRODUCTION

As an interface between digital processing systems and the analog world, the digital-to-analog converter (DAC) is one of the most widely used mixed-signal integrated circuits [1]. Along with the continuous advance in communications theories and other technologies in the past a few years, more and more high-speed high-accuracy data conversion operations are required in various applications. Test of data converters is viewed as one of the most challenging problems in the area of analog and mixed–signal (AMS) test. Conventional DAC test approaches use measurement equipments with higher precision than a device under test (DUT) to characterize the performance of the DUT, which makes the design and manufacturing of the tester really a challenge and introduces high test costs, especially for testing high-resolution DACs.

Build-in self-test (BIST) is believed to be a promising alternative strategy for testing data converters. BIST strategies implement some or all test blocks on chip to make the test process easy and cost-efficient. A BIST scheme for DAC testing usually needs to have a measurement ADC fabricated on the same chip as a DAC under test. In the test mode, the analog output of the DAC is connected to the input of the ADC. Providing a digital input code to the DAC, its output voltage is measured by monitoring the digital output of the ADC. This is an all-digital test approach, and the input and output data can be generated and processed by an on-chip digital signal processing block. Conventionally, however, the measurement ADC is still required to be much more accurate than the DAC under test. It is very difficult and needs lots of area to build such an ADC on chip. Therefore some other BIST schemes have been investigated, such as using analog techniques [2].

Reference [3] and [4] discussed an approach of using a low accuracy current steering DAC with deterministic dynamic element matching (DDEM) to generate stimuli with high linearity for precision ADC test. Current sources in the DAC were dynamically re-arranged to repeatedly generate ramp signals. For an input code, the DAC gave out multiple output voltages with different combinations of current sources determined by a special DDEM switching sequence. The whole set of output voltages associated with all distinct input codes was almost uniformly distributed over its range and able to test the nonlinearity errors of ADCs with a high resolution. A similar method can be applied to DAC testing by using ADCs with DDEM.

In this paper, we will discuss how to use a low accuracy flash ADC with DDEM as a test device to measure the static nonlinearity error of DACs. Section 2 gives general definitions of DAC nonlinearity errors. Section 3 shows the DDEM method and its realization in flash ADCs. Section 4 proposes the structure of the two-step DDEM ADC. Section 5 analyzes the estimation of a DAC's INL and DNL by using the two-step ADC. Section 6 shows simulation results and Section 7 concludes the whole paper.

II. STATIC NONLINEARITY ERRORS OF DACS

The nonlinearity errors in a DAC come from variations and mismatches in the conversion circuitry, and are usually characterized by differential nonlinearity (DNL) and integral nonlinearity (INL). DNL is the maximum deviation in the output steps from the ideal value of one least significant bit (LSB). INL is the maximum deviation of the output transfer curve from a linear transfer curve which is often defined as a fit line passing through the end points. For an n-bit DAC, each analog output V_k corresponds to a digital input k, where k is from 0 to 2^n-1. The fit line through the two end points, V_0 and V_{2^n-1}, defines a linear transfer curve and the value of one LSB. LSB, DNL(k), and INL(k) are defined as following:

$$LSB = \frac{V_{2^n-1} - V_0}{2^n - 1}, \quad (1)$$

$$DNL(k) = \frac{V_{k+1} - V_k}{LSB} - 1, \quad (2)$$

$$INL(k) = \frac{V_k - V_0}{LSB} - k. \quad (3)$$

The overall INL and DNL are the maximum values of the magnitudes of INL(k) and DNL(k) respectively. From (2) and (3), we can see linearity testing of a DAC only needs to estimate the positions of V_k relative to V_0.

III. DDEM IN FLASH ADC

Dynamic Element Matching (DEM) is a strategy that attempts to reduce the effects of component mismatches on electronic circuits by dynamically rearranging the interconnections of matching-sensitive components. Reference [4] discussed using DEM in current steering DAC design. By rearranging the connections of unit current sources, multiple analog outputs were generated for one digital input. The distribution of all possible output voltages was studied, and analyses show that general characteristics of the DEM outputs could be what are illustrated in Fig. 1. Theoretically the outputs are nearly uniformly distributed over the output range except at the two ends. This result is valid when enough analog outputs are available for one input and the mismatched components can be rearranged arbitrarily. To satisfy these two conditions, complex control logic and long test time are needed.

DDEM reduced the hardware complexity and the test time by deterministically rearranging the components to get a reasonable number of outputs and satisfactory output distribution. It was proved to be a good approach to generate stimuli for ADC test and easily implemented in [4]. In this section, we use an n-bit R-string flash ADC as an example to explain how the proposed DDEM approach works. Typically, mismatches in a resistor string will cause nonlinearity errors in reference voltages and limit the accuracy of an ADC. So when design a flash ADC, a lot of efforts and die area are put on resistor matching. DDEM can be used to cancel the effects of mismatch errors.

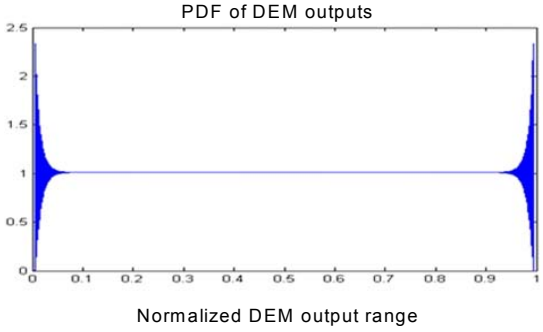

Figure 1. Probability density function of DEM output

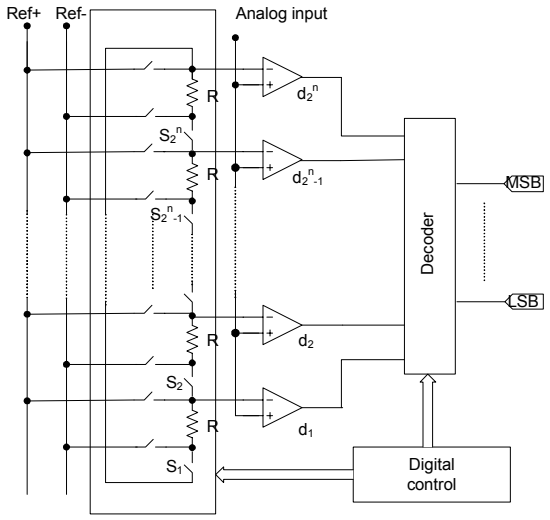

Figure 2. Structure of an n-bit DDEM flash ADC

Fig. 2 shows the structure of an n-bit DDEM flash ADC. Similar to a typical flash ADC, an R-string with N resistors of R forms a voltage divider that provides reference voltages, where $N=2^n$. Each comparator gives out a "1" when the analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0". The decoder converts thermometer codes to binary codes. Different from the conventional flash structure, resistors are physically connected as a loop via switches in the DDEM ADC. The loop can be broken at different positions by opening specific switches to build different R-strings, consequently different ADCs. N comparators are needed to make comparators be rearranged with resistors easily. The proposed DDEM strategy dynamically generates R-strings in such a way that all the resistors are almost equally used. Each time, one of P switches, S_i for $i=(j-1)*q+1, j=1, 2... P$, is open, where these P switches are uniformly distributed on the resistor loop. The parameter P is the number of different R-strings and so selected that $q=N/P$ is an integer. Connecting the two nodes of the open switch to external reference voltages, a set of internal reference voltages is generated. Therefore, P digital outputs are available for one analog input quantized by the DDEM ADC with different sets of reference voltages.

IV. DESCRIPTION OF A TWO-STEP DDEM FLASH ADC

The flash ADC provides the fastest conversion from an analog signal to a digital code and is ideal for applications requiring a large bandwidth. However, the resolution of flash ADCs is restricted to 8 bits by the large amount of power consumption, area, and input capacitance introduced by the 2^n comparators. To make the scheme suitable to high resolution test, a two-step flash ADC structure with DDEM is proposed. Fig. 3 illustrates the structure of the ADC.

This two-step structure uses a coarse quantization and a fine quantization to increase the resolution of the converter. It comprises a sample-and-hold stage, an n_1-bit coarse

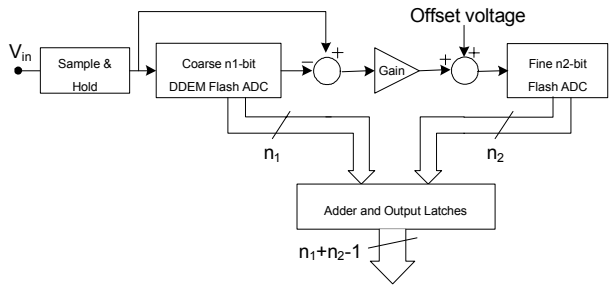

Figure 3. Block diagram of a two-step DDEM flash ADC

DDEM flash ADC and an n_2-bit fine flash ADC, a residual voltage generator, a gain stage, and a digital adder and output latches. The sample-and-hold stage is needed to compensate for the time delay in the coarse quantization and reconstruction steps. The coarse ADC does the conversion for the first n_1 bits. A residual voltage is generated by subtracting from the analog input the reference voltage right smaller than it, determined by the coarse ADC output, and the difference is amplified by the gain stage. In order to avoid missing codes, the full-scale range of the fine flash ADC is set to be equivalent to 2 LSBs of the coarse system. A constant offset voltage is added to the residual voltages to move them up to a desired input level for the fine ADC, where the middle part of the fine ADC's input range is. This shift operation can compensate for the errors in residual voltages introduced by comparator offset voltages. The final output code is a summation of shifted coarse and fine codes.

In this DDEM structure, mismatches in the coarse resistor strings are desired to spread out distributions of transition points after DDEM. This low matching requirement dramatically reduces the area consumption of the R-string. Because the full scale range of the fine stage is only equivalent to 2 LSBs of the coarse stage, the fine stage can greatly increase the test ability of the whole ADC, and accuracy and linearity of the fine stage are not critical to the test performance. So DDEM in the fine stage is not necessary. As shown in Section 6, the estimation accuracy is limited by the first stage and DDEM in the second stage doesn't help much.

V. ESTIMATION ALGORITHM AND ANALYSIS

In this section, the quantization process of an analog input is analyzed. Firstly, an n-bit single-stage DDEM flash ADC is used as an example. For each analog input V_i, which is from the DAC under test, P digital output codes, $d_{i,1}$, $d_{i,2}$... $d_{i,P}$, are obtained from the ADC. For j^{th} rearrangement of the resistors, the resistor string provides a transition point set $\{T_{j,1}, T_{j,2}... T_{j,N-1}\}$. Output code $d_{i,j}$ means first $d_{i,j}$ transition points in the j^{th} set are less than the input voltage V_i. To get the measurement m_i of V_i, we add up all the digital outputs $d_{i,1}$, $d_{i,2}$... $d_{i,P}$ together as in

$$m_i = \sum_{j=1}^{P} d_{i,j} = \sum_{j=1}^{P} \#\{T_{j,k} : T_{j,k} < V_i, k = 1,2,\cdots,N-1\} \quad (4)$$
$$= \#\{T_{j,k} : T_{j,k} < V_i, k = 1,2,\cdots,N-1, j = 1,2,\cdots,P\}$$

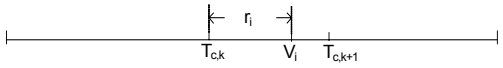

Figure 4. Input analog voltage relative to ideal transition points

If we plot all the transition points of the P ADCs obtained from DDEM on one axis, they are interleaved with each other and m_i is the number of points on the left of V_i as shown in (4). If P is large, the distribution of all the transition points is close to a uniform distribution, thus we can get a good estimation of the analog input from m_i. This process is very similar to the code density test of ADCs by using a DDEM DAC. Because transition points are not uniformly distributed at the ends of the DDEM ADC's input range, the input signal to the ADC, output voltages of the DAC under test, should be limited to the middle part of the whole range.

In the case of the two-step DDEM ADC, the estimation process is very complicated. The following shows some basic ideas. If $T_{c,1}$, $T_{c,2}$, ..., $T_{c,N-1}$ are the ideal transition points of the original coarse stage, the input analog signal can be expressed as $V_i = T_{c,k} + r_i$, where r_i is the residual voltage between $T_{c,k}$ and V_i. The position of the input signal V_i is shown in Fig. 4.

Assume for input V_i the outputs of the coarse DDEM ADC are $d_{c,i,1}$, $d_{c,i,2}$, ..., $d_{c,i,P}$, and $r_{c,i,1}$, $r_{c,i,2}$, ..., $r_{c,i,P}$ are the residual voltages which are supposed to be estimated by the fine stage with reasonable accuracy. For j^{th} rearrangement, the estimation of the input V_i is

$$m_{i,j} = T_{c,d_{c,i,j}} + r_{c,i,j} + \varepsilon_{Q,j}, \quad (5)$$

where the first term is the transition point for code $d_{c,i,j}$, and $\varepsilon_{Q,j}$ is the quantization error of the fine stage. The measurement of V_i is taken as

$$m_i = \frac{1}{p}\sum_{j=1}^{p} m_{i,j} = \frac{1}{p}\sum_{j=1}^{p}(T_{c,d_{c,i,j}} + r_{c,i,j} + \varepsilon_{Q,j}) \quad (6)$$
$$= T_{c,k} + \frac{1}{p}\sum_{j=1}^{p}(T_{c,d_{c,i,j}} - T_{c,k} + r_{c,i,j} + \varepsilon_{Q,j})$$

If the second part of the equation is a good estimation of r_i, m_i could be used to measure V_i. Usually there are some errors in the second part, which is due to deviation of the resistor values from the desired value. However, if P is large, these errors can be averaged out to an acceptable level.

VI. SIMULATION RESULTS

Simulations in Matlab are carried out to verify the proposed structure and previous analyses. In simulation, a 14-bit DAC is modeled as a device under test. The two-step DDEM flash ADC has an 8-bit coarse stage, and a 6-bit fine stage. The resistor strings in these two ADCs are generated by resistors from a Gaussian distribution with a nominal value of 1 and $\sigma = 0.1$, which can be easily achieved in practical design. It can be imagined that linearities of the resistor strings are poor. The offset voltages of the

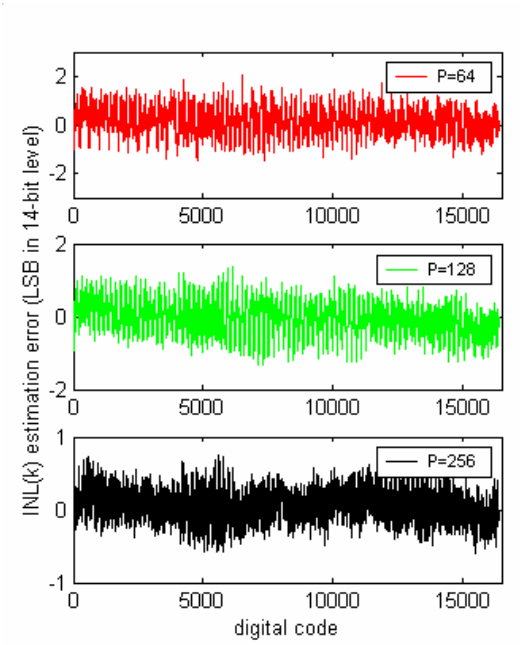

Figure 5. INL(k) estimation error with P=64, 128, and 256

comparators are set to be in the milivolt level. Fig. 5 illustrates the estimation errors in INL(k) tested by using the two-step DDEM flash ADC with P=64, 128 and 256, respectively. From these results, we can see that by increasing P, the estimation error is reduced. For each shift, all the analog outputs of the DAC need to be sent to the ADC. The larger is P, the more repeated ramp signals and longer test time are required. 100 different 14-bit DACs are test by the two-step DDEM ADC. Fig. 6 shows the relationship between the estimated INL values of different DACs and the true values, where the estimation errors are in the range from -0.2833LSB to 0.4089LSB. The results show that with P equal to 256, the proposed two-step DDEM ADC is capable of testing 14-bit DACs.

The fine stage could also be a DDEM flash ADC. Assume P_1 and P_2 are the iteration parameters of the coarse stage and the fine stage, respectively. Other parameters are the same as in the previous simulations. Fig.7 shows the

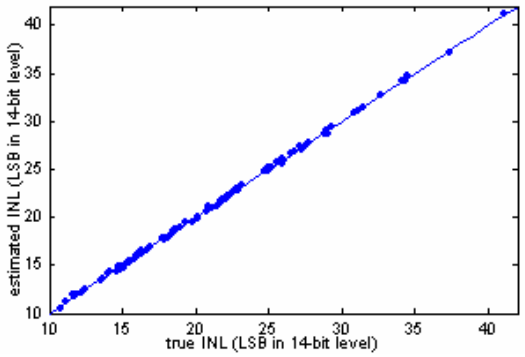

Figure 6. Estimated INL vs true INL for 100 14-bit DAC

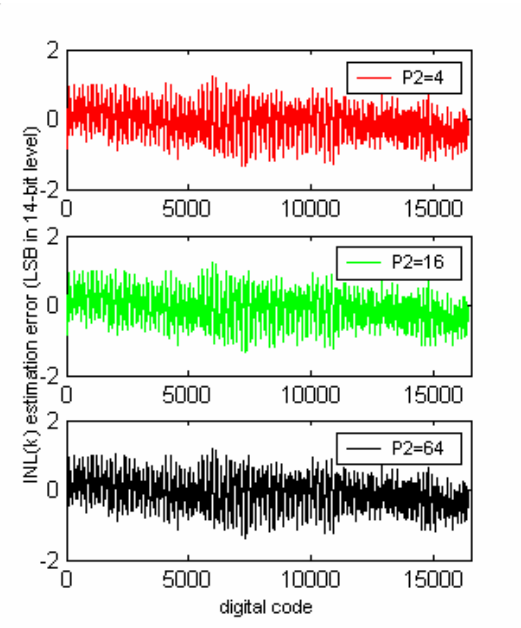

Figure 7. INL(k) estimation error with P_2=4, 16, 64

INL(k) estimation errors tested by the ADC with P_1=128, P_2=4, 16, 64. It can be seen that increasing the value of P_2 does not reduce the estimation error efficiently. The estimation error is limited by the coarse stage estimation.

VII. Conclusion

This work focuses on using a two-step DDEM flash ADC to test high-resolution DACs. The structure of the ADC is proposed. The DDEM strategy can be realized via simple digital control circuits. The structure and algorithm have been validated by numerical simulations. The iteration parameter P of the coarse stage, the number of the digital outputs for one analog input, is very critical to the test performance. Simulation results illustrate that a two-step DDEM flash ADC with 8-bit coarse resolution, 6-bit fine resolution and P equal to 256 is able to test 14-bit DACs.

References

[1] International Technology Roadmap for Semiconductors, 2003 edition, available online at http://public.itrs.net.

[2] J.-L. Huang and C.-K. Ong, "A BIST scheme for on-chip ADC and DAC testing," in Proc. Design, Automation and Test in Europe Conference and Exhibition 2000, pp. 216-220, March 2000.

[3] B. Olleta, L. Juffer, D. Chen and R. L. Geiger, "A deterministic dynamic element matching approach to ADC testing," in 2003 International Symposium on Citcuits and Systems, vol. 5, pp. V-533-536, May 2003.

[4] H. Jiang, B. Olleta, D. Chen and R. L. Geiger, "Parameter optimization of deterministic dynamic element matching DACs for accurate and cost-effective ADC testing," in Proc. 2004 International Symposium on Citcuits and Systems, vol. 1, pp. I-924-927, May 2004.