kT/C Constrained Optimization of Power in Pipeline ADCs

Yu Lin, Vipul Katyal, Randall Geiger
Dept. Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010, USA

Mark Schlarmann
Freescale Semiconductor, Inc.
Chandler, AZ, 85248, USA

***Abstract*—This paper presents a method to optimize the power consumption of a pipelined ADC with kT/C noise constraint. The total power dependence on capacitor scaling and stage resolution is investigated. With eight different capacitor scaling functions, near-optimal solution can be obtained. For 12bit pipeline ADC, the power decreases with effective number of bits per stage. This method can be easily extended to other resolution pipeline ADCs.**

I. INTRODUCTION

Reducing power dissipation is very important for portable battery powered devices such as digital cameras, cell phones, laptop PCs, etc. The analog to digital data converter (ADC) is one of the most commonly used building blocks of analog and mixed signal circuits used in such devices. Video-rate applications require a high resolution, high speed ADC. The pipeline ADC [1-5] is very attractive from both aspects.

The design of an ADC involves many issues related to specific requirements such as integral nonlinearity (INL), signal to noise ratio (SNR), voltage supply, data conversion range, etc. Lewis [1] examined the stage resolution effects on area and power assuming that power ratio between the sample and hold amplifier (SHA) and comparator is constant, which does not hold for different comparator and multiplying digital-to-analog converter (MDAC) architectures. The author concluded that minimizing the stage resolution minimizes the power dissipation. As suggested by Cline [2], low resolution pipelines favors low resolution per stage and slow capacitor scaling, which is defined as the capacitance ratio of the previous stage and the following stage, and high resolution pipelines favors high resolution per stage and rapid capacitor scaling. However, the approximation of linear relationship between the total capacitance and the total power is crude. Goes [6] gave a few design examples and concluded that the conventional wisdom of the use of the lowest possible stage resolution only applied to ADC with less than 10 bit resolution. Later on, Kwok [7] investigated the optimal stage resolution dependency of the power ratio of SHA to comparator for ADC to optimize power. It was suggested that for low power ratio of SHA and comparator less than 20, the optimal resolution is around 2 bit per stage (bps) with one bit redundancy. If the ratio is from 20~100, the optimal resolution stage will be 3 bps with one bit redundancy. For the same power ratio, high resolution pipeline ADCs favor low resolution per stage, which conflicts with the conclusion drawn by Cline [2]. Kwok also scaled the stage resolution to optimize the power. If the resolution of the ADC changes, the optimal combination of stage resolutions may change, which indicate that the results may not be applicable to different resolution ADCs.

In this paper, the strategy for power optimization with kT/C constraint will be developed. For a given total number of pipeline ADC bits, eight different capacitor scaling schemes are investigated. For each scheme, optimized power will be found with respect to effective number of bps.

II. POWER OPTIMIZATION

A. Power Consumption Sources

The block diagram of an h-stage m-bit/stage pipelined ADC is shown in Fig. 1. The individual stage is shown in Fig. 2. Each stage consists of a sample and hold circuit (S/H), an m-bit sub-ADC, an m-bit DAC and a switch capacitor amplifier. The blocks contained within the dashed rectangle are implemented with a single switch-capacitor circuit [2, 4] referred to as MDAC.

Each individual stage produces an m-bit binary code including one bit of redundancy. Therefore, the effective number of bits per stage is m-1 and the amplifier gain of the stage corresponds to this effective number of bits, i.e. for k^{th} stage the gain is given by $A_k = 2^{m-1}$. After the digital correction, the final resolution of the pipeline ADC will be n=h(m-1)+1.

For better performance of ADC, higher power consumption is required in the front end S/H. In a pipelined architecture, the first MDAC block can perform the function of a S/H and effectively reduces the overall power dissipation [3,5,8,9,10].

Without this front-end S/H, the sampling function and quantization function, i.e. MDAC and sub-ADC respectively, will be the dominant power contributor blocks for a high speed and high resolution pipeline ADC

[4]. The bias circuits, calibration circuits and other auxiliary circuits also contribute to the overall power but their contribution is small compared to the pipeline stages. Further, quantization function block power dissipation can be reduced by using dynamic comparator along with redundancy and digital correction [5, 11], eliminating the need to include it in the following analysis. Under these above mentioned condition, the sampling function block will be the bottleneck in the power minimization problem. The sampling function is mainly limited by the kT/C noise [4], which is related to the capacitor load and settling requirement of the amplifier, i.e., function of capacitor scaling and stage resolution [2].

B. Power Analysis of Pipeline Stages

As mentioned in Section II-A, capacitor scaling plays important role in overall power consumption. If the capacitors are not scaled from one stage to the next, the power of each stage will be the same and hence the total power will be large. Also, for large scaling factor, the total power consumption will be large [2]. Therefore, for optimized power, optimal scaling factor and optimal stage resolution have to be determined.

To simplify the problem, stage resolution will not be scaled. For the MDAC, which consists of switch capacitor amplifier, Fig.3, neglecting the DAC input will not change the analysis. During the phase φ_2, the feedback factor of the k^{th} stage switch capacitor amplifier of Fig.3 is given by

$$\beta_k = \frac{C_{fk}}{C_{uk} + C_{fk}} \tag{1}$$

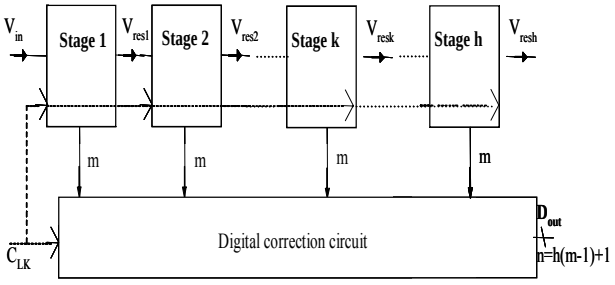

Fig. 1 Basic pipelined data converter architectures

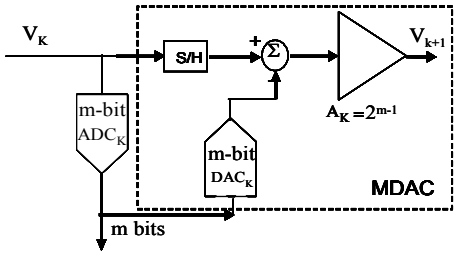

Fig.2. k^{th} Stage of basic pipelined data converters

For the switch capacitor amplifier during phase φ_2, the input referred RMS sampling noise voltage is given by

$$V_{rms,k} = \sqrt{\frac{kT}{C_{xk}}} \tag{2}$$

where C_{xk} is defined as the sampling capacitor for the k^{th} stage and is given by

$$C_{xk} = C_{uk} + C_{fk} \tag{3}$$

Consider a simple model of opamp, Fig. 4, modeled with a transconductance gain of g_{mk} and an output conductance of g_{ok}. The load $C_{x,k+1}$ represents the input capacitance to the next stage during the phase φ_1. The capacitor C_{uk} will be connected to DAC output. For a multi-bit per stage architectures, C_{uk} may be comprised of several capacitors in parallel, each connected to different DAC outputs.

The gain and the gain bandwidth product of the amplifier are given by

$$A_{0k} = \frac{g_{mk}}{g_{ok}}, \qquad GB_k = \frac{g_{mk}}{C_{x,k+1} + C_{xk}\beta_k(1-\beta_k)} \tag{4}$$

The magnitude of the closed loop pole is given by

$$p_{CLk} = \beta_k GB_k \tag{5}$$

It can be shown that the time required to settle to 1/4 LSB at the k^{th} stage is given by

$$t_{sk} = \frac{\ln 2\left(n+2-\sum_{i=1}^{k} m_i\right)}{p_{CLk}} = \frac{\ln 2\left(n+2-\sum_{i=1}^{k} m_i\right)}{\beta_k GB_k} \tag{6}$$

where m_i is the effective number of bits per stage.

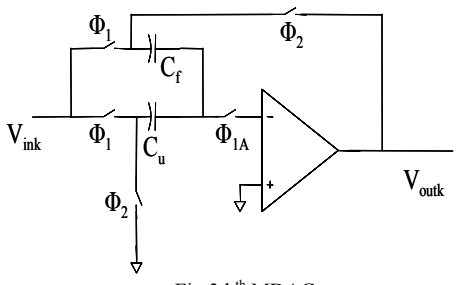

Fig.3 k^{th} MDAC

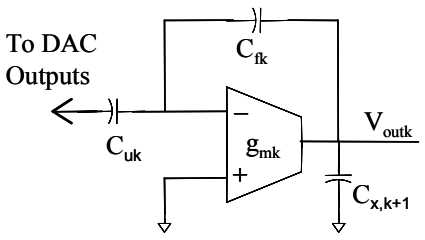

Fig.4 Operational amplifier of each stage

Assume now that the sampling noise contribution of stage k, referred back to the input, is given by

$$V_{rmseq,k} = \lambda_k \sqrt{\frac{kT}{C_{x1}}} \tag{7}$$

where λ_k relates the input refereed kT/C noise of k^{th} stage to that of the total capacitance of the first stage and hence λ_1=1. Since each of these noise sources is uncorrelated, it follows that the input referred RMS noise voltage due to all h stages is given by

$$V_{nrms} = \sqrt{\frac{kT}{C_{x1}}} \sqrt{\sum_{k=1}^{h} \lambda_k^2} \tag{8}$$

For acceptable noise budget of x bit below the ADC resolution, i.e.

$$V_{nrms} = \frac{V_{LSB}}{2^x} \text{ with } V_{LSB} = \frac{V_{REF}}{2^n} \tag{9}$$

the total 1st stage capacitance from (8) and (9) is given by

$$C_{x1} = kT \frac{2^{2(n+x)}}{V_{REF}^2} \sum_{k=1}^{h} \lambda_k^2 \tag{10}$$

For k>1, the noise of k^{th} stage referred back to the input of the pipeline is given by

$$V_{nrmseq\ k} = \frac{1}{\prod_{i=1}^{k-1} 2^{m_i}} V_{rms,k} = \frac{1}{2^{\sum_{i=1}^{k-1} m_i}} V_{rms,k} \tag{11}$$

It follows from (2), (7), and (11) that

$$\lambda_k = \sqrt{\frac{C_{x1}}{C_{xk}}} \cdot \frac{1}{2^{\sum_{i=1}^{k-1} m_i}} \tag{12}$$

This can be solved for C_{xk} to obtain

$$C_{xk} = \frac{C_{x1}}{2^{2\sum_{i=1}^{k-1} m_i} \lambda_k^2} \tag{13}$$

The transconductance gain of the amplifier is given by

$$g_m = \theta \frac{2I_Q}{V_{EB}} \tag{14}$$

where I_Q is the total quiescent current of the amplifier, V_{EB} is its excess bias of the input device, and θ is an architecture-dependent power efficiency penalty factor for the amplifier. It can be assumed that θ is independent of the port electrical variables of the amplifier, and θ≤1. For a single-stage single-ended amplifier, θ=1. From (4), (6) and (14), the quiescent current of stage k is given by

$$I_{Qk} = \frac{C_{xk}\beta_k(1-\beta_k) + C_{x,k+1}}{2\beta_k t_{sk}\theta_k} V_{EBk} \left(n + 2 - \sum_{i=1}^{k} m_i \right) \ln 2 \tag{15}$$

The total power dissipation in the ADC is given by

$$P = V_{DD} \sum_{k=1}^{h} I_{Qk} \tag{16}$$

Consider the special case where all stages are identical (for all k, m_k=m, β_k=β, θ_k = θ, and t_{sk}=t_s). This case will be used as a baseline for comparison. It follows from (12) that

$$C_{xk} = \frac{C_{x1}}{2^{2m(k-1)} \lambda_k^2} \tag{17}$$

with $\beta = \frac{1}{2^m}$, Equation (17) can be substituted into (15) to obtain

$$P = \left[\frac{V_{DD} V_{EB} kT \ln 2}{2 t_s \theta V_{REF}^2} 2^{2x} \right] \left[2^{2n+m} \right] \left[\sum_{k=1}^{h} \lambda_k^2 \right] \sum_{k=1}^{h} \left(\frac{n+2-km}{2^{2km}} \left(\frac{2^m - 1}{\lambda_k^2} + \frac{1}{\lambda_{k+1}^2} \right) \right) \tag{18}$$

Further, the first term in brackets on the right hand side of (18) can be normalized out since it is not a function of m, n or the λ variables. Thus, we will define the normalized power by the expression

$$P_{NORM} = \left[2^{2n+m} \right] \left[\sum_{k=1}^{h} \lambda_k^2 \right] \sum_{k=1}^{h} \left(\frac{n+2-km}{2^{2km}} \left(\frac{2^m - 1}{\lambda_k^2} + \frac{1}{\lambda_{k+1}^2} \right) \right) \tag{19}$$

III. RESULTS

From (19), we know that the optimization of the power for a given pipelined ADC involves determining m and λ_k variables for given values of n and x. Therefore, the total number of variable will be around h+1. In order to reduce the design variables, we examined eight different capacitor scaling functions. The 8 different capacitor-scaling functions are given below:

1. Equal stage noise (λ_k=1)

$$P_{NORM} = \left[2^{2n+m} \right] h \sum_{k=1}^{h} \left(\frac{n+2-km}{2^{(2k-1)m}} \right) \tag{20}$$

2. Noise Dominated by 1st stage (λ_1=1, λ_k=0.1)

$$P_{NORM} \cong \left[2^{2n+m} \right] \left[1 + \frac{h-1}{100} \right] \left[\frac{n+2-m}{2^m} \left(2^m + 99 \right) + \sum_{k=2}^{h} \left(\frac{n+2-km}{2^{2km}} 100 \left(2^m \right) \right) \right] \tag{21}$$

3. First stage provides approximately half of the noise ($\lambda_k^2 = \frac{1}{2^{k-1}}$)

$$P_{NORM} = \left[2^{2n+m} \right] \left[2 - \frac{1}{2^{h-1}} \right] \sum_{k=1}^{h} \left(\frac{n+2-km}{2^{2km}} \left(2^{k-1} \left(1 + 2^m \right) \right) \right) \tag{22}$$

4. First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{z(k-1)}}$, where z is a constant)

$$P_{NORM} = \left[2^{2n+m} \right] \left[\sum_{k=1}^{h} \frac{1}{2^{z(k-1)}} \right] \sum_{k=1}^{h} \left(\frac{n+2-km}{2^{2km}} \left(2^{z(k-1)} \left(2^m + 2^z - 1 \right) \right) \right) \tag{23}$$

5. First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{zm(k-1)}}$ where z is a constant)

$$P_{NORM}=\left[2^{2n+m}\right]\left[\sum_{k=1}^{h}\frac{1}{2^{zm(k-1)}}\right]\sum_{k=1}^{h-1}\left(\frac{n+2-km}{2^{2km}}\left(2^{zm(k-1)}\left(2^{m}+2^{zm}-1\right)\right)\right) \quad (24)$$

6. First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{z\sqrt{k-1}}}$ where z is a constant)

$$P_{NORM}=\left[2^{2n+m}\right]\left[\sum_{k=1}^{h}\frac{1}{2^{z\sqrt{k-1}}}\right]\sum_{k=1}^{h}\left(\frac{n+2-km}{2^{2km}}\left(2^{z\sqrt{k-1}}\left(2^{m}-1\right)+2^{z\sqrt{k}}\right)\right) \quad (25)$$

7. First stage provides more gain ($\lambda_k^2 = \frac{1}{2^{zm\sqrt{k-1}}}$ where z is a constant.)

$$P_{NORM}=\left[2^{2n+m}\right]\left[\sum_{k=1}^{h}\frac{1}{2^{zm\sqrt{k-1}}}\right]\sum_{k=1}^{h}\left(\frac{n+2-km}{2^{2km}}\left(2^{zm\sqrt{k-1}}\left(2^{m}-1\right)+2^{zm\sqrt{k}}\right)\right) \quad (26)$$

8. First stage provides more gain ($\lambda_k^2 = z\lambda_{k-1}^2$,where z is a constant)

$$P_{NORM}=\left[2^{2n+m}\right]\frac{1-z^{h}}{1-z}\sum_{k=1}^{h}\left(\frac{n+2-km}{2^{2km}}\right)\left(\frac{2^{m}-1}{z^{k-1}}+\frac{1}{z^{k}}\right) \quad (27)$$

For 12 bit ADC, numerical computation showed that case 4 with z=$\sqrt{2}$, case 5 with z=$\sqrt{\frac{1}{2}}$, and case 8 with z=0.38 have the best power performances as shown in Table 1. The other cases have much poorer performance, and are not shown here. From the results, it was observed that when m increases, the power decreases.

The optimal value of m is also going to be a function of ADC specifications. If the data conversion range is very small, then the offset of dynamic comparator will cause problems with the over-range protection of the ADC. To overcome this problem we have to use a static comparator and then the power consumption of the comparator can not be ignored. A typical dynamic comparator offset is approximately 10~20mV at speed of about 20MspS [12]. If a 2V pipelined ADC implemented in a 0.35um process has a maximum signal swing of only 1V, it may be more reasonable to have 2 effective-bits/stages instead of 4 to ensure adequate room for over-range protection.

TABLE I. THE POWER AND CAPACITANCE OF PIPELINE ADC

Effective bit/stage	**Normalized Overall Power and Capacitance**					
	Case 4 with z=1.414		***Case5 with z=0.707***		***Case8 with z=0.38***	
m	Power	Cap	Power	Cap	Power	Cap
2	31.463	1.915	31.463	1.915	31.449	1.925
3	21.497	1.637	21.251	1.389	21.557	1.647
4	16.843	1.532	16.302	1.194	16.902	1.540

IV. CONCLUSIONS

A method to optimize the power with kT/C noise constraint was proposed. Eight different scaling schemes were investigated to achieve near optimal solution. It was shown that for a 12 bit ADC, the total power decreases with the stage resolution provided comparator consumption is neglected. Although, the computation was done for a 12-bit ADC, the method can be easily extended to other resolution pipeline ADCs.

In this paper, only capacitor scaling was considered. Further study is needed to incorporate stage resolution scaling into the present capacitor scaling scheme for better understanding of the power optimized solution of a pipeline ADC.

REFERENCES

[1] Lewis, S.H., "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications", *IEEE transactions on circuits and systems II: Analog and digital signal processing,* Vol. 39, No. 8, Aug.1992, pp. 516-523

[2] Cline, D.W.; Gray, P.R.**, "**A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS", *IEEE Journal of Solid-State Circuits,* , Volume: 31 , Issue: 3 , March 1996, pp. 294 – 303

[3] S. H. Lewis et al., "A 10-b 20-MS/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, Mar. 1992. pp. 351–358

[4] T. Cho and P. Gray, "A 10 b 20 Msamples/s, 35mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, Mar.1995. pp. 166–172

[5] Cho, T.B.; Cline, D.W.; Conroy, C.S.G.; Gray, P.R., **"**Design considerations for low-power, high-speed CMOS analog/digital converters", *Low Power Electronics, 1994. Digest of Technical Papers.,* IEEE Symposium ,10-12 Oct. 1994 , pp. 70 – 73

[6] J.Goes, J.Vital, J. E.Franca, "Systematic Design for Optimization of High-Speed Self-Calibrated Pipelined A/D Converters", IEEE transactions on circuits and systems II: Analog and digital signal processing, Vol. 45, No. 12, Dec.1998, pp. 1513-1526

[7] Kwok, P.T. F. and Luong, Howard C, "Power Optimization for Pipeline Analog-to-Digital Converters", IEEE transactions on circuits and systems II: Analog and digital *signal processing,* Vol. 46, No. 5, May 1999, pp. 549-553

[8] Mehr, I.; Singer, L., " A 55-mW, 10-bit, 40-Msample/s Nyquist-rate CMOS ADC", *IEEE Journal of Solid-State Circuits,* Volume: 35 , Issue: 3 ,March 20000, pp. 318 – 325

[9] Chiang, Meei-Ling, U.S. application No. 09/506,284, filed Feb17, 2000, claims 1 to 27

[10] Chiang, Meei-Ling, U.S. application No. 09/506,208, filed Feb17, 2000, claims 1 to 17

[11] Abo, A.M.; Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, Vol. 34 , Issue: 5 , May 1999, pp. 599 - 606

[12] K.Kotani, T.Shibata, and T.Ohmi, "CMOS Charge-Transfer Preamplifer for Offset-Fluctuation Cancellationin Low-Power A/D conveters", *IEEE Journal of Solid-State Circuits*, Vol. 24 , Issue: 2 , Apr.1998, pp. 241 - 249