A Capacitor Sharing Technique for RSD Cyclic ADC

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Abstract— **A new cyclic ADC structure based on capacitor sharing is presented. This technique reduces the die area of the capacitors in the switched capacitor network by up to 50%. As a result, the proposed scheme also significantly reduces the power consumption requirement of the operational amplifier. This is achieved while maintaining the thermal noise performance and conversion rate of the conventional structure. A 10-bit, 2.3MHz cyclic ADC using the new structure is implemented in 0.5μm CMOS. Spectre simulation results of the new structure are presented.**

I. INTRODUCTION

A proliferation of portable devices such as laptop computers, mobile phones, personal organizers and digital music players has occurred in recent years. Due to their mobility, portable devices are battery powered. Although the density of digital integrated circuits on a chip has roughly followed Moore's law, battery capacities have not scaled as dramatically. Consequently, power efficient architectures must be used in digital as well as mixed signal circuits such as the analog-to-digital converters (ADCs).

ADCs enable the processing of real world analog signals in the digital domain and are ubiquitous in modern portable devices. Of the many ADC architectures, cyclic (or algorithmic) ADCs have the ability to perform analog to digital conversion with minimum area and low power at low to moderate frequencies. Traditional implementations of cyclic ADCs [1] involve a sample-and-hold (S/H) structure along with a gain stage, comparator, and sub-DAC. The hardware is used to implement a form of the binary search algorithm which takes n cycles to produce n-bit digital outputs with a one bit/stage structure. Other architectures combine the Redundant Sign Digit (RSD) technique [2], which compensates for loop offsets, with the inherent S/H functionality in Switched Capacitor (SC) amplifiers to replace the S/H in the traditional implementation with another gain stage [3]. Hence, with the addition of another sub-DAC and comparison block, the number of cycles required to produce n-bit digital output is reduced to $n/2$ cycles. Usually, each SC gain stage requires a separate operational amplifier (opamp), however, during the sampling phase of the SC amplifier, the opamp is not utilized. By captilizing on the this unused interval of the opamp, a single opamp can be shared among the two stages, similar to what is reported in [4]. We will refer to the this structure as the 'conventional structure' and discuss it further in Section II.

Two key observations are made on the operation SC amplifier and two-stage cyclic structure. In [5] it is observed that
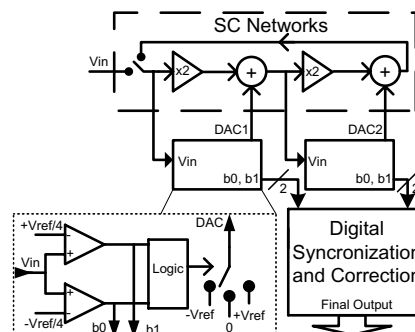

Fig. 1.   Two-Stage RSD cyclic ADC structure

the output voltage of a SC amplifier is actually held across its feedback capacitor. By treating this voltage as a "sampled voltage" for the SC gain stage, the need for an additional sampling capacitor can be eliminated [5]. The observation on the conventional two-stage cyclic structure is during the input sampling phase the second SC network capacitors are not utilized for a useful purpose. By utilizing the second stage capacitors in the input sampling phase, the technique of [5] is implemented in the proposed two-stage cyclic structure without having the drawback of alternatively sampling the input on different capacitors as it is the case in [5].

The proposed architecture automatically provides a limited degree of capacitance scaling similar to the concept of stage scaling of pipeline ADCs discussed in [6]. Hence, the new cyclic ADC is of smaller die area and power consumption levels than the conventional structures.

The proposed structure is discussed in Section III. Simulations results are shown in Section IV.

II. CONVENTIONAL CYCLIC STRUCTURE

A conventional, two-stage RSD cyclic ADC structure [3] is shown in Fig. 1 where it is assumed that the full-scale input range is $\pm V_{ref}$. A typical implementation of the SC network using what is commonly termed a "flip-around amplifier" is shown in Fig. 2. It consists of two sets of capacitors $CC1_a$, $CC1_b$ and $CC2_a$, $CC2_b$, switches, and a single shared opamp. The conventional cyclic operation is illustrated in Fig. 3 showing the states the SC networks are switched to and their sequence. For every clock phase, the ADC executes the following recursive function:

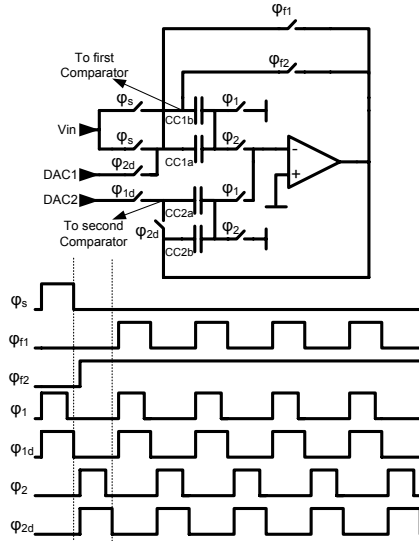$$V_i = 2 \times V_{i-1} - D_{i-1} \times V_{ref} \qquad (1)$$

Fig. 2. Simplified conventional SC networks for two stage RSD cyclic ADC with shared opamp. The non-overlapping clocks and delayed falling-edge clocks are also shown for 10-bit operation. A single-ended structure is shown for simplicity.

where the index i denotes the ith conversion cycle after a sample is taken, V_i is the ith residue voltage seen at the opamp output, $i \in [1, n-1]$, $V_0 = V_{in}$, and $D_{i-1} \in [-1, 0, +1]$. The value of $D_{i-1} \times V_{ref}$, the DAC output, is a function of the digits b_0, b_1 which are the comparison results of V_{i-1} against two reference values usually set at $\pm V_{ref}/4$ as shown in Fig. 1. The value of D_{i-1} is -1 if neither comparator is set, it is 0 if the lower comparator is set but the upper comparator is unset, and it is $+1$ if both comparators are set. For the switched-capacitor implementation shown in Fig. 2, V_0 (the input voltage V_{in}) is sampled on the capacitor pair $C1_a$, $C1_b$ at the start of the conversion. In subsequent conversion clock phases, the residue voltage is alternatively sampled on capacitor pairs $C2_a$, $C2_b$ and $C1_a$, $C1_b$ respectively.

The singed codes b_0, b_1 generated at the end of each clock phase are synchronized (simple multiplexing), transformed to binary, and then digitally corrected (simple digital addition) to give the final n-bit output digital word. Notice that only $n-1$ residue voltages are required to calculate the n-bit digital word that represents the sampled input voltage V_{in}.

The following observations are made:

1) The residue voltage is held across the feedback capacitor: In flip-around SC amplifiers, the residue voltage is impressed on the feedback capacitor. This fact suggests the use of the feedback capacitor in the SC amplifier as the sampling capacitor for the residue voltage. Therefore, no sampling capacitance is needed at the output of the SC amplifier. Amplification of the output voltage by two can take place by simply switching half of the feedback capacitor to form the flip-around structure [5].

2) The final residue amplification is not required: In the conventional cyclic operation shown in Fig. 3, the last residue voltage generated by $CC2_a$, $CC2_b$ and the opamp in the nth
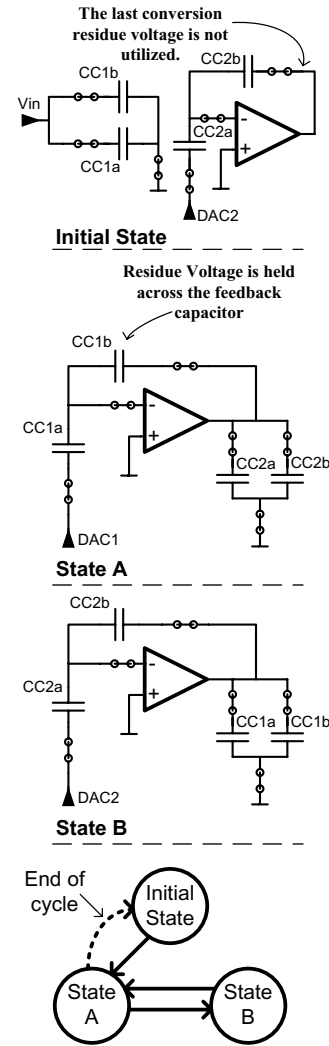

Fig. 3. Switching sequence of conventional SC networks

cycle is not utilized, because $CC1_a$, $CC1_b$, are sampling the input voltage. This suggests the idea of using $CC2_a$, $CC2_b$ as well as the opamp for other purposes. If needed, the opamp can be configured for offset cancellation.

A new structure, motivated by these two observations, is presented the following section.

III. PROPOSED CYCLIC STRUCTURE

The proposed SC structure's states and their sequence, which implement the same recursive function of (1), are shown in Fig. 4. In the 'Initial State' the capacitor pair $C2_a$, $C2_b$ and the capacitor pair $C1_a$, $C1_b$ both sample the input voltage. At the start of the next state 'State X', the pair $C2_a$, $C2_b$ are switched together to form one feedback capacitance for the first residue amplification, while connecting the $C1_a$, $C1_b$ pair to DAC1 voltage which is determined by the comparison result of the input voltage sampled in the 'Initial State'. Since the pair $C2_a$, $C2_b$ hold the value of the residue voltage when in 'State X', amplification during 'State B' can take place by
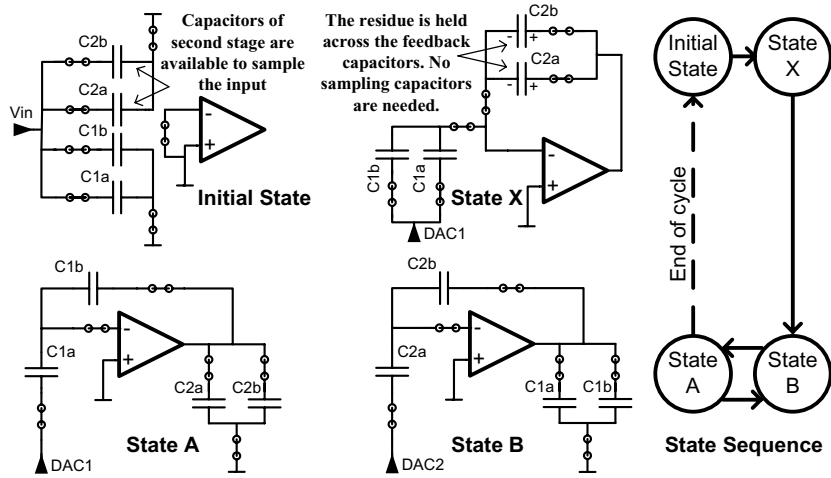
Fig. 4. Proposed switching sequence of SC networks for RSD cyclic ADC

simply connecting $C2_a$ to the output of the DAC2 voltage which is determined by the comparison result of the residue voltage of 'State X'. Since the capacitor pair $C1_a$,$C1_b$ is not needed for amplification during 'State B', these capacitors can be used to sample the residue voltage at the amplifier output. This process can then be repeated by alternating between 'State B' and 'State A' until the end of the conversion is reached. Then, the SC networks is switched back to the 'Initial State' from 'State A' to start a new conversion. The final SC networks for the proposed structure, along with the required clocks are shown in Fig. 5.

The rather subtle distinction between the proposed structure and the conventional structure is in the elimination of the extra sampling capacitance during the second step (the first 'State A' in the conventional case and 'State X' in the proposed structure). This subtle difference does, however, have a significant impact on overall performance as will be discussed in the following section.

A. Benefits of the proposed structure

The performance of a switched capacitor amplifier is dominantly determined by the size of the capacitors and it is this size difference that offers advantages for the proposed circuit shown in Fig. 5. It is well known that the capacitor size in a pipelined ADC becomes increasingly less important as one moves from the MSB stages to the LSB stages in the pipeline. Both reduced matching requirements and reduced effects of kT/C noise contribute to this relaxation in requirements. It was observed in [6] that an optimum capacitance stage-scaling factor for a pipeline ADC exists and is approximately equal to reciprocal of the interstage gain. Although aggressive capacitor scaling is practical in a pipelined architecture, capacitor scaling in a cyclic structure becomes temporal rather than spatial and circuit overhead makes it more difficult to take full advantage of capacitor scaling in a cyclic structure. But even in a cyclic structure, significant power and area benefits can be derived with appropriate capacitor sizing and scaling in the first one or
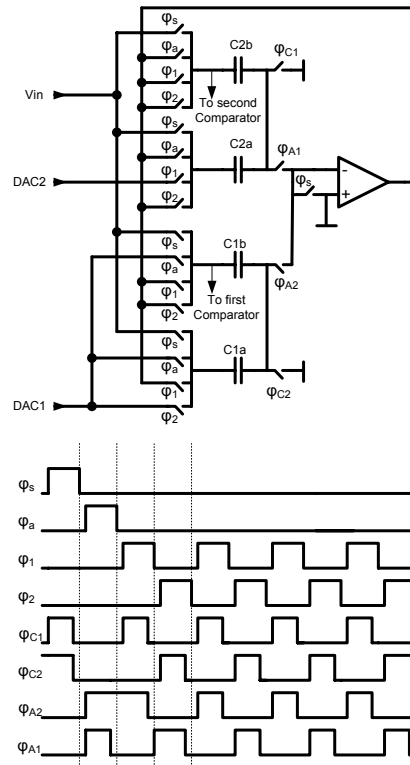

Fig. 5. Proposed SC networks for two stage RSD cyclic ADC with shared opamp together with the required clock signals for 10-bit conversion.

two conversion cycles. However, if capacitor scaling is used in a cyclic structure, making the temporal capacitor scaling factor equal to the reciprocal of the interstage gain should give near optimal performance for the cyclic structure as well. Since a 1-bit per clock-phase cyclic structure has a nominal interstage gain of two, good performance should be obtained if the capacitance from one stage to the next is decreased by a factor of 2. The proposed structure scales the sampling capacitance by a factor of 2 from the 'Initial State' to 'State

TABLE I

CAPACITIVE LOADING COMPARISON

Structure	Initial State	State X	State B	State A
Conventional	0.5C	N/A	2.5C	2.5C
Proposed	0	0.5C	1.25C	1.25C

Fig. 6. Reconstructed simulation spectrum of 100KHz sinusoidal input signal digitized at 2MHz. THD=-76.11dB, SFDR=74.95dB

X'. The same 'kT/C' noise performance at sampling input is maintained when comparing the proposed structure of Fig. 5 with the conventional structure of Fig. 2. This is true as the capacitors in the two circuits will be related by the expressions $C1_a + C1_b = CC1_a$ and $C2_a + C2_b = CC1_b$.

Table I shows the opamp's capacitive loading in each state for both the conventional circuit and the structure of Fig. 5 assuming that all of the conventional and proposed structures' capacitors are equal to '1C' and '0.5C' respectively, were C is an arbitrary unit. Note that the maximum capacitive load of the proposed structure has been reduced by a factor of 2 from '2.5C' to '1.25C' and it is this reduction in total capacitance that not only provides an area reduction for the layout of the capacitors but a significant power reduction in the design of the operational amplifier when the resolution of the cyclic structure is large as well. A fairer comparison may involve scaling the capacitors $CC2_a$ and $CC2_b$ to '0.5C' each. However, even with this scaling, the opamp will still be required to drive a maximum load of '2.25C' in 'State B' for the conventional sequence of Fig. 3. On the other hand, the opamp in the proposed structure would still only need to drive a maximum load of '1.25C'. Using a first-order model for the opamp, it can be shown that this results in a 44% reducion in this dominant power-consuming component. It is more common to have all of the capacitors of the conventional implementation equal, and hence a 50% power reduction is more realistic. The energy savings does depend on the architecture of the opamp and circuit parasitics such as the ON-resistance of the switches and parasitic capacitances. If these effects are included, the energy savings will be reduced but significant benefits would still be obtained.

Unlike the pipeline structure in [5], the proposed 2-stage cyclic structure samples the input voltage on the same set of capacitors at start of every conversion. Hence, every conversion will suffer consistent gain errors and therefore the proposed structure of Fig. 5 will not introduce a new source of harmonic distortion as in [5].

B. Design Issues

In the proposed SC switching sequence, 'State X' introduces two series switches in the signal path in the SC network. This suggests an increase in the time constant of the opamp in this state. However, as indicated by Tabel I, the loading of the opamp is reduced by a factor of five over the conventional implementation and this compensates for this effect well enough to make settling of 'State X' in the implemented ADC faster than 'State A' and 'State B'. Another design issue was the switching complexity of the proposed structure.
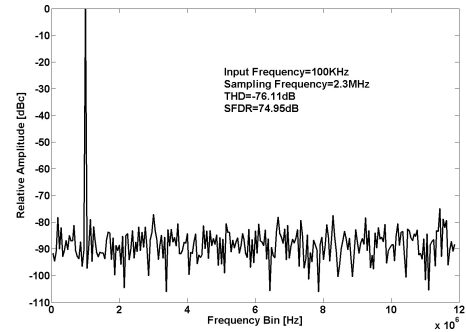
However, as shown in Fig. 5, dummy switches were added to simplify clocking while having better layout matching for the capacitors.

IV. IMPLEMENTATION AND SIMULATION RESULTS

The proposed structure was used in the design of a 10-bit, 2.3MHz cyclic ADC in a 0.5μ CMOS process. The opamp architecture is a cascode-cascade structure for high gain and large signal swing. The comparators are dynamic comparators for lower power consumption. The sampling switches are bootstrapped to accommodate the input signal swing. Spectral simulation results are shown in Fig. 6. Although not shown, the ADC demonstrated complete 10-bit performance for low frequencies and for frequencies up to near the Nyquist rate. The thermal noise and mismatches of circuit devices are not incorporated in the simulation results presented.

V. CONCLUSION

A new cyclic ADC structure that is built upon a conventional two stage RSD cyclic ADC with a shared opamp was introduced. The new structure can reduce the total capacitance by upto 50% and reduce the capacitive loading on the opamp by 50% as well thus resulting in a reduction of the opamp power consumption and a reduction in the area needed for the capacitor layout. This reduction in capacitance and power was achieved while maintaining the same SNR and conversion speed performance of the conventional implementation.

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