# A New Design Technique for Rail-to-Rail Amplifiers

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***Abstract* — A design technique for rail-to-rail operational amplifiers is presented. The technique adds dummy pairs to sense the common mode range of the input differential pair and adjusts the output current accordingly. An amplifier built in the TSMC 0.25µ process shows a DC gain of approximately 84dB. The amplifier provides high gain for a wider range of output voltages. Design considerations for reducing the impact of the additional circuitry on the core are provided. The technique described can be adapted for use with traditional fully-differential rail-to-rail amplifiers.**

## I. INTRODUCTION

As the industry migrates to nanometer CMOS processes, the supply voltage is getting scaled down for reliability. Although a boon for the digital circuits, the reduced supply voltage has made the design of analog circuits even more challenging. Operational amplifiers (opamps) are at the heart of many applications. The need for new opamps that are able to operate with reduced supplies while providing wide input and output swings has increased. Lower supply voltage necessitates the use of cascading or using active cascodes. However, such techniques may not always be feasible. The fact that threshold voltage of MOS transistors does not scale well with the supply and exhibits large variations over temperature and process corners limits the operation range of regular opamp topologies. New techniques that allow rail-to-rail operation of opamps have the potential of wide usage. In this work, we propose a new technique to enhance the gain characteristics of rail-to-rail opamps. The technique may be adapted for use with different input rail-to-rail stage architectures and can find application in regular and low supply processes.

The need for the rail-to-rail operation has resulted in many innovative solutions. Some recent solutions have used a single input amplifier by using level shifting, supply voltage doubling, and bulk-driven pairs, to name a few [1]-[3]. However, typical rail-to-rail opamps have their input applied to dual PMOS and NMOS input stages simultaneously [4][5] as shown in Fig. 1. Such an arrangement allows the input common-mode to vary from rail-to-rail as one pair takes over when its dual starts to turn off. However, if the gain of the opamp is divided between the input and the output stages, the output stage may not provide gain for the entire range of operation due to its dependence on the output voltage. The overall gain of the opamp then becomes a function of the output swing and deteriorates when the output voltage approaches the rail voltages. The technique presented in this paper alleviates this aspect of the amplifier behavior and extends the output voltage range where high gain remains available. The proposed scheme adds dummy transistors in parallel to the dual input stages that share the same tail current sources and provide additional current to the output stage when needed. When one of the input pairs is turned on, its corresponding dummy pair remains off. As the input pair turns off, its dummy pair turns on providing a substitute DC current to the output stage of the opamp. Consequently, the gain of the opamp remains high for a wider range of output voltages.

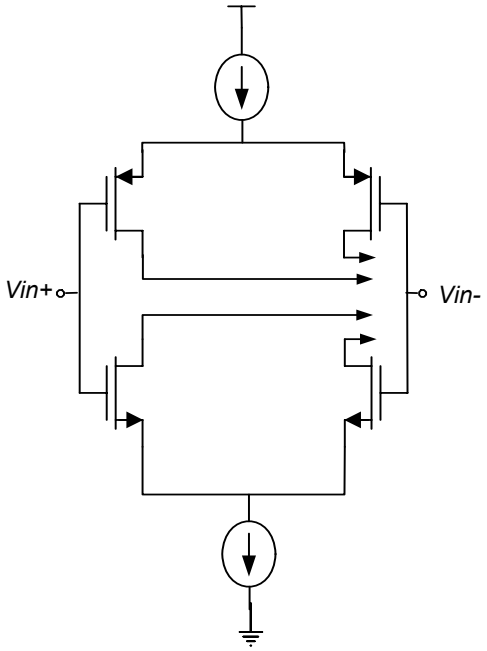


Figure 1. Typical dual input pairs for rail-to-rail amplifiers

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Section II presents the basic structure of the typical and the proposed circuit. Section III details the operation of the circuit followed by some design consideration. Simulation results are presented in Section IV.

## II. CIRCUIT OPERATION

The proposed opamp is shown in Fig. 2. The input of the opamp is comprised of dual p- and n-channel differential input pairs. Each input pair works independently of its dual providing the gain for its own range of operation. The outputs from the two dual cores are passed on to the second stage. For the n-type input stage, transistors M1, M1a, M2, M2a, and MnTail form the core amplifier. The output voltage of the differential pair is applied to the transistor M5. The transistors inside the dashed boxes are the addition to the base structure. For each input pair, a dummy pair is added to its output. As explained in Section III, the dummy pair can also have a voltage controlled resistor in series with the common source node connecting it to the common source of the input pair. M11 and M11a form the dummy pair that monitors the average of the output voltages of the input pair.

The operation of the circuit can be divided into three modes corresponding to the three ranges of common-mode input voltage: only the n-input pair is conducting, only the p-input pair is conducting, and when both the input pairs are conducting. Consider the circuit when the input common-mode level is in a range high enough to turn the p-input pair off. For this range of input common-mode values, the n-channel pair would conduct fully and provide gain. Since the p-input pair is turned off, the p-type dummy pair (M12, M12a) turns on and mirrors dc current to M8. At the same time, the dummy pair (M11, M11a) is fully turned off. Consequently, M6 and M7 remain off. The gain of the circuit during this mode can be written as

$$A_1 = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \cdot \frac{g_{m5}}{g_{ds5} + g_{ds6} + g_{ds7} + g_{ds8}} \qquad (1)$$

where $g_{ds6}$ and $g_{ds7}$ are designed to be very small, as explained in Section III. Similarly, the gain of the opamp for the dual case of p-input and the n-dummy pairs conducting is given by

$$A_2 = \frac{g_{m3}}{g_{ds3} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds5} + g_{ds6} + g_{ds7} + g_{ds8}} \qquad (2)$$

Again, both $g_{ds5}$ and $g_{ds8}$ are very small by design. For the mode when both the pairs are conducting, the total gain is the sum of $A_1$ and $A_2$ in (1) and (2) with $g_{ds7}$ and $g_{ds8}$ very close to zero. During this mode of operation, the dummy pairs should have minimal impact on the operation of the opamp. The output transistors M7 and M8 are turned off and the opamp provides the maximum gain to small signal differential inputs.

Another way to look at the role of M7 and M8 is to consider them as active loads. For example, when M5 is almost turned off and M6 is conducting, the gain of the second stage deteriorates. In the proposed technique, as M5 turns off, transistor M7 turns on and behaves as a current source boosting the gain for the output stage. The same holds true for the other half of the circuit in its active operation. As a result, the opamp is capable of providing high gain over a wider voltage range than the regular output stage even when the output voltage swings closer to a rail supply.

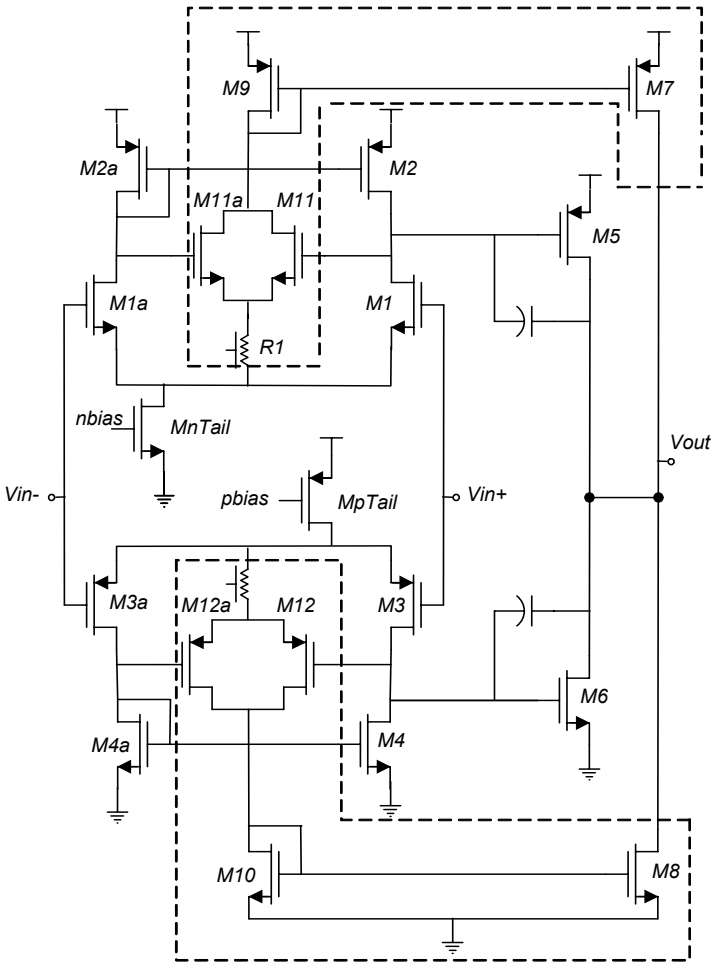


Figure 2. Schematic of the proposed opamp

## III. DESIGN CONSIDERATIONS

For the circuit to work properly, we need to make sure that the dummy transistors do not "steal" too much current when its corresponding input pair is turned on. We propose two strategies to minimize the impact of dummy transistors on the main circuit in such circumstances. First, the dummy transistors should be made much smaller than the corresponding input pairs. Since the dummy transistors add to the parasitic node capacitance at the drains of their corresponding input pairs, making their sizes small reduces their parasitic contribution. Second, we need to make sure that if an input pair is conducting, its corresponding dummy pair is off. For the case when input common-mode voltage in the mid range and the dummy pairs may start to conduct some current, a voltage controlled resistor can be added to

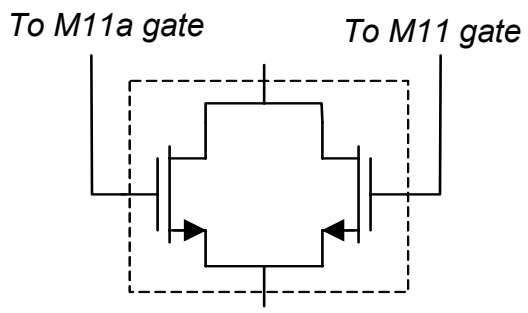


Figure 3. An implementation of voltage-controlled resistor

the source of the dummy pairs in order to reduce the $V_{gs}$ available to them. This helps ensure that the influence of the dummy pairs on the operation of circuit is minimal. Resistor value can be controlled by the average of the differential outputs of the first stage. Averaging can be done with switched capacitors or any other averaging technique. For the purpose of this work, each source voltage controlled resistor was implemented as shown in Fig 3. In this case, transistors M11 and M11a need to be in the ohmic region. It should be noted that this resistor might not be needed for lower supply voltages. For a given set of supply voltage, threshold voltages, and the desired swing at the drains of the input stages, the designer can choose to add or skip this resistor. However, whenever possible it would be better to add the resistor as it would help reduce the dummy pair's impact on the input pair's operation.

To reduce the offset voltage of the opamp, we need to make the input pairs transistors large. For newer processes, increasing the gate lengths of M1, M1a, M3, and M3a also helps with increasing the input range since threshold voltage of those transistors is a function of the gate length. Unfortunately, such a solution slows down the opamp

The technique described in this paper was implemented for a single-ended opamp. However, this technique is not only applicable to fully-differential opamps but may actually be more suitable for such structures since the differential outputs of the first stage are better matched around the quiescent point. Consequently, the averaging of the outputs would be more accurate.

## IV. Simulation Results

The proposed technique was implemented for a regular two-stage single ended Miller compensated opamp in TSMC 0.25µm process. The open loop DC output and its derivative around the high-gain transition point are plotted in Fig. 4. Simulations show a nominal DC gain of approximately 84dB with 2.5V supply.

To observe the output swing behavior, the opamp was set up in unity gain configuration. The input and output voltages for the configuration are plotted in Fig. 5. The output follows the input very closely and tapers off when reaching within 100mV of the supply. The inset in Fig. 5 shows the output

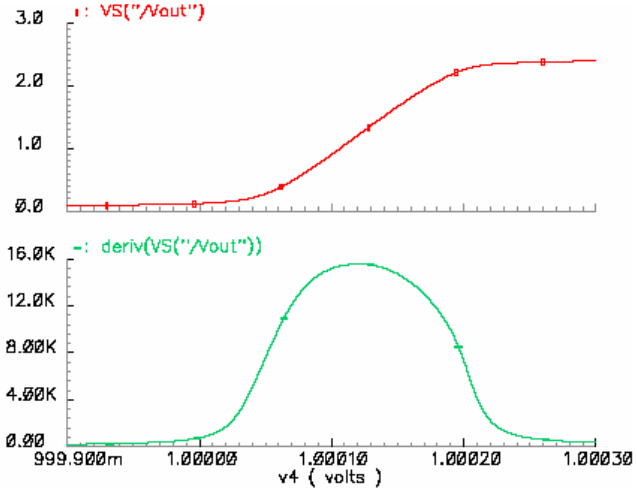


Figure 4. DC open loop output and gain

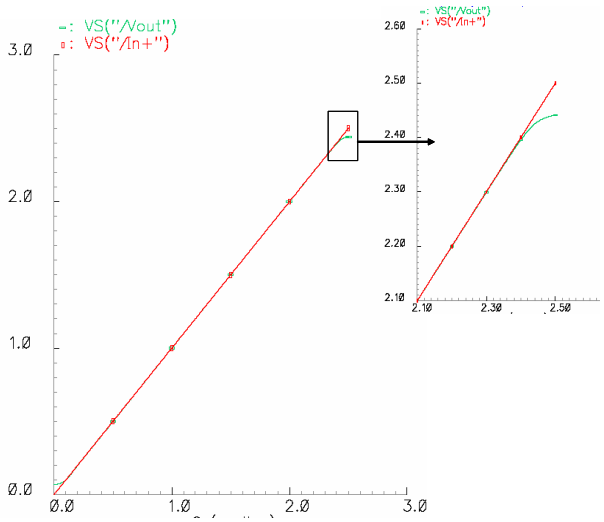


Figure 5. Unity gain input and output voltages

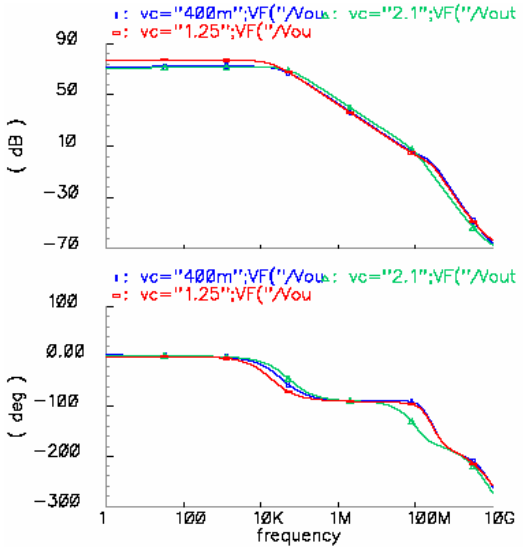


Figure 6. Frequency response showing open loop gain and phase for different input common-mode values

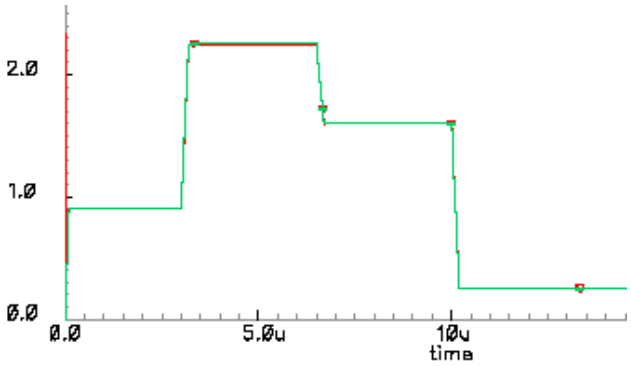


Figure 7. Unity gain configuration transient response for stability check

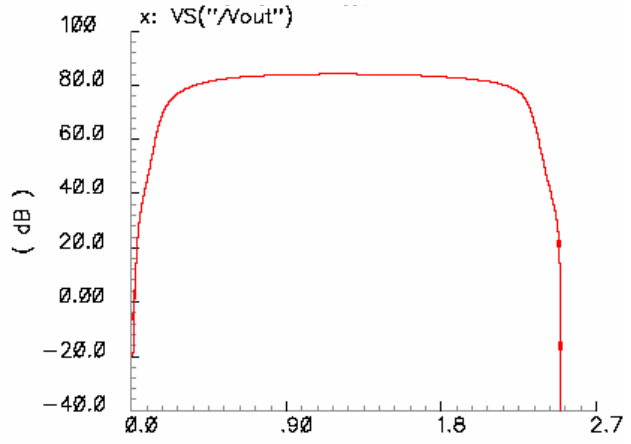


Figure 8: Open loop gain versus the output voltage swing

tapering off. This behavior is to be expected since the gain of the output stage drops when $v_{ds}$ of the output transistor becomes less than $v_{dsat}$. The opamp shows rail-to-rail operation and exhibits a DC gain in the range of 72dB to 84dB for input/output in the range of 0.2 to 2.3V and a DC gain in the range of 52dB to 84dB for input/output from 0.12V to 2.4V.

The frequency response of the opamp is shown in Fig. 6. The opamp has unity-gain bandwidth of 177MHz when both the pairs are on and a phase margin of approximately 68°. Simple Miller compensation was used in this implementation where two capacitors with series resistors (not shown) are connected between output of the second stage and outputs of the input stages. The unity gain frequency drops to approximately 150MHz when one of the pairs is on and the other pair is off resulting in DC gain of 73dB and a phase margin of 60 degrees. The two compensation capacitors and nulling resistors are made equal when the input pairs have equal transconductances and when M5 and M6 have equal gains. Independent compensation is required for mismatched transconductances and gains. The parallel paths of the first stages result in a left half plane zero at high frequency. In order to verify the stability, fast varying step inputs with transition time of about 10ns were applied to the opamp in unity-gain configuration loaded with 0.6pF capacitor. As can be seen from the transient analysis plot in Fig. 7, the output followed the input closely without oscillations.

Figure 8 shows the gain of the opamp for a range of output values. As expected, maximum gain is achieved in the mid-range of the output voltages and the gain drops off as the output voltage swings closer to the rails. However, the range in which the opamp has high gain is wide and high gain is maintained for this range of output values. Although, the gain does drop off but the drop is more gradual and happens closer to the rail voltages. As a result, this structure is suitable for applications that require high gain for a wide range of output voltages.

## V. Conclusions

A technique to improve the performance of rail-to-rail amplifiers was presented. Additional transistors added to the output stage help keep the gain high for higher input/output voltage swings. The technique was implemented for a single-ended opamp in TSMC 0.25µ process. Simulation results show a DC gain of approximately 84dB and a unity gain bandwidth of 177 MHz while consuming a total current of 1mA. Compensation cap size is 1pF each with a load cap of 600fF. The presented technique can be used with other rail-to-rail input-stage implementations as well as fully-differential amplifiers.

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